

DIGITAL CLOCK
A PROJECT REPORT
IN
DIGITAL ELECTRONICS

Submitted by:

RISHABH SINGHAL 2K19/CO/317

RAHUL AGGARWAL 2K19/CO/302

Under the supervision of

PROF. VARUN SANGWAN



DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

MAY, 2021

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

We, RISHABH SINGHAL & RAHUL AGGARWAL, 2K19/CO/317 & 2K19/CO/302.
Second year students of B.Tech. Computer Engineering, hereby declare that the project
Dissertation titled "Digital Clock" which is submitted by us to the Department of
Computer Engineering, Delhi Technological University, Delhi.

Place: Delhi

RISHABH SINGHAL

Date: 20-May-2021

RAHUL AGGARWAL

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CERTIFICATE

We hereby certify that the Project Dissertation titled "Digital Clock" which is submitted by

RISHABH SINGHAL & RAHUL AGGARWAL 2K19/CO/317 & 2K19/CO/302.

Computer Engineering Department, Delhi Technological University, Delhi.

Place: Delhi

PROF. VARUN SANGWAN

Date: 20-May-2021

SUPERVISOR

ABSTRACT

In this project we have created the simulation of a digital clock with the aid of the “Proteus Software”, with the help of a “74HC192” IC. This simulation/prototype made perform the exact function a real clock/stop watch performs.

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All glory and adoration be to the Almighty God for enabling us to complete this report. We have taken efforts in this project. However, it would not have been possible without the kind support and help of many individuals and organizations.

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INTRODUCTION

A digital clock is a type of clock that displays the time digitally (i.e. in numerals or other symbols), as opposed to an analogue clock, where the time is indicated by the positions of rotating hands.

Digital clocks are often associated with electronic drives, but the "digital" description refers only to the display, not to the drive mechanism. (Both analogue and digital clocks can be driven either mechanically or electronically, but "clockwork" mechanisms with digital displays are rare).



Fig.1 Digital Clock

COMPONENTS ASSOCIATED WITH ALL TYPES OF CLOCKS

No matter what type of clock is being considered, they all have some components in common.

No matter what types of technology or electrical components are used in a clock they will all

share these features or qualities that make them a clock or a time keeping piece:

- ✓ Power supply or source
- ✓ A time-base or counter that keeps time and is the heart of the clock, or its heartbeat
- ✓ Components which break down the time base into components: seconds, minutes and hours
- ✓ Some way of displaying the time (analog clocks use a face and hands, digital uses a lighted display)

Digital clocks are not a lot different than analog clocks except that they handle the basic time keeping functions using all electronic components instead of mechanically. For instance, digital clocks use an electronic power supply, either AC power from an outlet in the wall or from a battery. It also has a time base that is electronic and “ticks” at an accurate rate. And a digital clock has an electronic “gear mechanism” usually called a counter. And for the display the digital clock typically uses one of two kinds of lights. It will use either Light Emitting Diodes (LED) or a Liquid Crystal Display (LCD) to display the lighted time

HOW THE DIGITAL CLOCK WORKS?

An oscillator is needed for any type of clock to work. In a digital clock, this is usually provided by using a crystal which is made out of glass. As an electric charge passes through the crystal, it will change shape slightly and make a very light sound. The sound which is heard at a regular frequency is then converted into an electronic signal. By using a series of counters, the oscillations from a 60 Hertz oscillator is reduced to a 1 Hertz oscillation. The first counter will count one for each set of ten oscillations, and the other one will count one

for each six “tens” oscillations. This sets up the 1 Hertz signal so that it can pass seconds because the actual definition of 1 Hertz is one oscillation for each second. The six counter sets up the hours, since it counts for 6 sets of 10 – or 60. Each of the counters is connected to an electronic chip that signals to the display which uses lights to display the time.

This LED or LCD light display is called a “7-segment display.” This is because there are seven segments that can light up to display a number. For instance, the number 8 uses all 7 lights. But the light segments are designed to be able to light up in any array to display the numbers 0 to 9. These lights are situated on the display so that they display two sets of two digit numbers. When the digital clock reaches 12:59 and goes to 1:00 it essentially resets or starts over. The electric components in a digital clock are designed so that they have a built-in processor which basically looks for a “13” in the hours display. When it occurs, it resets the counter back to 1. Users can also reset the time using digital buttons that are installed on the clock in some accessible location. These buttons allow increased frequencies so that the numbers more much faster.

THE 74HC192 IC

The 74HC192 is asynchronously presentable BCD Decade and Binary Up/Down synchronous counters, respectively. Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input (PL)\. The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input).

A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and CLock-Down inputs, respectively, of the next most significant counter.

FEATURES

- ✓ Synchronous Counting and Asynchronous Loading
- ✓ Two Outputs for N-Bit Cascading
- ✓ Look-Ahead Carry for High-Speed Counting
- ✓ Fanout (Over Temperature Range)
- ✓ Standard Outputs 10 LSTTL Loads
- ✓ Bus Driver Outputs 15 LSTTL Loads
- ✓ Wide Operating Temperature Range -55°C to 125°C
- ✓ Balanced Propagation Delay and Transition Times
- ✓ Significant Power Reduction Compared to LSTTL Logic ICs
- ✓ HC Types
- ✓ 2V to 6V Operation
- ✓ High Noise Immunity: $\text{NIL} = 30\%$, $\text{NIH} = 30\%$ of VCC at $\text{VCC} = 5\text{V}$
- ✓ HCT Types
- ✓ 4.5V to 5.5V Operation

- ✓ Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
- ✓ CMOS Input Compatibility, $I_L \leq 1\mu A$ at V_{OL} , V_{OH}

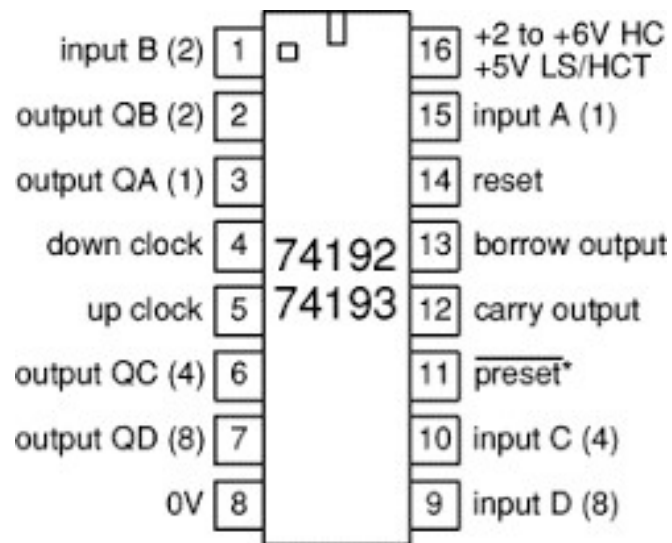


Fig2. Circuit diagram of 74HC192

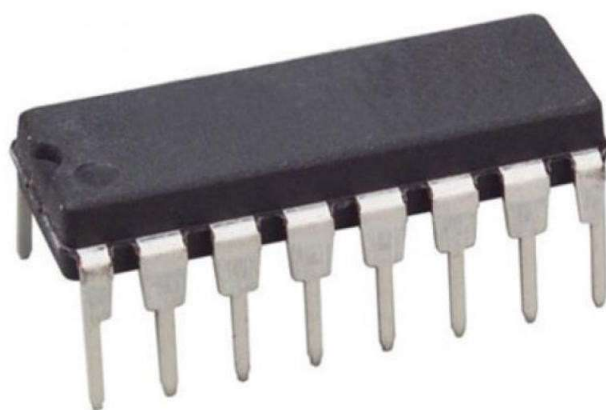


Fig3. 74HC192

PROTEUS SIMULATION

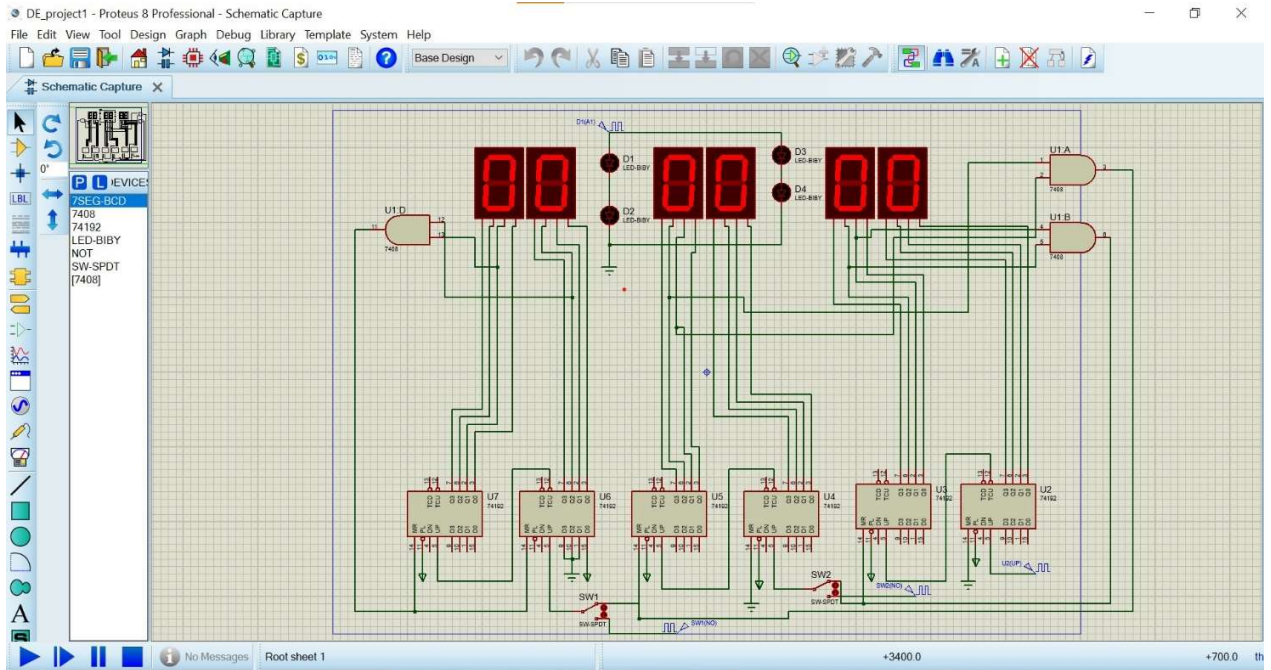


Fig4. Prototype of the Digital Clock using Proteus Software

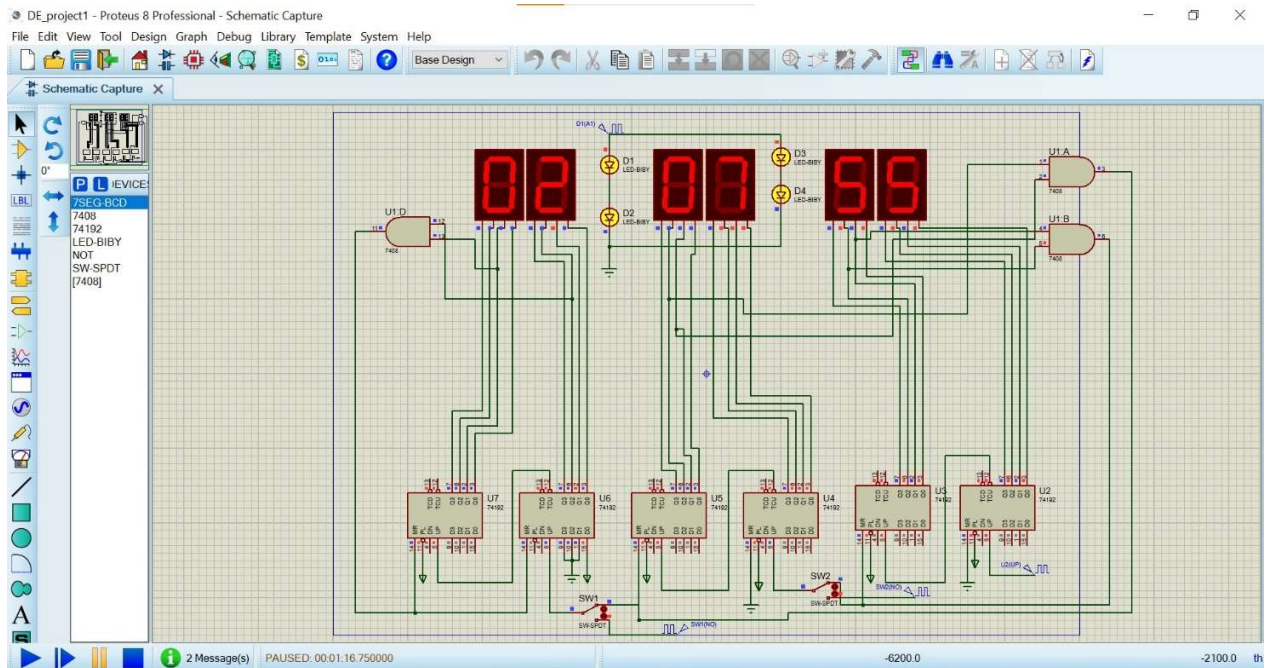


Fig5. Digital clock running.

WORKING PRINCIPLE

In order to obtain a better understanding, the working principle has to be divided into three distinct parts: The seconds block, the minutes block and the hours block.

A. The Seconds Block

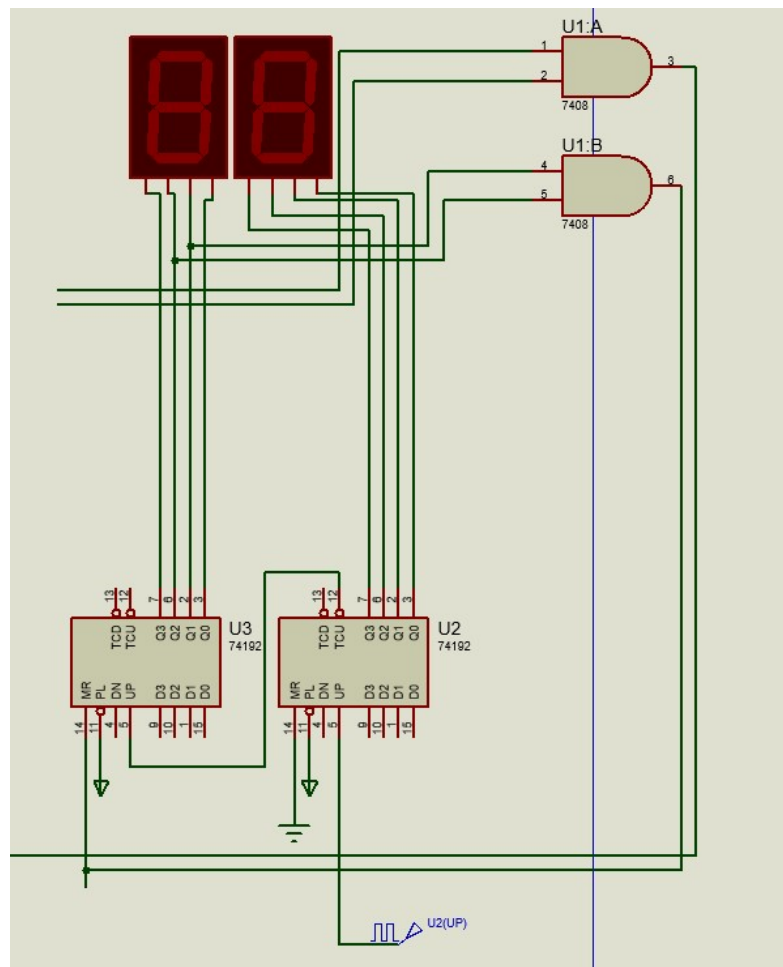


Fig 6: The seconds block of the circuit

It is through the seconds block, most precisely through the first counter, terminal 5, that the circuit receives its main clock pulse. The clock is a low-high-low type, and it has a frequency of 1Hz, in order to generate 1PPS (pulse per second).

After each pulse, a binary combination is generated by the first 74192 IC, resulting of the counting process, and this combination is displayed by the 7-segment display, by connecting the output terminals 7, 6, 2, and 3 (decreasing order of bits significance), to the terminals of the 7-segment display.

The seconds block is formed by a divide by 10 circuit, followed by a divide by 6 circuit. This will ensure that the seconds block counts and displays only up to 59 seconds.

When the first 74192 IC count reaches the binary value 1010, which is 10 in decimal, by “default”, it resets to 0 and through the terminal 12, which is the carry output, sends a pulse to the second 74192 IC, which is connected to the first by the terminal 5 (Up clock), in order to start the counting of it. This process is repeated up to a point when the first IC counts 1010 (10 in decimal), and the second one counts 0101 (5 in decimal).

In order to reset the counting and send a pulse to the minutes block, a logic condition must be formed: if the second IC reaches 0110 (6 in decimal), the seconds block resets and, through the terminal 12, sends a pulse to the minutes block. This logic decision is made by the use of an AND gate (U1: B in the circuit), whose output is connected to the terminal 14 (reset terminal) of the second IC.

B. The Minutes Block

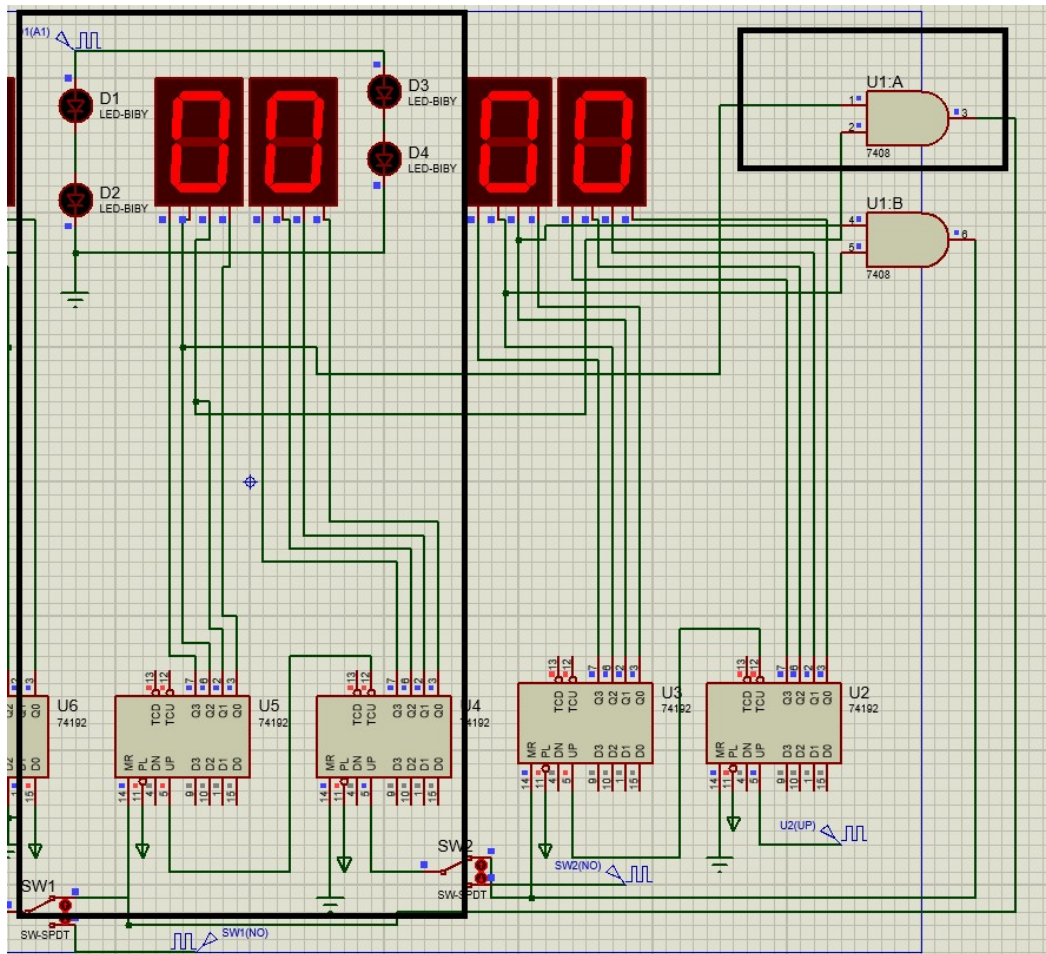


Figure 7: The seconds block of the circuit

The principle of the minutes block is pretty much the same as of the seconds' block, since both blocks consists of a divide by 10 circuit, followed by a divide by 6 circuit in order to ensure that they count and display only up to 59. The decision described in the last two paragraphs of the last subsection is done by the logic gate AND U1: A for the block of the minutes

The key differences are: The type of pulse received and the presence of a switch.

The minutes block receives an 1PPM (pulse per second) from the seconds block by connecting the output terminal of the AND gate U1: B to the up clock terminal (terminal 5) of the third IC. This 1PPM is the result of the reset of the whole seconds' block.

The presence of the switch is to allow to set the correct time in the minutes block, by allowing pulses of 1Hz frequency of a clock to go directly to it.

C. The hours block

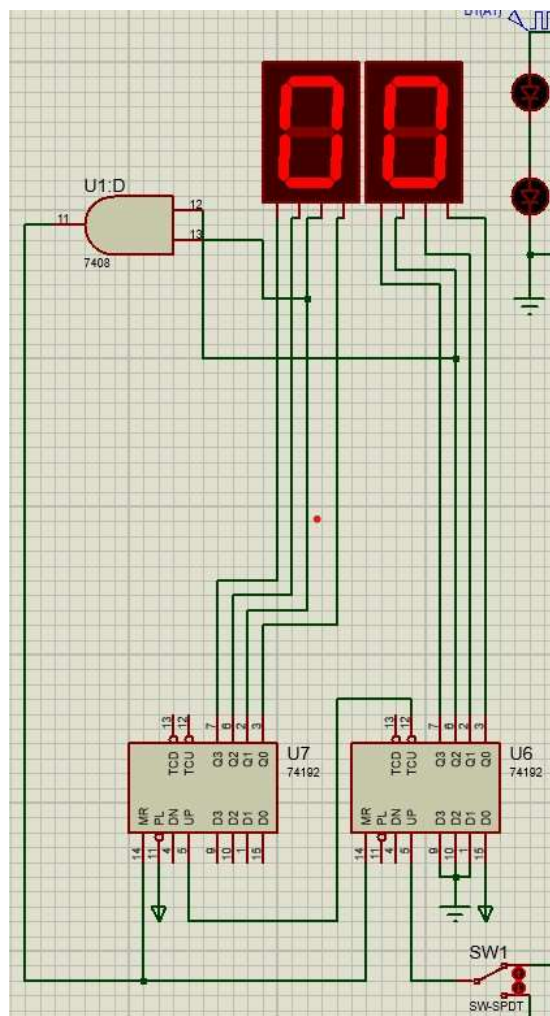


Figure 8: The seconds block of the circuit

The hours block working is different of the previous two presented. The hours block receives an 1PPH (pulse per hour) from the minutes block by connecting the output terminal of the AND gate U1: A to the up clock terminal (terminal 5) of the fourth IC. This 1PPH is the result of the reset of the whole minutes' block.

Since the circuit is for the design of a 24-hours digital clock, some restrictions have to be set to both ICs (namely the fifth and sixth). The hours block resets its counting counting when the fifth IC reaches 0100 (4 in decimal) and the sixth reaches 0010 (2 in decimal). In order to satisfy such condition, AND gates were used, the U1: C for the fifth IC, whose output is connected to the U1: D, the AND gate assigned to the sixth IC.

The output of U1:D is connected to the terminals 14 of both fifth and sixth ICs, in order to reset both the its output is 1.

Similarly to the minutes block, the hours block as a switch, and it as the same purpose of the one of the minutes' block: to allow to set the correct time.

ADVANTAGES OF DIGITAL CLOCK

1. Coordinated indications of all clocks at the site with a global universal time (UTC/GMT);
2. Synchronous indication of an exact zone time in the pointer and digital formats on all clocks;
3. Automatic conversion of clocks during the transition to winter/summer time;
4. Automatic setting of the clock to the exact time after restoration of power or liquidation of the accident on a line;
5. Automatic restoration of the correct indications of the clock at failures or during power interruption for a period of up to 1 week;
6. Synchronization of the computer network in accordance with the calendar date and exact time;
7. Simplicity of usage that does not require special training of the engineering personnel.

DISAVANTAGES OF THIS SYSTEM

1. Easy to misread (sometimes an 8 looks like a 0)
2. Very limited viewing angle
3. Only run on electricity
4. Lit screens can sometimes too bright enough to make it difficult to select

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