IC TESTER

Submitted by: Group 89

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Contents

User Requirements & Technical Specifications

Design a Microprocessor based Tester to test the logical functioning of the following chips:

1. 7400

2. 7408

3. 7432

4. 7486

5. 747266

The IC to be tested will be inserted in a 14 pin ZIF socket. The user places the IC in the ZIF socket, closes it – then enters the IC No, followed by the enter key.

The IC number is to be entered via a keyboard.

The keyboard has keys 0-9, backspace, enter and test.

The IC No. is displayed on the 7-segment display.

The testing will start once the user presses the test key.

After Test the result PASS/FAIL must be displayed on the 7-segment display.

Assumptions

- User presses enter key before test key
- No simultaneous keys are pressed. If so then they are ignored
- Switch (in the Proteus design) acts as a lever present in ZIF. Whenever the lever is open, the IC is not tested.

Components used with justification wherever required

- 8086
- 3x LS 373,2x LS 245,2x LS138 and required gates for buffers and latches
- 2x 8255 - 1 for display and keypad, another for ZIF
- 4x 2716 - Since this is the smallest available ROM. One is added at the start and another at the end. Since we have 2 banks (odd and even) thus we use 2 chips for each bank.
- 2x 6116 - This is the smallest available RAM chip. It is placed after the first ROM chip. 2 chips are used for odd and even banks respectively.
- 8284 - used for clock generation of 8086.
- 2:4 decoder- 74hc139 - used to decode between the 2 8255s
- 1x 7447 for BCD to 7 Segment decoding
- 6x 7-segment displays - as max number of digits is 6
- ZIF
- 13x Buttons for construction of keypad

Address Map

Memory Map

00000 - 00FFF - ROM1

01000 - 01FFF - RAM 1

FF000 - FFFFF - ROM2

I/O Map

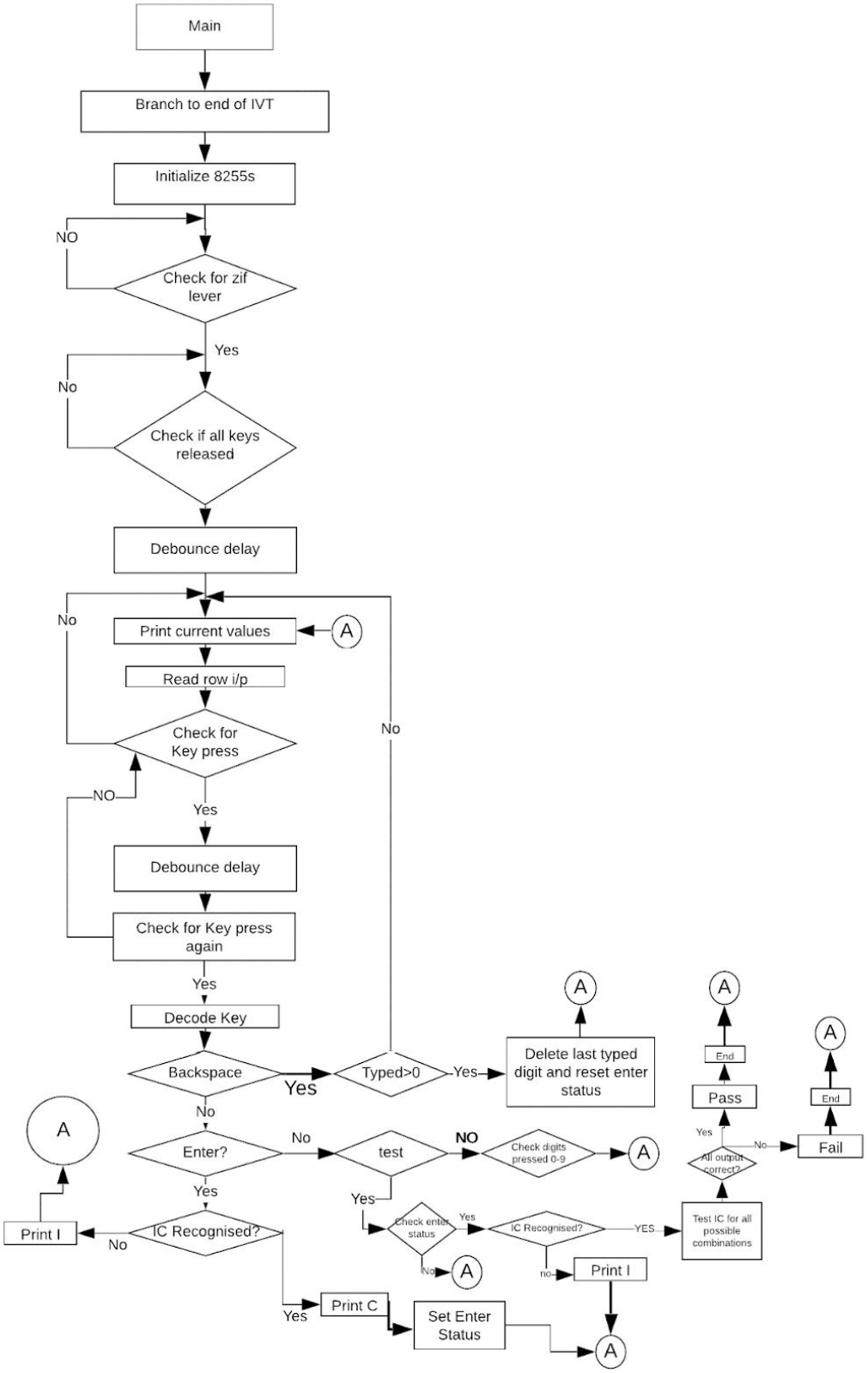
1st 8255 for display and keyboard
00 - port 1a
02 - port 1b
04 - port 1c
06 - Control register 1

2nd 8255 for keypad
10 - port 2a
12 - port 2b
14 - port 2c
16 - Control register 2

Design

Complete design shown with proper labelling (design attached)

Flow Chart


Main
Branch to end of IVT
Initialize 8255s
NO
Check for zif lever
Yes
No
Check if all keys released
Debounce delay
No
Print current values
A
Read row i/p
Check for Key press
No
NO
Yes
Debounce delay
Check for Key press again
Yes
Decode Key
Backspace
Yes
Typed>0
Yes
Delete last typed digit and reset enter status
A
No
Enter?
No
test
NO
Check digits pressed 0-9
A
Yes
Yes
Check enter status
Yes
IC Recognised?
YES
Test IC for all possible combinations
No
A
no
Print I
A
End
Pass
Yes
All output correct?
No
Fail
A
End
A
Print I
IC Recognised?
No
Yes
Print C
Set Enter Status
A

Variations in Proteus Implementation with Justification

- 2732 is used as 2716 is not available in proteus
- A built in module of 6 concatenated 7 segment displays which was available in Proteus is used.
- Built in clock generator was used instead of 8284
- ZIF is implemented using standard wires and terminals due to unavailability of a ZIF module in Proteus.

Firmware

- Implemented using emu8086 attached.

List of Attachments

1. Complete Hardware Real World Design – design.pdf
2. Manuals
    a. 7447
    b. 747266
    c. 7400
    d. 7408
    e. 7432
    f. 7 segment display
    g. 74HC139
    h. ZIF
3. Proteus File – ic_tester.dsn
4. EMU8086 ASM File – ic_tester.asm
5. Binary File after assembly – ic_tester.bin