Research Challenges in Supervisory Control Theory

Michel Reniers
Eindhoven University of Technology
M.A.Reniers@tue.nl

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1 Introduction

In the era of Cyber-Physical Systems (of Systems) and the Internet of Things, much effort goes into the development of supervisory controllers that need to provide a safe (and efficient) coordination of subsystems.

One of the approaches that has been researched in the past decades is *supervisory control theory* [9], where based on a model of the uncontrolled system and a model of the (safety) requirements, a model of the supervisory controller is generated such that the controlled system (i.e., the uncontrolled system under the control of the supervisory controller) is (1) controllable, (2) safe w.r.t. the requirements, and (3) nonblocking. Traditionally, SCT works with so-called discrete-event systems, typically in the form of (extended) finite automata [3, 12].

In this short position paper, research challenges that are currently worked on and for which progress is expected / needed in the near future are described. This is not intended to be an overview of all the activities that take place in the field, but merely presents the authors current view on some interesting ones.

2 Core challenges in SCT

Challenges in the area of supervisory control synthesis, in no particular order, are

1. development of a *discipline of modelling* that facilitates use of the model-based engineering approach towards supervisory control synthesis;
2. scalability of supervisory controller synthesis;
3. expressivity of requirements;
4. development of synthesis techniques for networked supervisors, i.e., supervisors that are connected with the uncontrolled system by means of a network with its inherent communication characteristics (e.g., communication delays and losses);
5. integration of performance optimization techniques and supervisory controller synthesis.

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2.1 A discipline of modelling for SCT

Inspired by experiences from application of supervisory control synthesis to relevant cases such as manufacturing systems [15], automotive systems [7], and waterway locks [11], recent (unpublished) research attempts to provide a set of sufficient conditions on models of uncontrolled system and requirements that provide a trivial controllable system without blocking.

Of course there are also relevant systems for which these conditions do not hold, and it is important to establish heuristics for modelling such systems that on the one hand allow application of supervisory controller synthesis, and on the other hand make the modelling effort itself manageable in terms of compositionallity and evolvability.

It is our ambition to formulate a discipline of modelling that allows practical and efficient application of supervisory control synthesis.

2.2 Scalability of supervisory controller synthesis

Scalability issues with monolithic synthesis algorithms have led to the study of techniques that decompose the synthesis problem into a number of smaller synthesis problems from the solution of which a supervisor can be obtained. Most of these techniques require a creative/manual effort to decide the decomposition of the system.

In recent research, Design Structure Matrices and clustering techniques are used to obtain a decomposition automatically [5]. Still much research is needed to provide guarantees for the supervisor obtained by composing the supervisors for the subproblems as in general nonblockingness and maximal permissiveness are sacrificed in such an approach.

Ideas for a form of compositional synthesis (involving intermediate abstractions and synthesis steps) are emerging in literature [4] and are actively researched by research groups involved with the tool sets Supremica [1] and CIF [2].

Adaptation of the well-known partial-order reduction techniques from model checking for use in the domain of supervisory control theory are studied in [14]. Such reductions need to preserve properties such as controllability and nonblocking, which are not standard in model checking in general.

2.3 Expressivity of requirements

Traditional synthesis is restricted to requirements specified by (extended) finite automata and state-based expressions. In

recent years there have been some attempts to generalize the synthesis to requirements in fragments of temporal logics such as LTL and modal μ-calculus (see, e.g., [6]), but still much more expressivity is needed to capture meaningful behavioural requirements.

For (mechanical and control) engineers, capturing informal requirements in formal models is more than a challenge, and much better support is needed in formulating such properties. Candidates are formulation of properties in terms of scenarios-based formalisms such as life sequence charts. Validation of complex requirements is hardly supported by tool sets in the domain of supervisory control.

2.4 Synthesis of networked supervisors

A basic assumption in the supervisory control theory framework is that the supervisor and uncontrolled system interact synchronously. Practical applications require to relax this assumption since mostly there is some communication medium between supervisory controller and (parts of) the uncontrolled system. Such communication media introduce asynchronicity between plant and supervisor and may result in overtaking of messages and even message losses. Under such conditions obtaining a safe and nonblocking supervisory control becomes more challenging, obviously. Initial work is reported (see [10], and references therein), but both conceptually as well as in terms of applicability many improvements are still expected and required before such theories may become usable.

2.5 Synthesis of performance-optimal supervisors

It would be interesting and practically relevant if we could combine techniques for obtaining a supervisor that provides functional properties of the system and techniques for obtaining a supervisor that adheres to some performance properties, such as a guaranteed throughput. For fully controllable systems, promising first results have been developed in [13], and for partially controllable systems, initial work is given in [8].

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