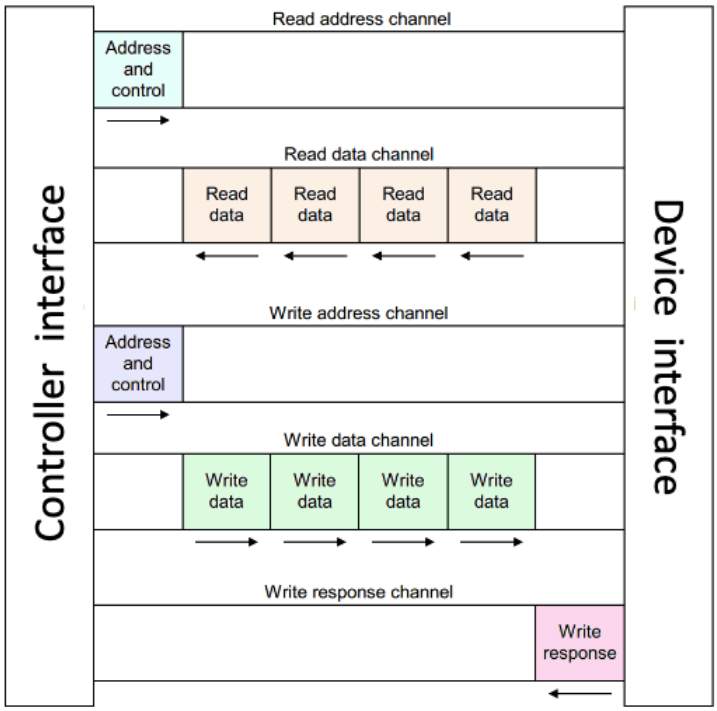
AMBA (Advanced Microcontroller Bus Arch)

- Consists of 3 bus protocols
  - **AXI** (Advanced eXtensible Interface)
    - Connects high-speed components such as OoO CPUs and DRAM memory
  - **Advanced High-performance Bus** (AHB)
    - Connects lower speed *(in-order)* CPUs and SRAM memory
  - **APB** (Advanced Peripheral Bus)
    - Connects slow peripherals such as UART, Timer, GPIOs with microcontroller

AXI

- AXI separates different tasks into 5 channels
  - Each task can happen independently. Burst wrtes doesn't affect slow reads.
  - Simple bus support only 1/2 channels
- AXI supports multiple **outstanding** transactions
  - A controller can have multiple requests pending at the same time
    - multiple addresses being read from memory



AMBA Channels

APB / AHB : Two channels

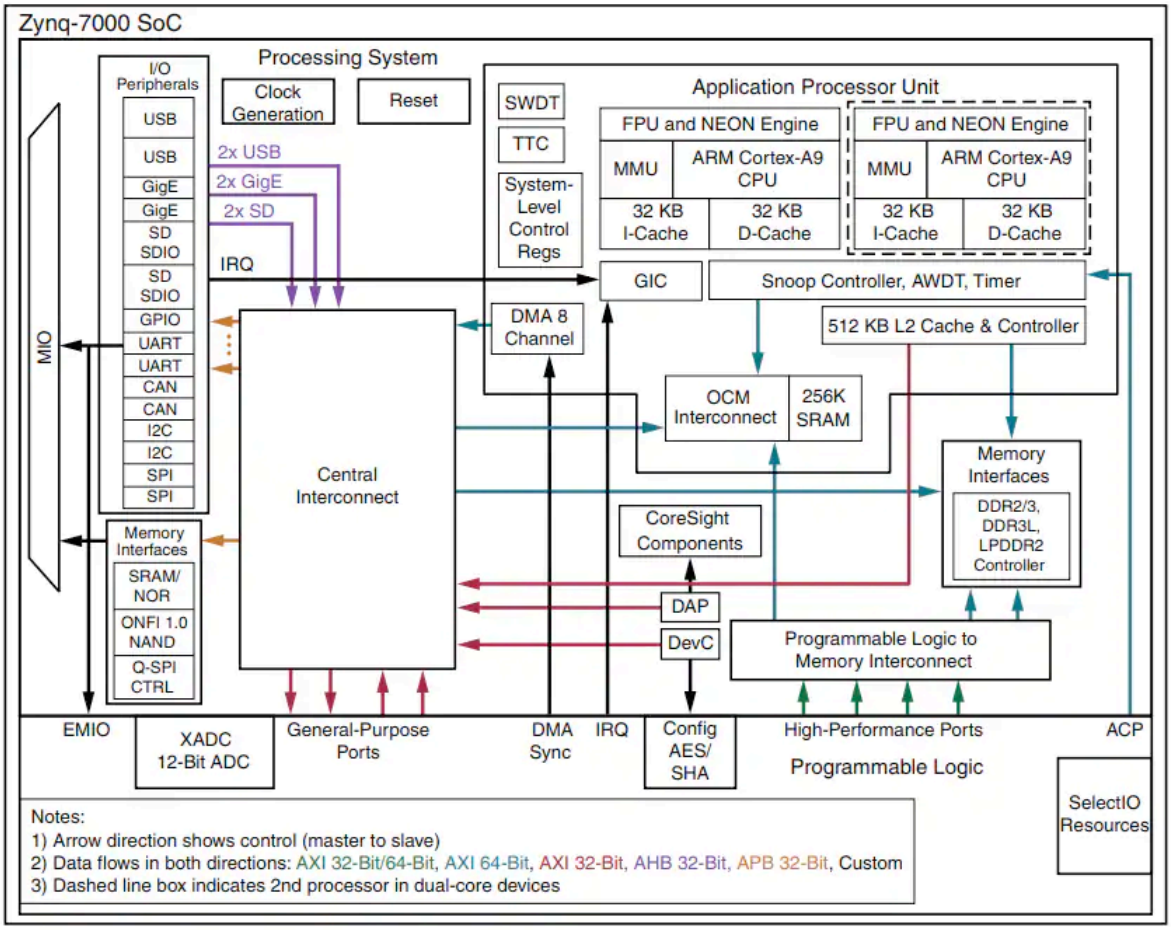
- APB:
  - Address
  - Data
- AHB:
  - Address/Data
  - Control
- Half-duplex (can only read or write at a time, but not both)

AXI: Five channels

- Write Address channel
- Write Data channel
- Write Response channel
- Read Address channel
- Read Data channel
- Full duplex (can read and write at the same time)

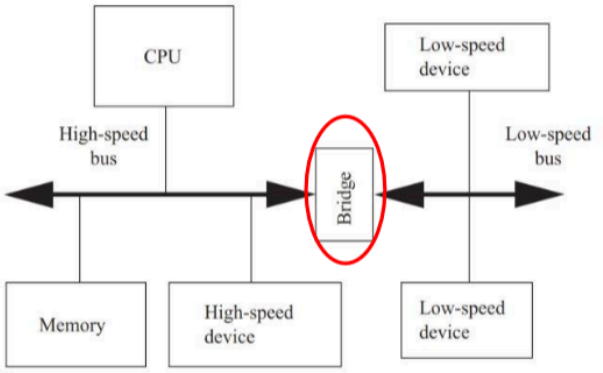
AXI vs. AHB vs. APB

Feature	AXI	AHB	APB
Data Width	32, 64, 128, or more bits	32 or 64 bits	Typically, 8, 16, or 32 bits
Data Transfer	Burst or single transfers	Burst or single transfers	Single transfers
Operation	Full duplex	Half duplex	Half duplex
Throughput	Very high	High	Low
Complexity	Complex	Moderate	Simple
Latency	Low latency	Medium latency	Higher latency
Efficiency	High	Moderate	Low
Power Consumption	High	Moderate	Very low
Controller support	Multiple controllers	Single controller	Single controller

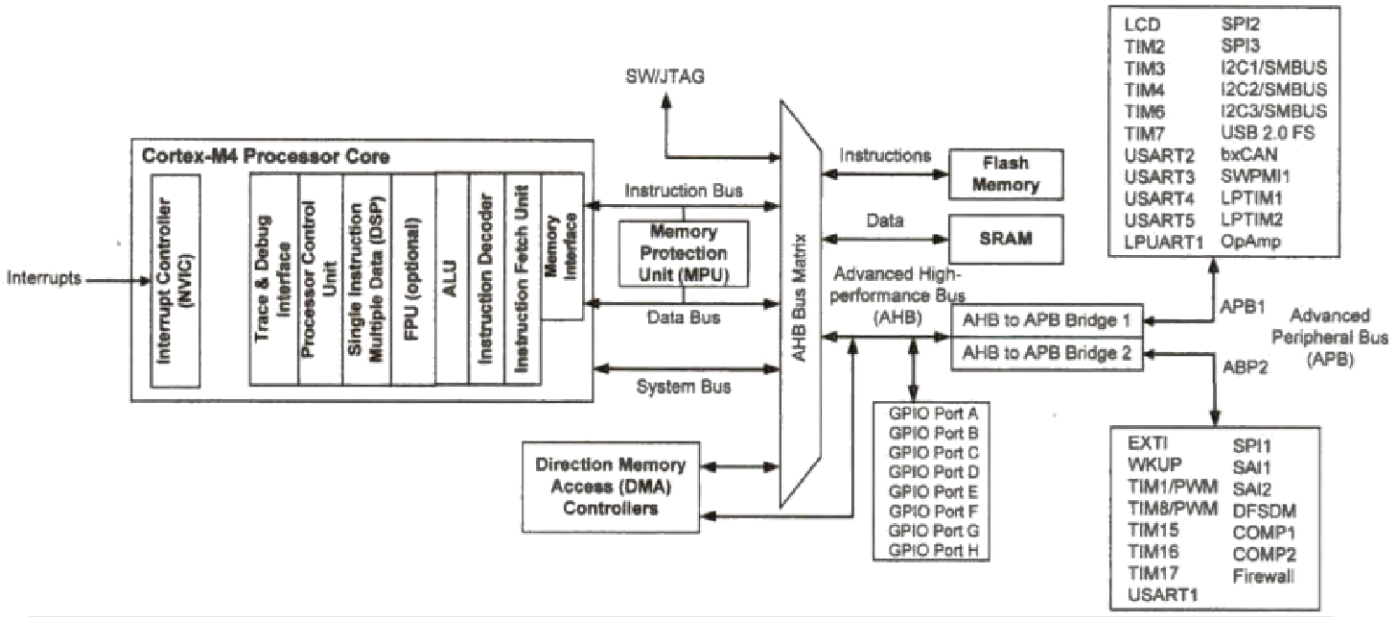


Multiple Buses

- Systems have different buses operating at **different speeds**, connecting different modules
- Need a bus interface/bridge to move data between them
- High speed dev connected to high performance bus; low speed dev to different bus



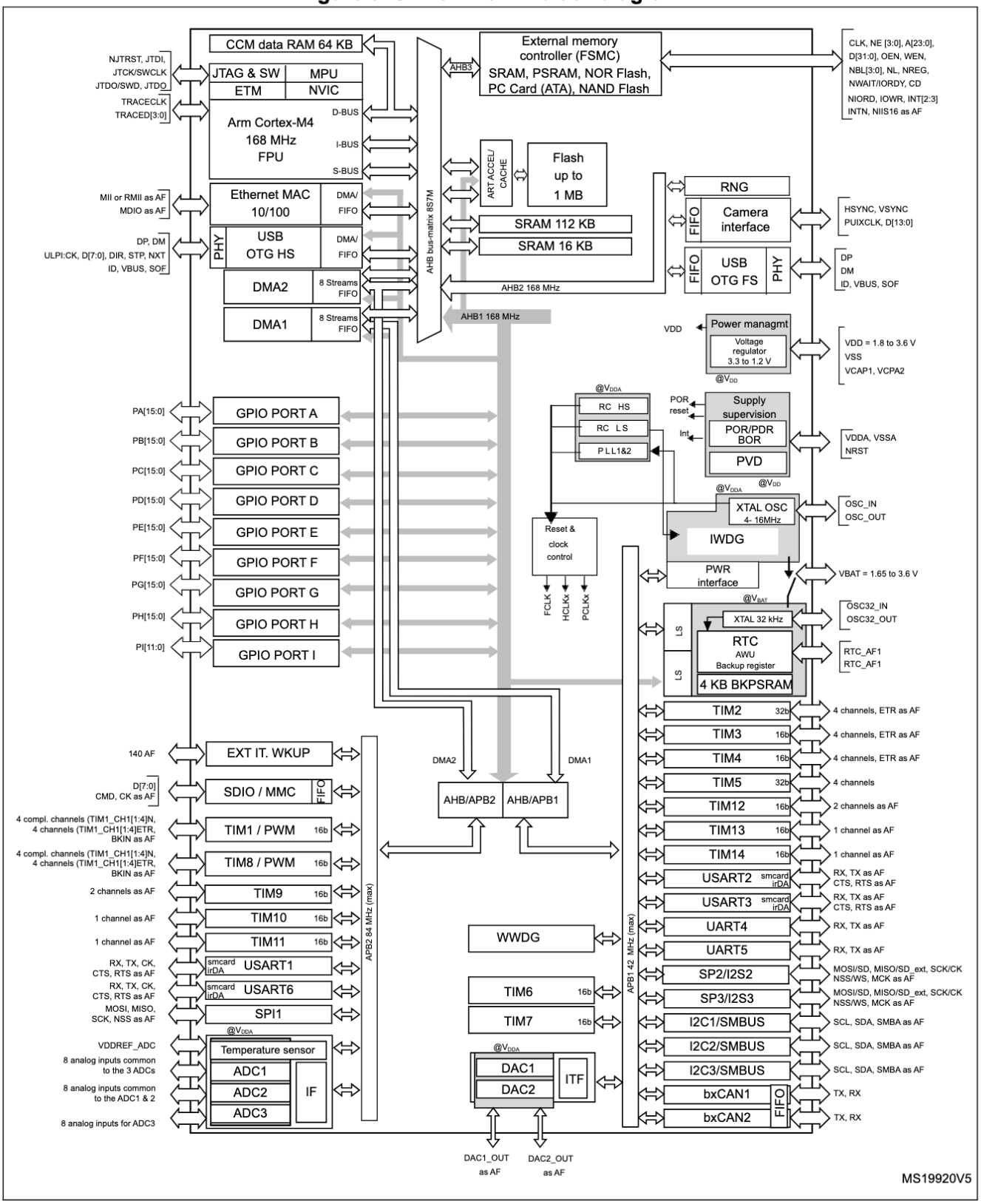
ARM Cortex M4



STM32 - F4x Devices

2 *AHB; 2* APB buses

Figure 5. STM32F40xxx block diagram



1. The camera interface and ethernet are available only on STM32F407xx devices.

Why Multiple Buses

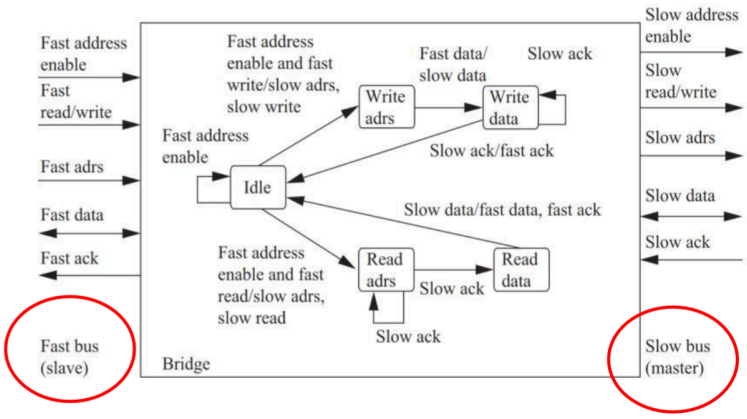
- More efficient use of the bigger bus
  - pack operations to and from multiple slow dev over a single operation of the large bus
- Simpler protocol for peripherals
  - Connecting UART or timer over AXI adds a lot of complexity for no benefit

- Simpler address decoding logic
  - Address decoder for the AHB bus can treat all APB peripherals as a single dev

Bus Interface (Bridge)

Bridge is the logic that connects between buses

- A state machine or dedicated processor
- Also allows buses to operate independently
  - I/O operations may be done in parallel



Not always but, bridge is a device of the fast bus and controller of the slow bus.

- Takes commands from the fast bus
- Issues those commands to the slow bus, then returns the results from the slow bus to the fast bus
- It also serves as a protocol translator

Some components can be either Controller or Device at a time (hybrid)

- Example: a memory controller is a Device when being configured, but is a Controller when writing blocks to memory

Multiple buses on bigger systems