Clocks

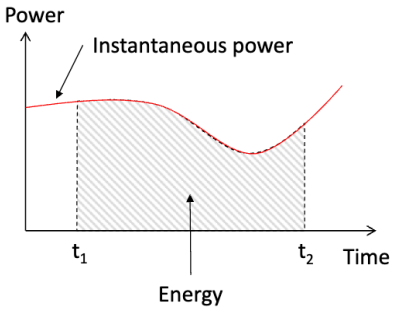
- crystal oscillators
  - only produces a single frequency
- **phase-locked loops (PLL)** produce clocks of different frequencies

Clock Domains

- every system has multiple clocks
  - different things run at different speeds
  - each interface needs a different clock
- F446ZE has 4 PLLs
  - check clock config tab in STMCube

Power VS Energy

- Energy = Power x Time
  - instantaneous power
  - power changes overtime



Static Power

- power from transistor leakage
- even when gate voltage < threshold voltage, some current leaks through
- constant and determined by the transistor's physical properties

Dynamic Power

- power from **switching** (transistors turning on / off)

$$dynamic\ power = \alpha \cdot (V_{dd})^2 \cdot C_L \cdot f$$

- f clock frequency
- V_{dd} Supply voltage
- C_L total capacitance of circuit
- α switching factor

Switching factor a

- a is percentage of the clock switching
  - the clock's α is always 100% (1.0)
  - if signal switches on every rising edge, $\alpha = 0.5$
- accurate a needs circuit simulation
  - common to use a nominal value of $\alpha = 0.1$ or 10%

Capacitive Load

- measure how 'big' circuit is
  - larger circuit, more charge needed
- α and C_L are independent of code, determined by **hardware** itself

Frequency

- has control over
- power increases proportional to frequency
  - Current = 244 μA per MHz (at max voltage)
- equation includes alpha and CL

Voltage

- power increases exponentially with voltage
  - increase voltage to get higher frequency
  - higher V allows higher I, which loads capacitance faster (higher f)
- If circuit running at max frequency for a given Vdd, increasing frequency can significantly increase power
  - needs a higher Vdd to support higher freq
  - power increases due to both higher Vdd and higher freq

Voltage VS Frequency

- higher freq $\neq$ higher V
  - not simple linear relationship
- voltage only determines **maximum possible frequency** F_max
  - at a given voltage, you can run at a lower frequency than F_max

Illustrative table of frequencies supported at different voltages.

	100 MHz	150MHz	200 MHz	250MHz
1.0V	✓	✗	✗	✗
1.2V	✓	✓	✗	✗
1.4V	✓	✓	✓	✗
1.6V	✓	✓	✓	✓

A circuit runs at 100MHz @ 1.8V. You want to run this circuit at 250MHz, which requires a voltage of 3.3V. How much more dynamic power is consumed at 250MHz compared to 100MHz?

$$dynamic\ power = \alpha \cdot (V_{dd})^2 \cdot C_L \cdot f$$

$$dynamic\ power_{100} = \alpha \cdot (1.8)^2 \cdot C_L \cdot 100MHz = (324 \times 10^6) \cdot \alpha C_L$$

$$dynamic\ power_{250} = \alpha \cdot (3.3)^2 \cdot C_L \cdot 250MHz = (2722.5 \times 10^6) \cdot \alpha C_L$$

$$Increase = \frac{dynamic\ power_{250}}{dynamic\ power_{100}} = \frac{2722.5}{324} = 8.4$$

Techniques to Reduce Power

- controlling freq and voltage
  - reduce freq
    - lower freq of blocks when not needed
    - lower CPU freq when inside a delay function
  - power gating
    - turn off power to parts of the chip
    - reduces static (leakage) power