PROIECT CID

Bistabile D (mux 4:1, mux 2:1)
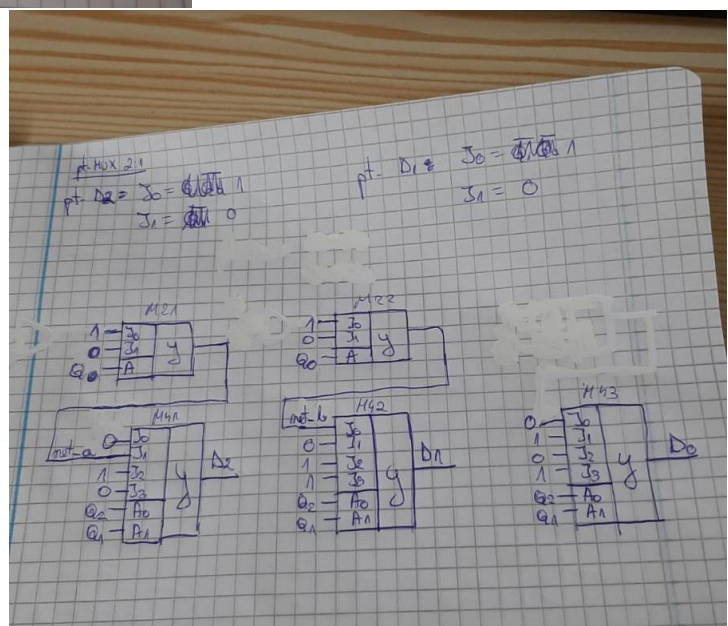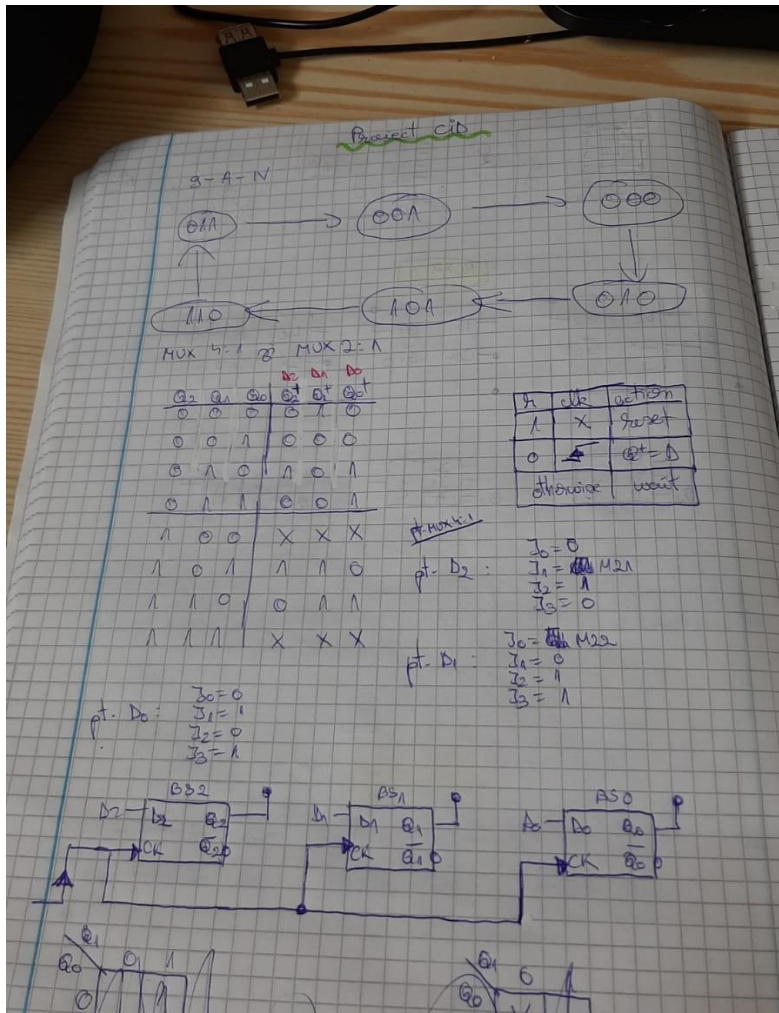
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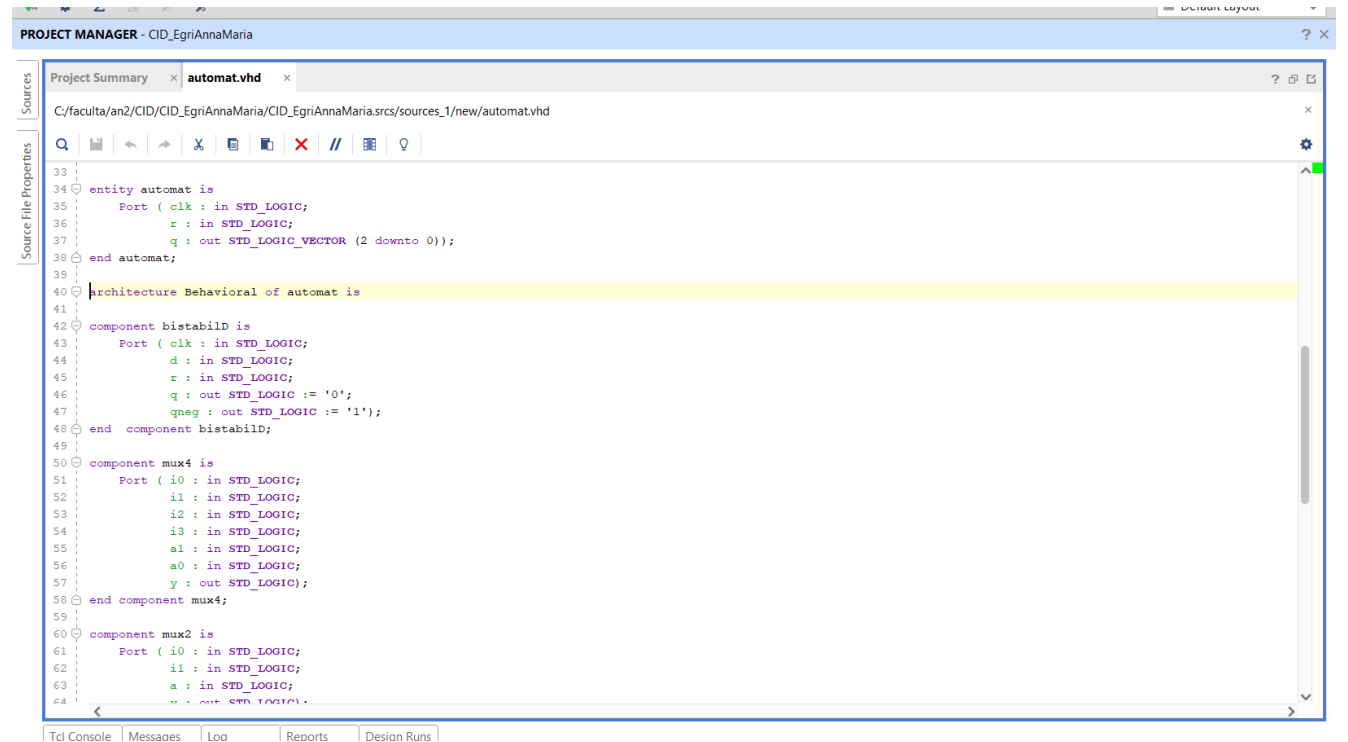
CUPRINS

1.Proiectul rezolvat pe hartie

2.Cod automat si simulare

Project Summary | automat.vhd

C:/faculta/an2/CID/CID_EgriAnnaMaria/CID_EgriAnnaMaria.srcs/sources_1/new/automat.vhd
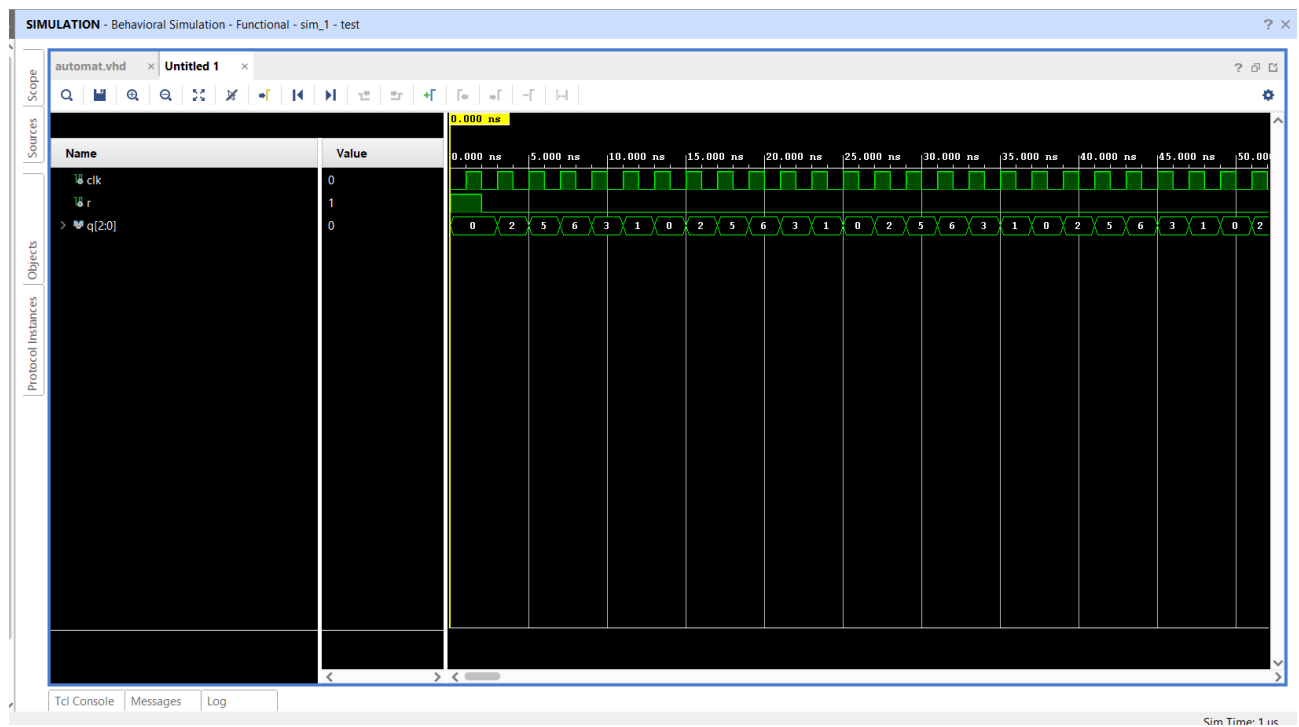
```vhdl
33
34  entity automat is
35      Port ( clk : in STD_LOGIC;
36              r : in STD_LOGIC;
37              q : out STD_LOGIC_VECTOR (2 downto 0));
38  end automat;
39
40  architecture Behavioral of automat is
41
42  component bistabilD is
43      Port ( clk : in STD_LOGIC;
44              d : in STD_LOGIC;
45              r : in STD_LOGIC;
46              q : out STD_LOGIC := '0';
47              qneg : out STD_LOGIC := '1');
48  end  component bistabilD;
49
50  component mux4 is
51      Port ( i0 : in STD_LOGIC;
52              i1 : in STD_LOGIC;
53              i2 : in STD_LOGIC;
54              i3 : in STD_LOGIC;
55              a1 : in STD_LOGIC;
56              a0 : in STD_LOGIC;
57              y : out STD_LOGIC);
58  end component mux4;
59
60  component mux2 is
61      Port ( i0 : in STD_LOGIC;
62              i1 : in STD_LOGIC;
63              a : in STD_LOGIC;
64              y : out STD_LOGIC);
```

Tcl Console | Messages | Log | Reports | Design Runs

PROJECT MANAGER - CID_EgriAnnaMaria

Project Summary | automat.vhd

C:/faculta/an2/CID/CID_EgriAnnaMaria/CID_EgriAnnaMaria.srcs/sources_1/new/automat.vhd

```vhdl
66
67  signal D0, D1, D2, net_a, net_b:std_logic;
68  signal qint: std_logic_vector(2 downto 0);
69
70  begin
71
72  q<=qint;
73
74  B2: bistabilD port map(clk=>clk,
75  r => r,
76  d=>D2,
77  q=>qint(2)
78  );
79
80  B1: bistabilD port map(clk=>clk,
81  r => r,
82  d=>D1,
83  q=>qint(1)
84  );
85
86  B0: bistabilD port map(clk=>clk,
87  r => r,
88  d=>D0,
89  q=>qint(0)
90  );
91
92  M41: mux4 port map (i0=> '0', i1=>net_a, i2=>'1', i3=>'0', a1=> qint(2), a0=>qint(1), y=>D2);
93  M42: mux4 port map (i0=> net_b, i1=>'0', i2=> '1', i3=>'1', a1=> qint(2), a0=>qint(1), y=>D1);
94  M43: mux4 port map (i0=> '0', i1=>'1', i2=> '0', i3=>'1', a1=> qint(2), a0=>qint(1), y=>D0);
95  M21: mux2 port map (i0=> '1', i1=> '0', a=>qint(0), y=> net_a);
96  M22: mux2 port map (i0=> '1', i1=> '0', a=>qint(0), y=> net_b);
97
```

Tcl Console | Messages | Log | Reports | Design Runs

40:1   Insert   VHDL

3.Cod bistabil D si simulare


```vhdl
--use UNISIM.VComponents.all;

entity bistabilD is
    Port ( clk : in STD_LOGIC;
           d : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC := '0';
           qneg : out STD_LOGIC := '1');
end bistabilD;

architecture Behavioral of bistabilD is

signal qaux: std_logic;

begin
q <= qaux;
qneg <= not qaux;
process(r, clk)
begin
    if r = '1' then
        qaux <= '0';
    elsif rising_edge (clk) then
        qaux <= d;
    else
        qaux <= qaux;
    end if;
end process;

end Behavioral;
```
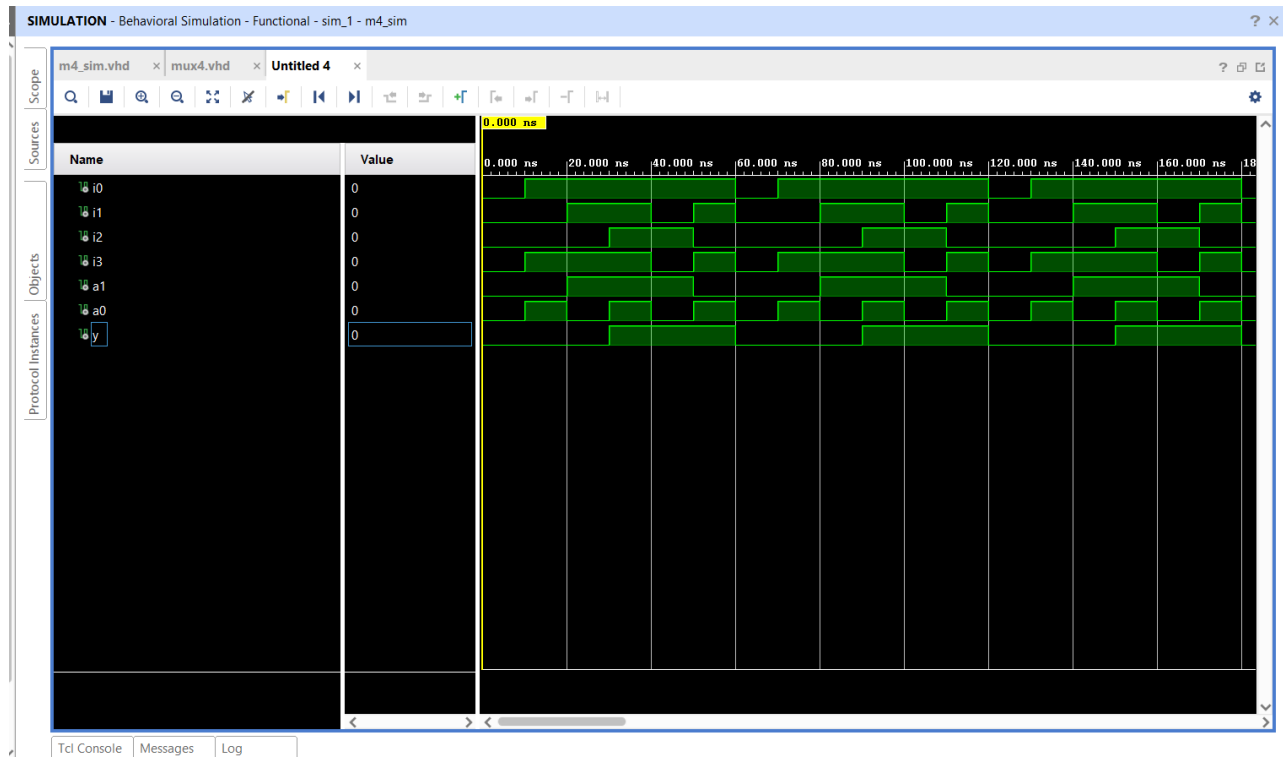
4.Cod MUX 4:1 si simulare


```vhdl
29    -- Uncomment the following library declaration if instantiating
30    -- any Xilinx leaf cells in this code.
31    --library UNISIM;
32    --use UNISIM.VComponents.all;
33
34    entity mux4 is
35        Port ( i0 : in STD_LOGIC;
36               i1 : in STD_LOGIC;
37               i2 : in STD_LOGIC;
38               i3 : in STD_LOGIC;
39               a1 : in STD_LOGIC;
40               a0 : in STD_LOGIC;
41               y : out STD_LOGIC);
42    end mux4;
43
44    architecture Behavioral of mux4 is
45
46    signal adr:std_logic_vector(1 downto 0);
47
48    begin
49
50    adr <= a1 & a0;
51
52    with adr select
53        y <= i0 when "00",
54             i1 when "01",
55             i2 when "10",
56             i3 when "11",
57             i0 when others;
58
59      end Behavioral;
```

5.Cod MUX 2:1 si simulare


```vhdl
18   --
19   ----------------------------------------------------------------------------------
20
21
22   library IEEE;
23   use IEEE.STD_LOGIC_1164.ALL;
24
25   -- Uncomment the following library declaration if using
26   -- arithmetic functions with Signed or Unsigned values
27   --use IEEE.NUMERIC_STD.ALL;
28
29   -- Uncomment the following library declaration if instantiating
30   -- any Xilinx leaf cells in this code.
31   --library UNISIM;
32   --use UNISIM.VComponents.all;
33
34   entity mux2 is
35       Port ( i0 : in STD_LOGIC;
36              i1 : in STD_LOGIC;
37              a : in STD_LOGIC;
38              y : out STD_LOGIC);
39   end mux2;
40
41   architecture Behavioral of mux2 is
42
43   begin
44
45   y <= i1 when a='1' else i0;
46
47   end Behavioral;
48
```