UWE FASSNACHT

Tuebingen,Germany uwefassnacht@gmail.com

PROFILE AND CORE COMPETENCIES

Results-oriented, decisive and energetic technical leader with international experience. Skilled in product management and evangelizing through teamwork, strategic thinking and tactical execution.

- Innovative technical leadership
- Client relationship and customer facing skills
- Bilingual (English and German) with excellent presentation skills
- Collaborating and communicating across organizational structures and geographic boundaries
- Bridging the gap between R&D and the customer through demos, prototypes and proof-of-concepts

PROFESSIONAL EXPERIENCE

IBM - R&D LAB BOEBLINGEN, GERMANY **04/2014 - PRESENT**
PRODUCT MANAGER & DEVELOPER ADVOCATE FOR IBM BLUEMIX

Responsible for presenting and positioning the Bluemix cloud platform both within IBM and in front of enterprise customers, partners, developers, analysts and the press. Specifically focussed on demoing, defining and architecting innovative Internet of Things (IoT) solutions.

Enabling the world wide IBM sales & architecture teams, as well as working directly with clients to define early engagements and proof-of-concepts. Collecting customer feedback and driving requirements back into the international development teams.

Representing Bluemix at conferences, trade-shows, and developer events with a world wide team of developer advocates. Defining, planning and supporting hackathons to drive adoption in the developer ecosystem as well as among corporate clients.

Very familiar and comfortable with presenting at both the higher management and the developer level.

IBM - R&D LAB BOEBLINGEN, GERMANY **12/2010 - 04/2014**
TECHNICAL SOLUTION MANAGER FOR THE IBM MIGRATION FACTORY

Responsible for the complete sales cycle (opportunity identification and qualification, assessment, solution assembly, proof of concept, final customer commitment) of application migration services from competitive platforms to IBM server and cloud offerings. Orchestrated complex migration solutions by assembling teams across various IBM organizations and brands, as well as business partners.

Led an international team of architects and covering Europe, the Middle East and Africa. Since 2010, sold 8 M$ in migration services and influenced hardware sales of over 600 M$.

Acted as the lab advocate for several key clients (Vodafone, Evry, …) and fed their issues back into the IBM R&D teams.

IBM - MOUNTAIN VIEW, CA, USA **1/2004 - 12/2010**
ENGINEERING SERVICES TECHNICAL SALES LEAD

Coordinated teams in IBM research, development and sales to define, staff, start and run proof-of-concepts, resulting in 15M$ of software licensing contracts.

Responsible for presenting detailed technical proposals to a variety of clients across all geographies worldwide (Google, Cisco, Qualcomm, Texas Instruments, General Dynamics, Nokia, Ericsson, VIA, AMD, MediaTek, OKI, S3 Graphics, Huawei, …).

IBM - SANTA CLARA, CA, USA **1/2003 - 1/2004**
ONSITE DESIGN METHODOLOGY CONSULTANT AT NVIDIA

Based onsite at nVIDIA as a methodology consultant in the customers R&D team.

Involved in the design, verification and performance optimization of three graphic processors that were successfully manufactured by IBM. Enhanced nVIDIA's design methodology and software in the areas of DFM, timing analysis and layout optimization, which resulted in a $4M tool licensing contract for IBM.

Promoted to Senior Technical Staff Member

IBM - R&D LABS IN GERMANY (BOEBLINGEN) AND USA (NY AND VT) **10/1990 - 1/2003**
DESIGN ENGINEER AND CLIENT ENGAGEMENT MANAGER

Took a major part in defining and establishing the ASIC layout methodology of IBM and successfully taped out several demanding chips from various clients. Coordinated between customers, world-wide ASIC design teams and the electronic design automation (EDA) development group to quickly and efficiently improve timing and layout optimization software.

Cooperated closely with the Research Institute for Discrete Mathematics at the University of Bonn to further integrate advanced mathematical algorithms into the IBM design automation tool set.

Consulted and guided ASIC clients (e.g. Siemens, Alcatel, Cisco, Ericsson, Nokia, EZchip, ... in the development and implementation of successful and efficient timing methodologies for their ASIC designs. Spent substantial time onsite, working directly with clients development and management teams.

EDUCATION

Graduated with a BS in Electrical Engineering from the Berufsakademie Stuttgart, Germany in 1989

TECHNICAL SKILLS

Frameworks, Platforms and Cloud Services: Bluemix, SoftLayer, Cloud Foundry, IBM Watson, …

Operating Systems: Linux, AIX Unix, MS Windows, Mac OS X and iOS

Programming: node.js, Perl, shell scripting, awk, sed, C, JavaScript, git, express, MongoDB, Cloudant, …

PUBLICATIONS

"Timing Analysis and Optimization of a High-Performance CMOS Processor Chipset" at the Design, Automation and Test Conference (DATE) in 1998.

"A Robust ASIC Design and IP Integration Methodology for 65nm and Beyond" at ICCAD in 2004

"Practical Clock Skew Scheduling on a high performance Processor" at DesignCon in 2007

"Unifiying Transistor- and Gate-Level Timing through the Use of Abstraction" at Design Automation Conference in 2009

PATENTS

Patent No. DE9-2004-0016 "Regular Routing for Deep Sub-micron Chip Design"

Patent No. DE9-2008-0177-US1 "WiFi Locations using optical Indications on the screen of a mobile Device"

Patent No. DE9-2011-0026-US1 "Post Timing Layout Modification for Performance"