**ECE-111 Advanced Digital Design Projects**

**Homework-2a:**

**Convert 1-bit ALU to 4-bit ALU and change ALU module instantiation in ALU top module from explicit name port connection to dot-star port connection**

* Port name of module alu in alu.sv can be changed when converting explicit name port connection to dot-star port connection for alu instantiation in module alu\_top.sv
* Synthesize alu\_top and alu module
* Using provided alu testbench, run simulation for dot-star based alu instantiation in alu\_top
* Review synthesis results (FPGA resource usage and RTL netlist/schematic)
* Review input and output signals in simulation waveform

**Homework Submission :**

**Submit report (PDF file) which should include :**

* alu\_top, alu SystemVerilog design and testbench code
* Explain changes done in SystemVerilog code to change it from explicit name based port connections to dot-start based port connections for alu instantiation
* Explain changes done in SystemVerilog code to convert 1-bit ALU to 4-bit ALU
* Review post-Synthesis FPGA resource usage and schematic generated from RTL netlist viewer
* Simulation snapshot and explain simulation result

**Note :**

Lab2.zip folder has **alu\_top.sv, alu.sv and alu\_top\_testbench.sv** which should be used as a starting point for Homework-2a.

**Homework-2b:**

**Synthesis and Simulate 4-bit counter SystemVerilog Code**

* Review synthesis results (resource usage and RTL netlist/schematic)
* Run simulation using counter testbench code
* Review counter input output signals in simulation waveform

**Homework Submission :**

**Submit report (PDF file) which should include :**

* Counter SystemVerilog and testbench code
* Post synthesis FPGA resource usage and schematic generated from RTL netlist viewer
* Simulation snapshot and explain simulation result

**Note :**

Lab2.zip folder has **counter\_4bit.sv and counter\_4bit\_testbench.sv** which should be used for Homework-2b.