**ECE-111 Advanced Digital Design Projects**

**Homework-3:**

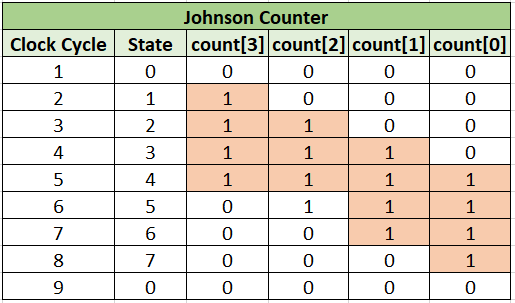
**Develop SystemVerilog RTL model for 4-bit Johnson Counter and perform following mentioned :**

* Synthesize Johnson counter
* Run simulation using Johnson counter testbench provided
* Review synthesis results (resource usage and RTL netlist/schematic)
  + Note : Explanation of resource usage in report is not mandatory to provide.
* Review input and output signals in simulation waveform.

**About Johnson Counter :**

* Similar to Straight Ring counter with below mentioned difference
* Johnson counter connects the complement of the output of the last shift register to the input of the first register and circulates a stream of ones followed by zeros around the ring
* Johnson Counter has 2N states (if N is 4, then total states for counting is 8. And 4-bit pattern will repeat after 8 cycles).

**4-bit Johnson Counter with initial load count value = 4’b0000**

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**4-bit pattern repeats every 8 cycles**

**Homework Submission :**

**Submit report (PDF file) which should include:**

* Snippet of SystemVerilog design code
* RTL netlist viewer schematic and Synthesis resource usage
  + Optional: Resource usage explanation and post mapping schematic
* Simulation snapshot and explain simulation result to confirm it works as a Johnson counter

**Note:**

* When creating RTL model for Johnson Counter, name SystemVerilog Module name as : **johnson\_counter**
* **Assume below mentioned Primary Ports for Johnson Counter**
  + Input clk (clock)
  + Input clear (asynchronous reset / negedge signal)
  + Input preset (synchronous and active low singal)
  + Input load\_cnt (value gets loaded when !preset)
  + Output count (output count value)

Johnson Counter

**clk**

**clear**

**count[0]**

**count[1]**

**count[2]**

**count[3]**

**preset**

**load\_cnt**

**4-bit pattern repeats every 8 cycles**

Lab3.zip folder posted on Piazza and Canvas has **johnson\_counter\_testbench.sv** testbench code to simulate with johnson counter SystemVerilog module.

**Note :**

* Assume initial load\_cnt signal value is set to 4’b0000 in testbench code provided.
* Students can update johnson\_counter\_testbench.sv code including initial load\_cnt value which can be changed or any other stimulus under initial block, and more.