2. What are the names of the 74xx series logic gates that you should use to do the above problem in real-life situation?

The logic gates that I think should be used in the problem above are a Quad 2-Input AND (74x08) and OR (74x32) normal inputs as well as a NOT gate used for the g function.

3. Calculate the delay performance (time delay between change of any input which leads to change of the output) of the two circuits designed above. Assume that you have used 74Fxx or 74LSxx series gates to implement the circuit. Use respective data sheets for the required chips.

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC08										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 6 [1]								
		V_{CC} = 2.0 V	-	25	90	-	115	-	135	ns
		V_{CC} = 4.5 V	-	9	18	-	23	-	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	7	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	7	15	-	20	-	23	ns
t_t	transition time	see Fig. 6 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	10	-	-	-	-	-	pF

Figure 1 AND Gate

CD54/74AC257, CD54/74ACT257, CD74AC1258

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case) **(Continued)**

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay, $\overline{OE}$ to Y AC/ACT257	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	5	4.1	-	14.6	4	-	16.1	ns
Propagation Delay, In to $\overline{Y}$ 'AC/CD74ACT258	t_{PLH}, t_{PHL}	5	2.4	-	8.5	2.3	-	9.3	ns
Propagation Delay, S to $\overline{Y}$ 'AC/CD74ACT258	t_{PLH}, t_{PHL}	5	4	-	14	3.9	-	15.4	ns
Propagation Delay, $\overline{OE}$ to $\overline{Y}$ 'AC/CD74ACT258	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	5	4.1	-	14.6	4	-	16.1	ns
Three-State Output Capacitance	C_O	-	-	-	15	-	-	15	pF
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	130	-	-	130	-	pF

NOTES:

Figure 2 OR Gate

F) 3 or gates

8.5 + 8.5 + 8.5 = 25.5 ns

G) 2 and gates and 1 or

18 + 18 + 8.5 = 44.5 ns

4. Which data sheet parameter(s) did you use to calculate the delay performance and why?

I used the Propagation Delay, In to Y 'AC/CD74ACT258 for the OR Gate at -40 to 85 degrees Celsius, I believe that this would represent best the OR gate in the scenario listed above in an everyday unit. For the AND gate I used 25 degrees Celsius at a voltage of 4.5 at max to represent the worst case possible in what I believe to be the everyday scenario.

Part 2:

1. Identify the following design parameters –

a. Number of switches that will be required. –

7 switches, (A, B, C, D, E, F, G)

b. Number of the bits/wires required in the data bus.

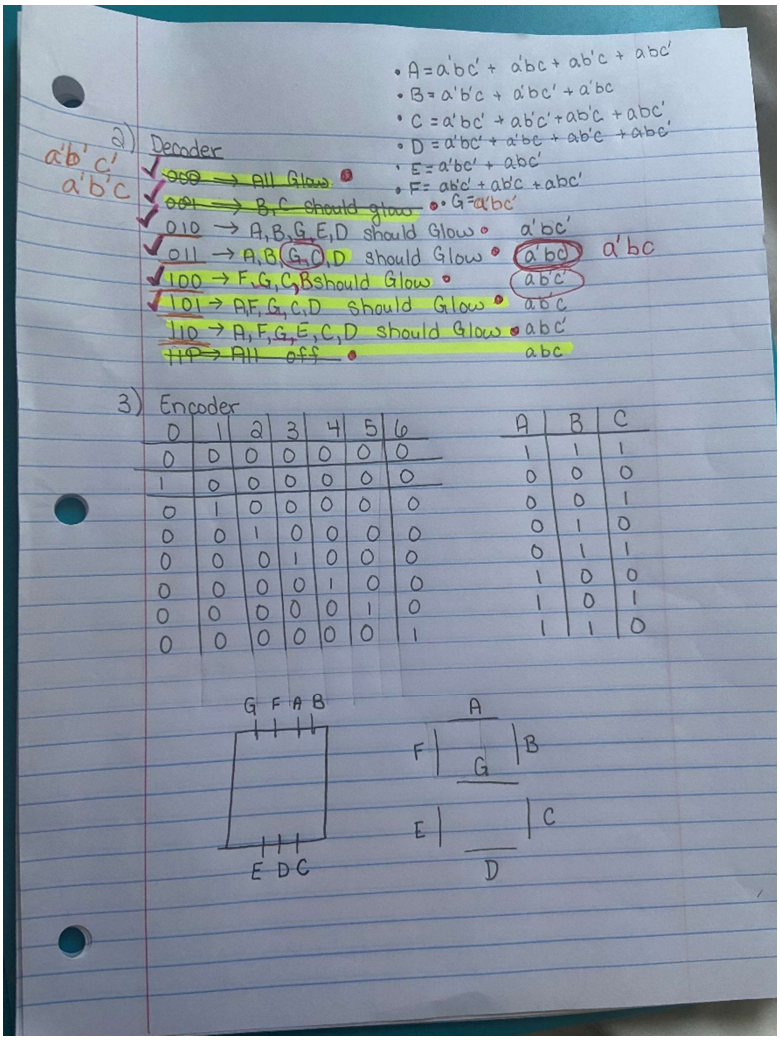
3 bits required in the data bus

c. Size of the encoder and decoder.

3X8

2. Read one of the 7 segment LED display data sheet, try to understand how to use it.

3. Design the encoder and decoder blocks with basic **logic gates** then incorporate the same into a complete digital system on Logisim.



4. Submit your design with a brief text explanation/description on how it will actually work. You must explain the working of your system to get full credit.

When all buttons are pushed the coder should display A, B, C, D, E, F, G should light up, creating a zero. When 001 is pushed B and C should be lit up creating a one. When 010 is pushed A, B, E, D, and G When none are pushed A, B, C, D, E, F and G should light up creating a zero. When 001 is pushed B and C should be lit up creating a one. When 010 is pushed A, B, E, D, and G should be lit up creating a two. When 011 is pushed A, B, C, D, and G should be lit up creating a three. When 100 is pushed B, C, F, and G should be lit up creating a four. When 101 is pushed A, C, D, F, and G should be lit up creating a five. When 110 is pushed A, C, E, D, F, and G should be lit up creating a six. And lastly when 111 is pushed there should be no lights on.