SWICS DPU

F. Gliem
W. Rieck
H. Dinse

TU Braunschweig
Institut für Datenverarbeitungsanlagen
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CONTENTS

1. Introduction

This paper is a short description of the SWICS DPU. It is not a complete documentation but a reference manual for those who are familiar with the instrument.

The aim of this paper is to answer questions which could arise during operation of the instrument or during data analysis. Therefore the main topics are: (i) interpretation of science data and housekeeping data transmitted with the experiment data block; (ii) description of the commands that control the instrument and (iii) description of the operation modes.

For further details please contact the authors.

2. The SWICS DPU

2.1 Tasks

The main tasks of the SWICS DPU are:

(i) measurement control
DPU controls Deflection Plate Power Supply, Post Acceleration Power Supply and Sensor Electronics. Operation modes are changed automatically or by memory load commands.

(ii) data flow control
DPU selects, buffers and formats both science and housekeeping data.

(iii) fast onboard data preprocessing
DPU adapts the high raw data rate (maximum average event rate: 10 kHz or 24 bit * 10 kHz = 0.24 Mbps) to the low telemetry rate (88 bps, 44 bps, 22 bps or 11 bps according to telemetry mode).

2.2 Configuration

Fig. 2.2-1 and 2.2-2 show the basic DPU configuration. The "Fast Data Preprocessing" block constitutes the core of the DPU. This block implies (1) the real time event classification (max. event rate: 20 kHz), (2) the counting memory for the individual classes (512 * 24 bit channels) and (3) the extraction of distinct events according to a priority scheme (30 PHA-words).

The encirled numbers in Fig. 2.2-2 are the reference numbers of the attributed electronic boards. The boards 1 and 2 provide all interfaces to both the experiment and the S/C.

The three boards 3, 4 and 5 are attributed to the "Fast Data Preprocessing", in detail 3 and 4 to the classification procedure and 5 to the counting memory.

Board 6 and 7 are attributed to the data processing and experiment control, which is based on a CDP 1802 micro-processor. Board 7 contains the program memory (7 k * 8 bit) and the µP are located on board 6.

The board stack is sketched in Fig. 2.2-3. The size of the daughter boards is outlined in Fig. 2.2-4. All daughter boards with exception of board 8, the dc-dc-converter, are 6-layer-boards with 1.2 mm thickness. The heavier parts of the power supply are mounted on a 1.5 mm board. The mother board is a 6-layer-board with 1.5 mm thickness. Mother board and daughter boards are connected via 80-Pin Mil-Strip-Connectors.

All signals between S/C and DPU are fed via the DCM37P connector and all signals between experiment and DPU via the MDM51P connector. The DEM9P connector is used for the power lines.

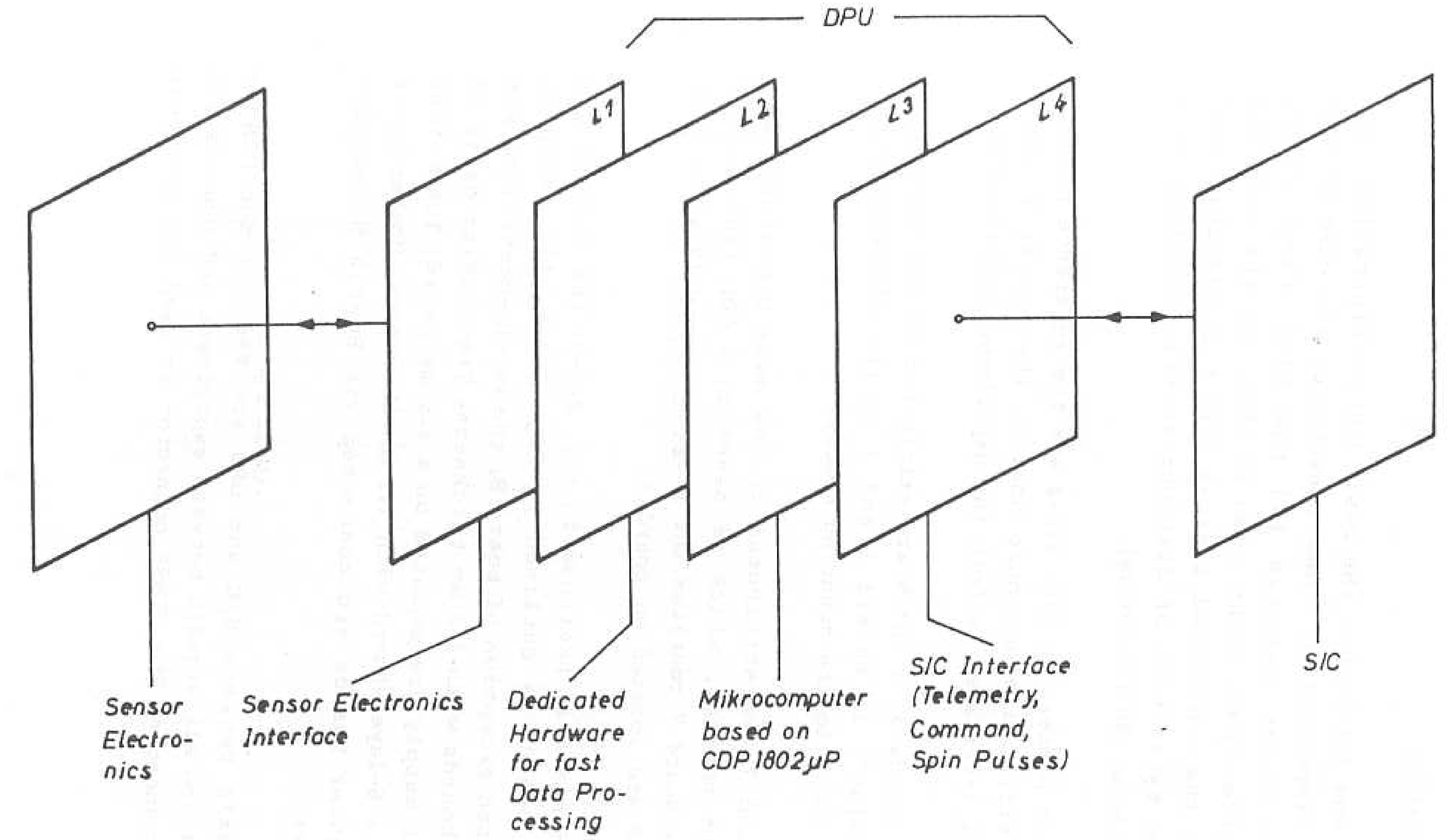


Fig. 2.2-1 Four Level Structure of the SWICS DPU

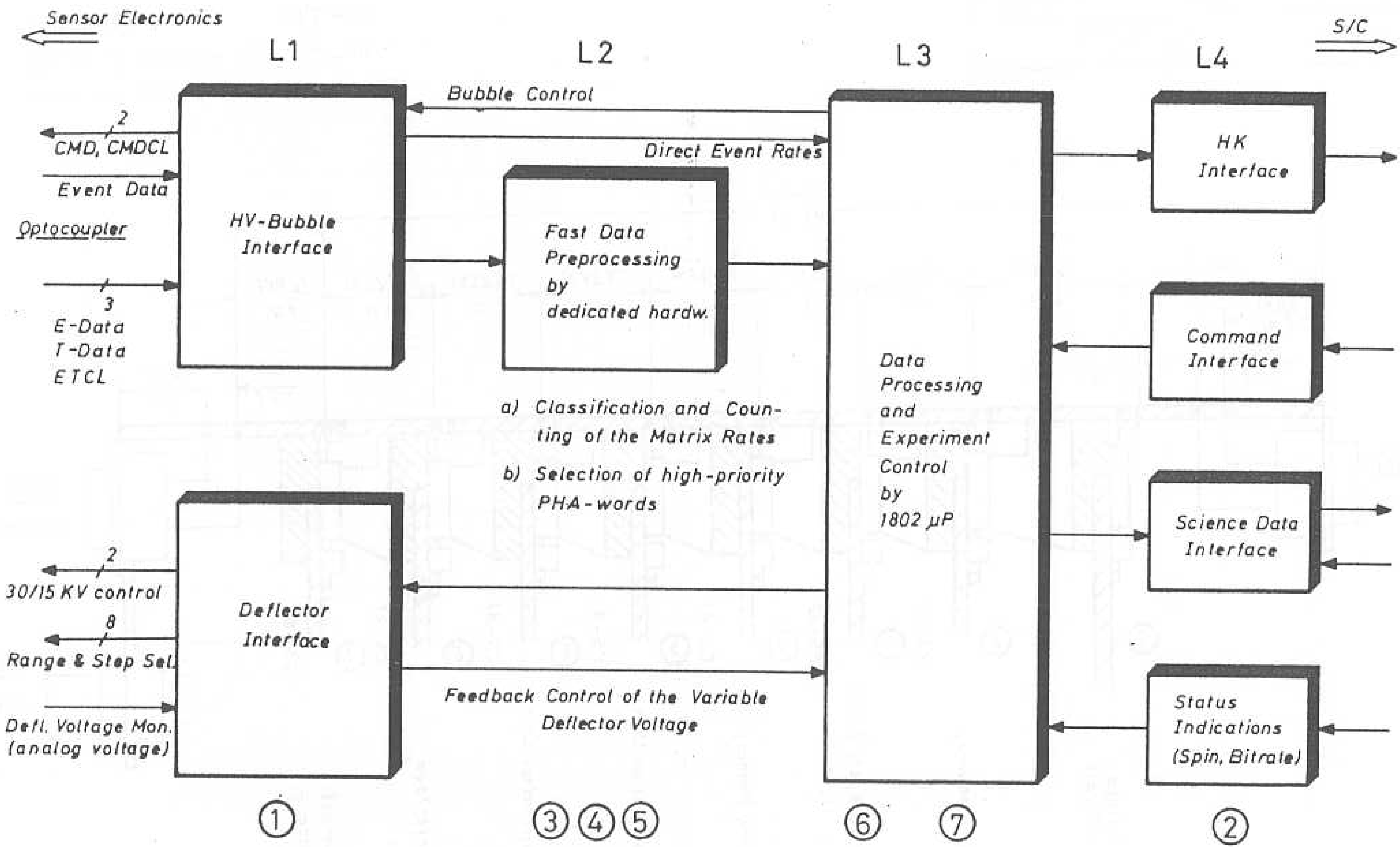
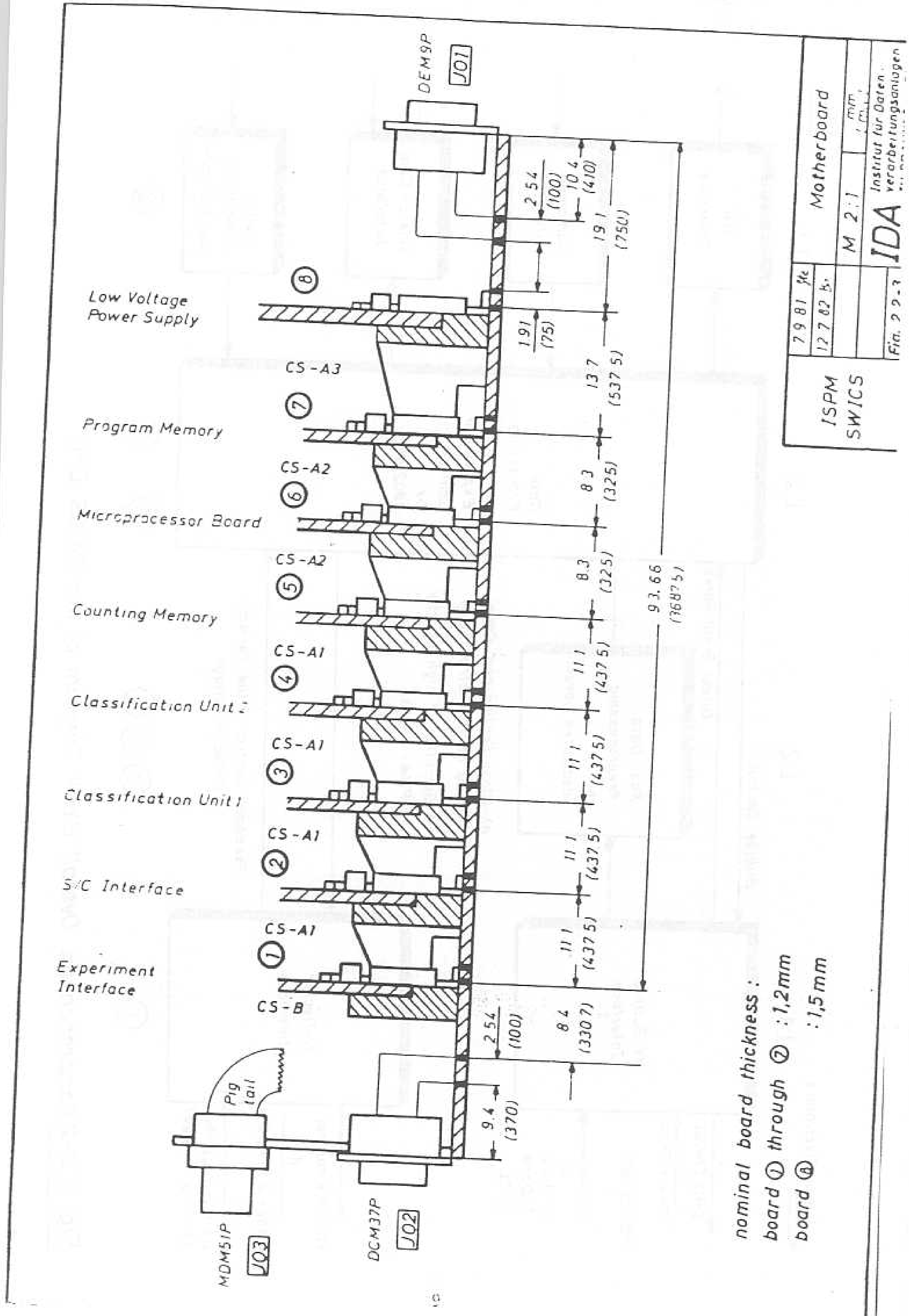
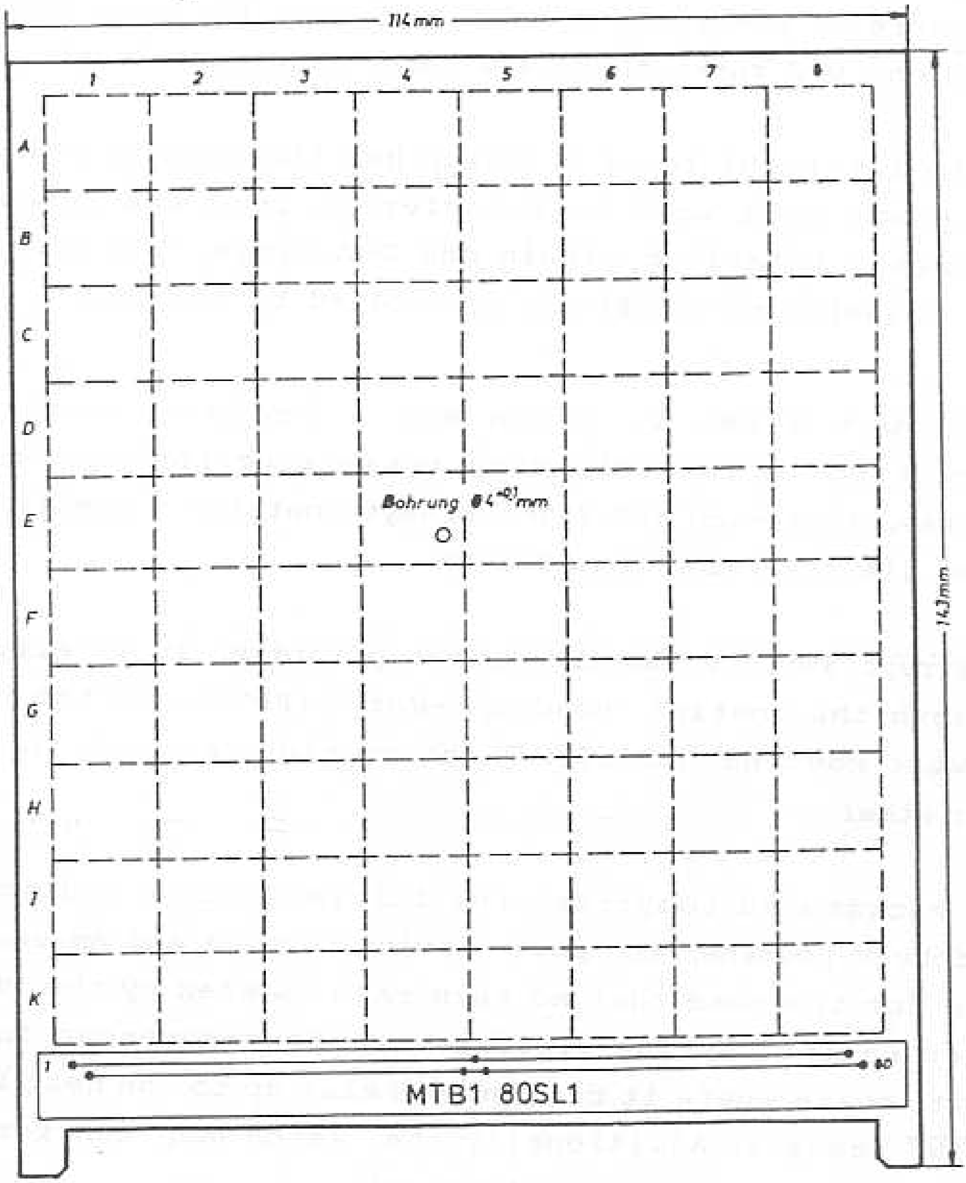


Fig. 2.2-2 Comprehensive Overall Block Diagram of the SWICS DPU


Low Voltage Power Supply
Program Memory
Microprocessor Board
Counting Memory
Classification Unit 2
Classification Unit 1
S/C Interface
Experiment Interface
CS-A3
CS-A2
CS-A2
CS-A1
CS-A1
CS-A1
CS-A1
CS-B
8
7
6
5
4
3
2
1
DEM9P
J01
DCM37P
J02
MDM51P
J03
Pig tail
2.54 (100)
10.4 (410)
19.1 (750)
1.91 (75)
13.7 (537.5)
8.3 (325)
8.3 (325)
11.1 (437.5)
11.1 (437.5)
11.1 (437.5)
11.1 (437.5)
93.66 (3687.5)
2.54 (100)
8.4 (330.7)
9.4 (370)
nominal board thickness :
board 1 through 7 : 1,2mm
board 8 : 1,5mm
ISPM SWICS
Motherboard
M 2:1
IDA
Institut für Datenverarbeitungsanlagen



ISPM

SWICS

20.5.85

Fig. 2.2 - 4

Daughterboard

IDA Institut für Datenverarbeitungsanlagen TU BRAUNSCHWEIG

2.3 Program Structure

The program structure (Fig. 2.3-1) reflects the interrupt structure of the SWICS DPU. According to the priority of the different DPU tasks there are three interrupt levels.

In the interrupt level 0, which has the highest priority , one 8 bit data word is transferred from the RAM to the Telemetry interface within one DMA cycle. The succeeding data transfer to the S/C is controlled by the S/C.

Interrupt level 1, which has a medium priority, is attributed to the telemetry frame synchronization. This ensures, that each S/C-frame always contains a complete EDB-frame (11 byte, see Fig. 3.1-1).

Interrupt level 2 has the lowest priority. It is attributed to both the routine 'Read E/T-Word' (RDET) and the 'Sector Service Routine' (SECSR). These routines can not interrupt each other.

The background comprises the initialization routine, the selfcheck routine, the power saving routine and an emergency mode for the case that no spin rate is seen by the DPU. The power saving routine directs the microprocessor into the 'Wait' state where it remains dormant up to the next $\overline{\text{DMA OUT}}$ or $\overline{\text{INT}}$ request. Additionally the 'watch dog' can force the microprocessor out of the dormancy.

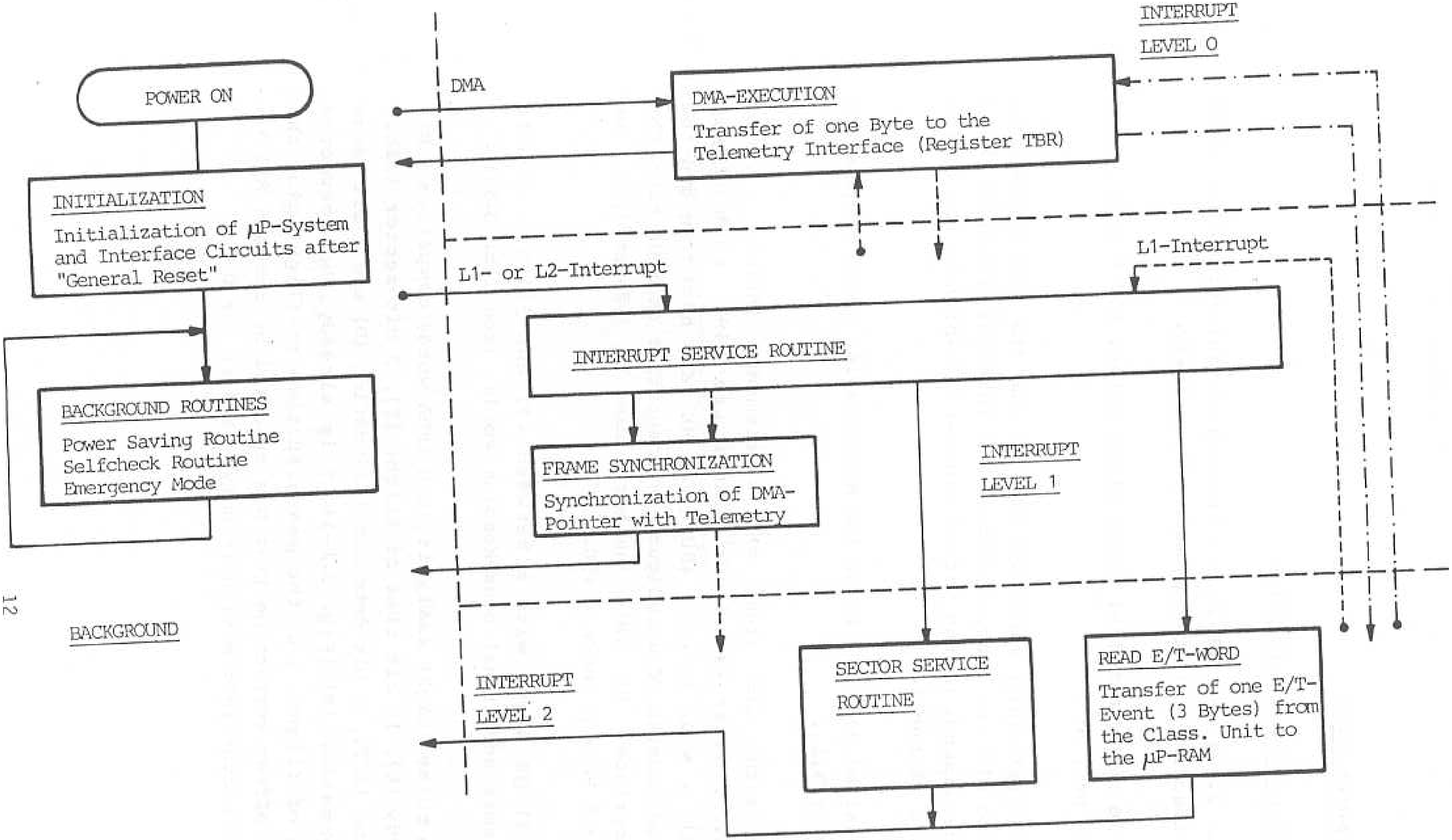


Fig. 2.3-1: SWICS Program Structure

3. SWICS Data

3.1 Experiment Data Block

Figs. 3.1-1 and 3.1-2 show the experiment data block (EDB) for tracking and storage mode respectively.

The 16 bit identifier has a fixed value: ID0 = hex. 14 and ID1 = hex. 6F .

The housekeeping words HK1 and HK2 and the matrix elements ME0 to ME7 are subcommutated. The interpretation of these words depends on the period counter PC which is one of the status channels.

A detailed description of the housekeeping words is given in chapter 3.5 .

With each EDB eight matrix elements (ME(n), $n = 0, 1, \ldots, 7$) are read out. There are 491 such rates ME(x), $x = 0, 1, \ldots, 490$). The ME rate number n and the period counter PC unambiguously identifies each ME rate. The appropriate ME rate number can be determined by $x = 8 * PC + n$ for $x \leq 490$.

The 21 ME words with x between 491 and 511 are used to transmit additional housekeeping words (see Tab. 3.5-1).

Each pulse height analysis word (PHA word) comprises 8 bit energy (E), 10 bit time of flight (T), 3 bit sector information (SCT), 2 bit detector information (D) and 1 bit range information (R) (Fig. 3.1-3). T is already the corrected time of flight, i.e. the measured time of flight plus the time offset correction that was selected by command ML3.0 . The detector information is only valid if $E \neq 0$.

8-Bit Words →

11-Word Frames ↓

	0	1	2	3	4	5	6	7	8	9	10
0	IDØ	ID1	HKØ	HK1	HK2	DRØ FSR	DR1 DCR	DR2 TCR	DR3 MSS	DR4 ACPS1	DR5 ACAS1
1	DR4S ACPS2	DR5S ACAS2	MRØ PR	MR1 AR	MR2						MR8
2	MR9								MR17	BRØ	BR1
3	BR2	MEØ							ME7		PHAØ
4			PHA1								
5											
6											
7											
8											
9											
10											
11										PHA29	

$T_{Fr} = 1$ s

$T_{EDB} = 12$ s

Fig. 3.1-1: Experiment Data Block for Tracking Mode

DR: Detector Rate; PR: Proton Rate; AR: Alpha Rate;
MR: Matrix Rate; BR: Basic Rate; ME: Matrix Element

8-Bit Words →

11-Word Frames ↓

Frame	0	1	2	3	4	5	6	7	8	9	10
0	IDØ	ID1	HKØ	HK1	HK2	DRØ FSR	DR1 DCR	DR2 TCR	DR3 MSS	DR4 ACPS1	DR5 ACAS1
1	DR4S ACPS2	DR5S ACAS2	MRØ PR	MR1 AR	MR2						MR8
2	MR9								MR17	BRØ	BR1
3	BR2	MEØ							ME7	←	PHAØ
4	→	←	PHA1	→							
5									←	PHA7	→

Fig. 3.1-2: Experiment Data Block for Storage Mode

DR: Detector Rate
PR: Proton Rate
AR: Alpha-Rate
MR: Matrix Rate
BR: Basic Rate
ME: Matrix Element

Tel. Mode	T_{Fr} /s	T_{EDB} /s
STMA (512 bps)	2	12
STMB (256 bps)	4	24
STMC (128 bps)	8	48

0																							23
E7							E0	T9									T0	S2	S1	S0	D1	D0	R

Fig. 3.1-3: Bit Allocation in the PHA Word

E0 ... E7: Energy, msb : E7

T0 ... T9: Time of Flight, msb : T9

S0 ... S2: Sector (one of eight), msb : S2

D0 ... D1: Detector (one of four)

R : Range, R = 0: range R0
R = 1: range R1 if $E \neq 0$
range R2 if $E = 0$

D1	D0	Detector
0	0	MSS 3
0	1	MSS 2
1	0	MSS 1
1	1	USS

Data Group	Data Item	Accumulation Time	Data Type	Remark
ID & housekeeping	ID0	-------------	binary	hex: 14
	ID1	-------------	"	hex: 6F
	HK0	1 Period	"	subcommutated, see fig. 3.5-1
	HK1	8 Periods	"	
	HK2	16 Periods	"	
Detector Rates	FSR	1 Period	floating point	
	DCR	1 "	" "	
	TCR	1 "	" "	
	MSS	1 "	" "	
	ACPS1	1 "	" "	
	ACPS2	1 "	" "	
	ACAS1	1 "	" "	
	ACAS2	1 "	" "	
Matrix Rates	MR n	1 Period	floating point	n = 0, 1, ... , 17
Basic Rates	BR n	1 Period	floating point	n = 0, 1, 2
Matrix Elements	ME (8*PC+n)	1 Cycle	floating point see tab. 3.5-1	ME 0 to ME 490 } n = 0, 1, ... , 7 ME 491 to ME 511 }
Direct Events	PHA n	1 Period	see fig. 3.1-3	n = 0, 1, ... , 29

Tab. 3.1-1: Summary of SWICS Science - and Housekeeping Data

3.2 Data Accumulation and Transmission

All measurements and the data transmission are spin related. The accumulation time for most of the science data is a period (E/Q-step). Only the matrix elements (ME) are accumulated during 64 periods or a cycle.

During one period (1, 2 or 4 spins according to the telemetry mode, see 5.2) the deflection voltage is held constant. All events are counted in the respective channels (ME, MR and BR) and up to 30 PHA-Words are selected. Besides this the DPU reads the Detector Rates (FSR, DCR, TCR, MSS, ACP and ACA) 32 times per spin (i.e. every 375 ms at nominal spin rate) and accumulates them during one period. At the end of each period an experiment data block (EDB) is formatted. It will be transmitted to the S/C as soon as possible (normally during the next period).

During one cycle (64 periods) the deflection voltage is changed according to the selected deflection voltage mode (see 5.3). The matrix elements which are accumulated during one cycle will be transmitted during the following cycle (Fig. 3.2-1).

Between period 63 and period 0, i.e. between two voltage cycles, a 'sync spin' is inserted (Fig. 3.2-1). During this spin no measurements are performed.

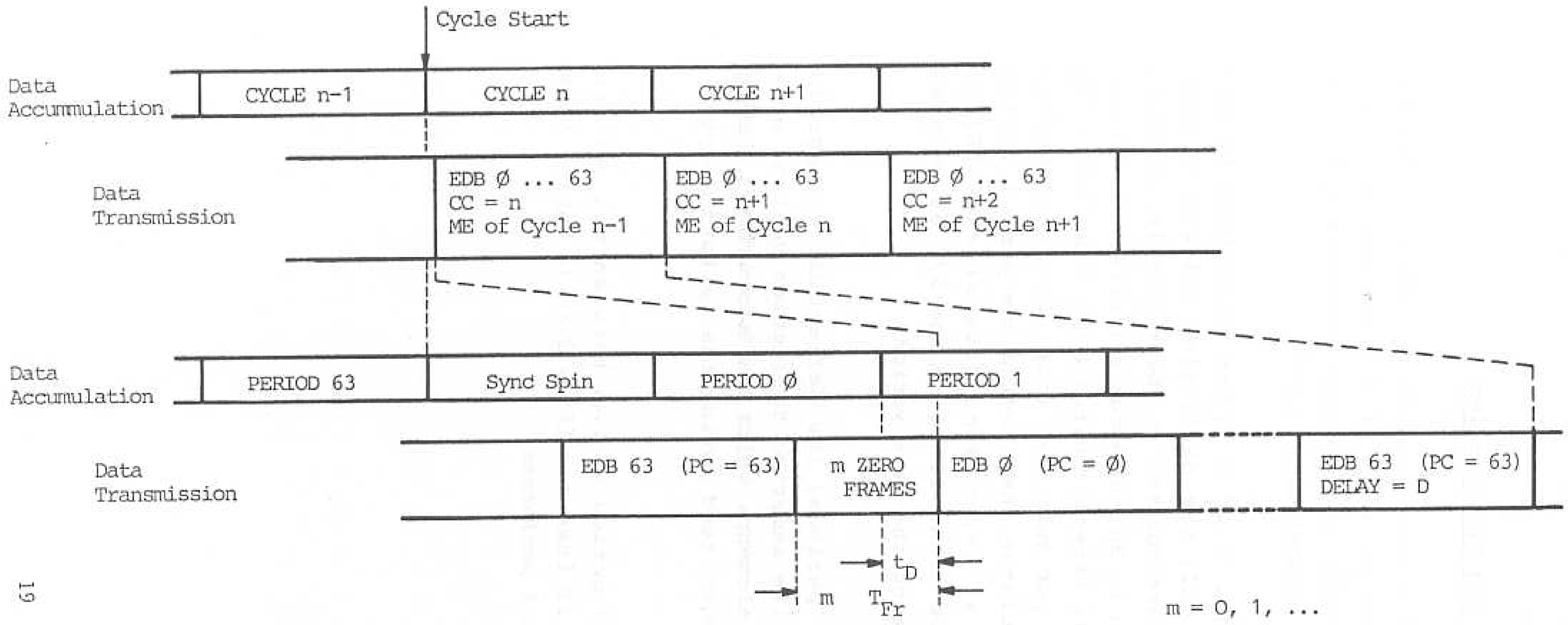


Fig. 3.2-1: SWICS Data Accumulation and Transmission

CC = Cycle Counter
PC = Period Counter

T_{Fr} = transmission time for one S/C-Frame
t_D = transmission delay of EDB Ø

3.3 Timing

3.3.1 Sectoring

The S/C signal 'spin rate' is used to devide each spin into 8 sectors. They are numbered from 0 to 7. A measuring period always starts with sector 0.

Fig. 3.3-1 shows the normal orientation of the sectoring. Normal orientation means, that the sun direction coincides with the center line of sector 4.

The orientation of the sectoring in respect to the sun is determined by the sun pulse and the sector adjustment command ML3.2. By the sector adjustment command the position of the sun pulse in respect to the sectoring is defined.

In case that the sun pulse is not detected within the sun pulse sector defined by the sector adjustment command, the necessary synchronization is performed during the sync-spin between two voltage cycles.

3.3.2 Experiment Time and S/C Time

The DPU does not get any information about the absolute time from the S/C. If only SWICS data are considered, the revolution counter RC can be used as a time reference.

The revolution counter counts the spins of the S/C. It is incremented at the beginning of sector 0 of each spin and transmitted with every 8^{th} EDB as housekeeping word HK1.1 (Fig. 3.5-1 and A3)

An additional information about the time relation of different EDB's can be gained from the period counter PC (A3) and the cycle counter CC (A3)
In order to establish a relation between the absolute time

and the relative time of the experiment, the time when the first EDB of a cycle (EDB0, PC=0) is formatted until it begins to be read out is measured with a resolution of 1/32 spin. This delay D is transmitted as EDB-word ME3 with EDB61 (Fig. 3.2-1, A3)

If there was no sync period inserted between period 0 and period 1 (in this case the end of period 1 coincides with the formatting of EDB0), the transmission delay t_D can be calculated as follows.

$$t_D = \frac{T_S}{32} * D$$

The spin period T_S (nominal 12 s) is available in the S/C housekeeping data.

The condition that no sync period follows period 0 is fulfilled if RC (period 8) - RC (period 0) = n * 8, where n=1 for TRM (1024 bps) or STMA (512 bps), n=2 for STMB (256 bps) and n=4 for STMC (128 bps).

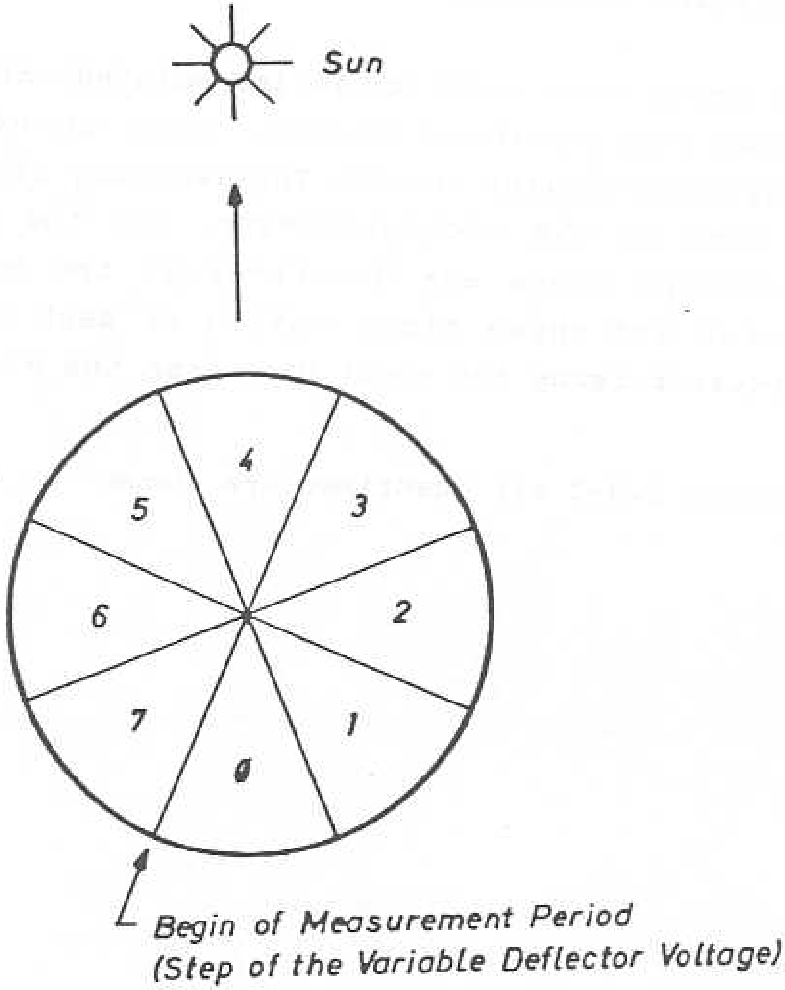


Fig. 3.3-1: SWICS Sectoring

3.3.3 Deadtimes of the DPU

There are some short time intervals during which the DPU count rates (ME, MR and BR) are not incremented and no PHA words are assembled.

The count rates will not be incremented while the processor reads the counting memory. This is necessary at the beginning of each sector. The assembly of PHA words, which is done by the microprocessor, has the lowest priority. Therefore there are deadtimes at the beginning of each sector and three times within of each sector while the processor reads the event data from the HV-bubble.

In Fig. 3.3-2 all deadtimes are shown.

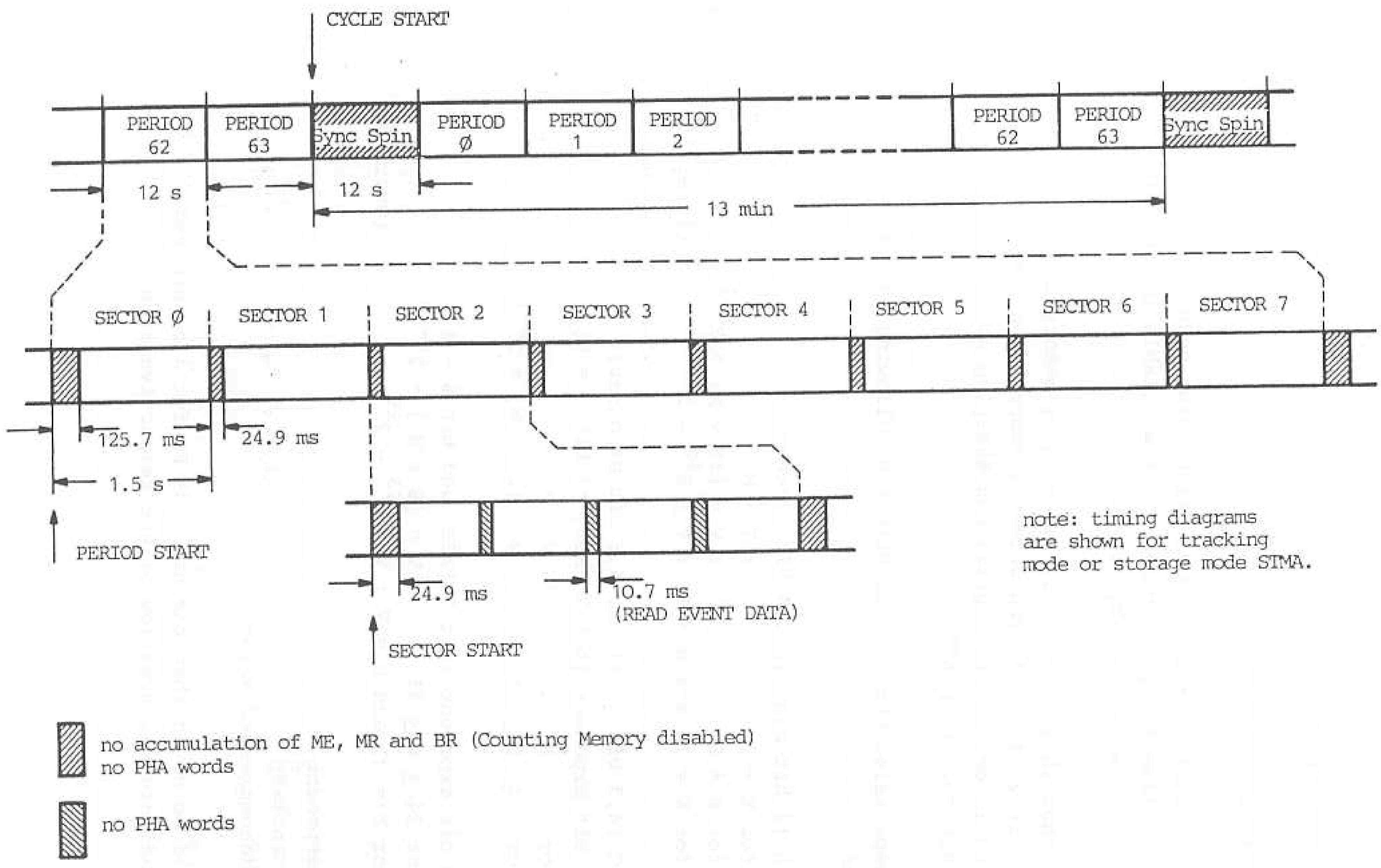


Fig. 3.3-2: Deadtimes of the SWICS DPU

3.4 Science Data

3.4.1 Data Compression

For the compression a uniform floating point code (A) and a non-uniform floating point code (C) is available in the DPU. Both codes are shown in Tab. 3.4-1.

The code that shall be used is selected by memory load command (bit 2 of ML2.A) The selected compression code is identified in one of the digital housekeeping words (bit 6 of HK1, subcom. state X000)

The decompression can be done with the following set of equations:

1. Code A (4 bit mantissa, 4 bit exponent):

   for $E = 0$: $V = M$

   for $E \neq 0$: $V = (16 + M) * 2^{E-1}$

   for $E = 15$ and $M = 15$: $V \geq 2^{19} - 2^{14}$ (Overflow)

2. Code C (4,3 bit mantissa, 4,5 bit exponent):

   a) 4 bit exponent (bit 7 (MSB) or bit 6 = 0)

   for $E = 0$: $V = M$

   for $1 \leq E \leq 11$: $V = (16 + M) * 2^{E-1}$

   b) 5 bit exponent (bit 7 (MSB) and bit 6 = 1)

   for $24 \leq E \leq 31$: $V = (8 + M) * 2^{E-12}$

   for $E = 31$ and $M = 7$: $V \geq 2^{23} - 2^{19}$ (Overflow)

E = exponent
M = mantissa
V = decompressed value

It should be noted that the hex code FF for a compressed value indicates an overflow of the respective rate.

A			C		
E	M	value V	E	M	value V
0000	XXXX	0			
0001	XXXX	to 16			
0010	XXXX	32			
0011	XXXX	64			
.					
.					
.					
0111	XXXX	2^{10}			
1000		2^{11}			
1001		2^{12}			
1010		2^{13}			
1011		2^{14}			
1100		2^{15}	11000	XXX	2^{15}
1101		2^{16}	11001	XXX	to 2^{16}
1110		2^{17}	11010	XXX	2^{17}
1111	XXXX	2^{18}	11011	XXX	2^{18}
		to $2^{19}-2^{15}$	11100	XXX	2^{19}
		$\approx 5*10^5$	11101	XXX	2^{20}
1111	1111	$\geq 2^{19}-2^{14}$	11110	XXX	2^{21}
			11111	XXX	2^{22}
					to $2^{23}-2^{20}$
					$\approx 7.3*10^6$
			11111	111	$\geq 2^{23}-2^{19}$

Tab. 3.4.-1: Code Table for SWICS / CHEM Compression Codes
E = Exponent , M = Mantissa

3.4.2 PHA Words

During one voltage step (n_s spin revolutions, n_s = 1,2 or 4) up to 90 E-T pairs are selected and transferred to the microprocessor system and there assembled to PHA words (Fig. 3.1-3). The selection condition is supplied by the microprocessor and changed after 30 E-T pairs are transferred, i.e. 3 times per voltage step. The PHA words are stored in a FIFO store (part of the µP-RAM) with a capacity of 30 PHA words. Thus only the last 30 E-T pairs transferred are available for the transmission to ground.

The whole NM-NQ matrix is devided into 3 ranges (R0,R1 and R2). At the beginning of a voltage step a certain priority is assigned to each range. For the priority assigment two modes are foreseen: the normal mode with fixed priority assigment (range R2: high priority, range R1: medium priority, range R0: lowest priority) and the rotating mode with a rotating priority system. In addition it is possible to mask events from range R2 while the sensor faces the sun (sun gating), to mask all events from range R2 or to mask all events from the ranges R2 and R1.

The first 30 E-T pairs that are transferred to the microprocessor system are taken from any of the three ranges. The next 30 E-T pairs from the ranges with medium or high priority. The last 30 events that are transferred during one voltage step are from the high priority range only.

The transfer of the E and T values and the additional information about the detector and the range is controlled by the microprocessor. To transfer an E-T pair and assemble a PHA word takes about 656 µs. Due to other activities of the microprocessor (event data transfer, data transfer to the telemetry, etc.) the transfer of E-T pairs can take place during about 95% of a spin period only. The classification is not interrupted by the transfer of the E and T values.

3.5 Housekeeping Data

3.5.1 Digital HK-Words

The EDB-word HK0 contains the 4 least significant bits of both the period counter and the deflection voltage code. The 4 most significant bits (PCL) of HK0 indicate the sub-commutation state for HK1 and HK2.

The EDB-words HK1 and HK2 contain subcommutated housekeeping data. In Fig. 3.5-1 all subcommutated hk words are shown. The contents of these words is a snapshot of the instrument status.

HK1 indicates the instrument status at the beginning of period n*8 (n = 0, 1, ... , 7).

The bubble hk informations (BUHK-INFO, SID 0, ... , 6) in HK2 are analog performance parameter of the HV-bubble. They were received from the HV-bubble at the end of the period indicated by the period counter.

The hk words DPUCD0 to DPUCD8 indicate the instrument status at the beginning of period n*16 (n = 0, 1, 2, 3).

Subcom. State	HK0 (MSB … LSB)	HK1 (MSB … LSB)	HK2 (MSB … LSB)	HK-WORDS READ OUT IN EDB ...
0	0 0 0 0: DVL	:PCH: DVH	BUHK-INFO T1	0 + n * 16
1	0 0 0 1: DVL	RC	BUHK-INFO T2	1 + n * 16
2	0 0 1 0: DVL	BUCD1 : BUCD0	BUHK-INFO V+	2 + n * 16
3	0 0 1 1: DVL	BUCD2 : BUCD3	BUHK-INFO I+	3 + n * 16
4	0 1 0 0: DVL	BUCD4 : BUCD5	BUHK-INFO V-	4 + n * 16
5	0 1 0 1: DVL	BUCD6 : BUCD7	BUHK-INFO I-	5 + n * 16
6	0 1 1 0: DVL	ERROR	BUHK-INFO VMCP	6 + n * 16
7	0 1 1 1: DVL	DPU-STATUS	DPUCD8	7 + n * 16
8	1 0 0 0: DVL	:PCH: DVH	DPUCD0	8 + n * 16
9	1 0 0 1: DVL	RC	DPUCD1	9 + n * 16
A	1 0 1 0: DVL	BUCD1 : BUCD0	DPUCD2	10 + n * 16
B	1 0 1 1: DVL	BUCD2 : BUCD3	DPUCD3	11 + n * 16
C	1 1 0 0: DVL	BUCD4 : BUCD5	DPUCD4	12 + n * 16
D	1 1 0 1: DVL	BUCD6 : BUCD7	DPUCD5	13 + n * 16
E	1 1 1 0: DVL	ERROR	DPUCD6	14 + n * 16
F	1 1 1 1: DVL	DPU-STATUS	DPUCD7	15 + n * 16

$\underbrace{\text{0 0 0 0}}_{\text{PCL or SID}}$

with n = 0, 1, 2, 3

PLC = 4 l.s.b.' s of the PERIOD COUNTER ; SID = Subcommutation Identifier
PCH = bit 4 and bit 5 of the PERIOD COUNTER

DVL = 4 l.s.b.' s of the DV-Code
DVH = 4 m.s.b.' s of the DV-Code

BUCD0 through 7 = Bubble Command Status
DPUCD0 through 8 = DPU Command Status
BUHK-INFO = HK-Information from Bubble

Fig. 3.5-1: HK Subcommutation

3.5.1.1 Error Messages

A. Interrupt Error 1 (HK 1.6)

The interrupt source could not be identified. Before this message is given the microprocessor checks the flag lines EF1 (Telemetry Interrupt), EF2 (Sector Interrupt) and EF3 (PHA Interrupt) as well as the Sector Change Flip Flop SCHFF of the Sector Pulse Receiver.

B. Interrupt Error 2 (HK1.6)

Incorrect interrupt from the Sector Pulse Receiver. Only the Sector Change Flip Flop SCHFF was set.

C. No Bubble HK-Identifier (HK 1.6)

The HK-Identifier (bit 5,6, and 7 of the last 8-bit word of the subframes 1 through 7) of the bubble hk-information (BU HK-INFO) had not the expected value.

Possible reasons:

- data transfer from Bubble to DPU was disturbed, in this case detector rates and BU HK-INFO could be wrong.
- subcommutation counter of the Analog Electronics was not reset or incremented; in this case the BU HK-INFOS's and the bubble command status (BUCD0...BUCD7) in the EDB could be wrong.

This error message should be considered as a warning that detector rates, bubble command status and the bubble hk-informations of the respective monitor interval can be wrong.

D. No Bubble Sync. WORD (HK 1.6)

The bubble sync. word (the first 8-bit word of the subframes 1 through 7, hex C7) was not recognized by the DPU.

Possible reasons:

- data transfer from Bubble to DPU was disturbed, in this case detector rates and BU HK-INFO could be wrong.
- subcommutation counter of the Analog Electronics was not reset or incremented; in this case the BU HK-INFOS's and the bubble command status (BUCD0...BUCD7) in the EDB could be wrong.

This error message should be considered as a warning that detector rates, bubble command status and the bubble hk-informations of the respective monitor interal can be wrong.

E. No Spin Rate (HK 1.6)

This error message indicates that the spin rate was not seen by the DPU for more than n * 128 sec (n = 1 for tracking mode, n = 2 for storage mode A, n = 3 for storage mode B, n = 4 for storage mode C) and that the DPU was in the emergency mode 'no spin rate' during the respective monitor interval.

F. MLD Address Wrong (HK 1.6)

At least one time during the monitor interval the memory load address could not be recognized because more than one ml-command group was selected.

G. Sun Pulse not within Sun Pulse Sector (HK 1.6)

At least one time during the monitor interval the Sun Pulse was not within the sun pulse sector (SPS) possible reasons:

- there was a drastic change of the spin rate
- an additional sun pulse was received

H. No Sun Pulse (HK 1.6)

This message indicates that at least one time during the monitor interval there was no sun pulse during one spin.

I. Formating Error (HK 2.14)

This message indicates that during the monitor interval at least one EDB was not stored in the assigned RAM area and therefor will not be transmitted correctly. Besides this unexpected status changes could occur~~e~~.

K. PHA Error (HK 2.14)

During the monitor interval PHA words w~~as~~ere not stored in the assigned RAM area. It is therefore possible that some of the transmitted PHA words are incorrect and/or that unexpected status change can occur~~e~~.

If the telemetry mode was changed from tracking to storage mode during the respective monitor interval, the error message indicates that there were already more than 7 PHA-Words in the assigned RAM space (PHA-Buffer) at the time the DPU recognizes the mode change.

L. Mode Status Error (HK 2.14)

The state of the mode lines could not be identified at least one time during the monitor interval. The mode lines are read once per spin.
possible reasons:

- mode lines changed while the processor reads the lines
- noise on the mode lines

3.5.2 Deflection Voltage Monitor

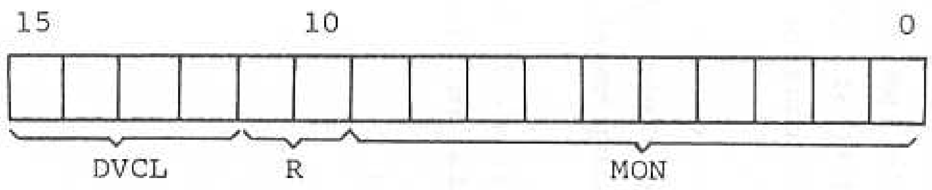
During each voltage cycle the DV-Monitor reads the voltsensor output of the Deflection Plate Power Supply (DPPS) for eight successive voltage steps. The voltsensor output is read at the end of the voltage step (end of a period).

For each voltage measurement the DPU assembles a 16 bit Deflection Voltage Monitor Word (DVM). It contains the monitor reading MON (10 bit), the range information R (2 bit) and the voltage information DVCL (4 lsb's of the respective Deflection Voltage Code DVC) (see Fig. 3.5-2).

The DV-Monitor words DVM0 through DVM3 are transmitted with the experiment data block EDB 62 and the words DVM4 through DVM7 are transmitted with EDB 63. In addition to these monitor words some related hk-words (DV-Code, period P_o, revolution REV_o and cycle) are included in EDB 61 (Tab. 3.5-1). The DV-Code, P_o and REV_o belong to the monitor word DVM0.

A complete voltage cycle is monitored during eight cycles (8*64 = 512 spin or 1:42:24 hours during tracking mode).

The DV-Monitor can be disabled by ml-command (ML2.3). HK2.13 (DPUCD5) indicates whether the DV-Monitor is enabled or disabled.



DVCL = defl. voltage (4 lsb s of DVC)
R = range
MON = monitor reading

DVC = defl. voltage control word (8 bit),
DVC is sent to the DPPS.

Measured Voltage V_{MON} = MON * Resolution

Bit 11	Bit 10	RANGE	Resolution/mV FM	Resolution/mV FS
0	0	0	0.28	0.28
0	1	1	2.0	2.0
1	0	2	5.0	4.9
1	1	3	---	---

Fig. 3.5-2: DV-Monitor Word

	EDB-WORD	Content of EDB-WORD	
EDB61	ME0	MATRIX ELEMENT "488"	
	ME1	" " "489"	
	ME2	" " "490"	
	ME3	DELAY	
	ME4	CYCLE COUNTER	
	ME5	REVOLUTION REV_O	belonging to monitor word DVM0
	ME6	PERIOD P_O	
	ME7	DV-CODE	
EDB62	ME0	BIT 8 THROUGH 15	of DVM 0
	ME1	BIT 0 " 7	
	ME2	BIT 8 " 15	of DVM 1
	ME3	BIT 0 " 7	
	ME4	BIT 8 " 15	of DVM 2
	ME5	BIT 0 " 7	
	ME6	BIT 8 " 15	of DVM 3
	ME7	BIT 0 " 7	
EDB63	ME0	BIT 8 THROUGH 15	of DVM 4
	ME1	BIT 0 " 7	
	ME2	BIT 8 " 15	of DVM 5
	ME3	BIT 0 " 7	
	ME4	BIT 8 " 15	of DVM 6
	ME5	BIT 0 " 7	
	ME6	BIT 8 " 15	of DVM 7
	ME7	BIT 0 " 7	

Tab. 3.5-1: Deflection Voltage Monitor Words DVM
and related hk-informations

3.5.3 Analog HK-Channel

A summary of all analog housekeeping channels is given in Table 3.5-2.

Exp Code	S/C Code	Channel Information	Word(s)	Frame(s)
A1	B 006	GLG 1 Temp Monitor	62	5
A2	B 017	Post-accel. Power Supply Monitor	62	13
A3	B 018	Deflection Plate Voltage Monitor	62	21
A4	B 011	Current Monitor (+28V)	62	29
A5		GLG Subcom	62	6
A5/0		Identifier/Sync Ref	"	"
A5/1	B 012	DPU +28V Monitor	"	"
A5/2	B 014	DPU +5V Monitor	"	"
A5/3	B 015	DPU -5V Monitor	"	"
A5/4	B 013	DPU +10V Monitor	"	"
A5/5		DPU +28V Monitor (as B012)	"	"
A5/6		DPU +5V Monitor (as B014)	"	"
A5/7		DPU -5V Monitor (as B015)	"	"
T1	B 003	GLG 2A Temp (S/C Thermistor)	66	8

Tab. 3.5-2: Analog hk-channel

3.5.3.1 Temperature Monitor (Channel A1)

The thermistor is located on the Experiment Interface Board (board 1) of the DPU.
The calibration curve for FM and FS is given in Table 3.5-3 and Fig. 3.5-3.

V(A1)/V	TLM COUNTS	T/°C
0.45	23	- 40
0.75	38	- 30
1.2	61	- 20
2.25	115	0
3.25	166	+ 20
3.6	184	+ 30
3.85	196	+ 40
4.15	212	+ 60

Tab.3.5-3: GLG1 Temperature Monitor (FM,FS)

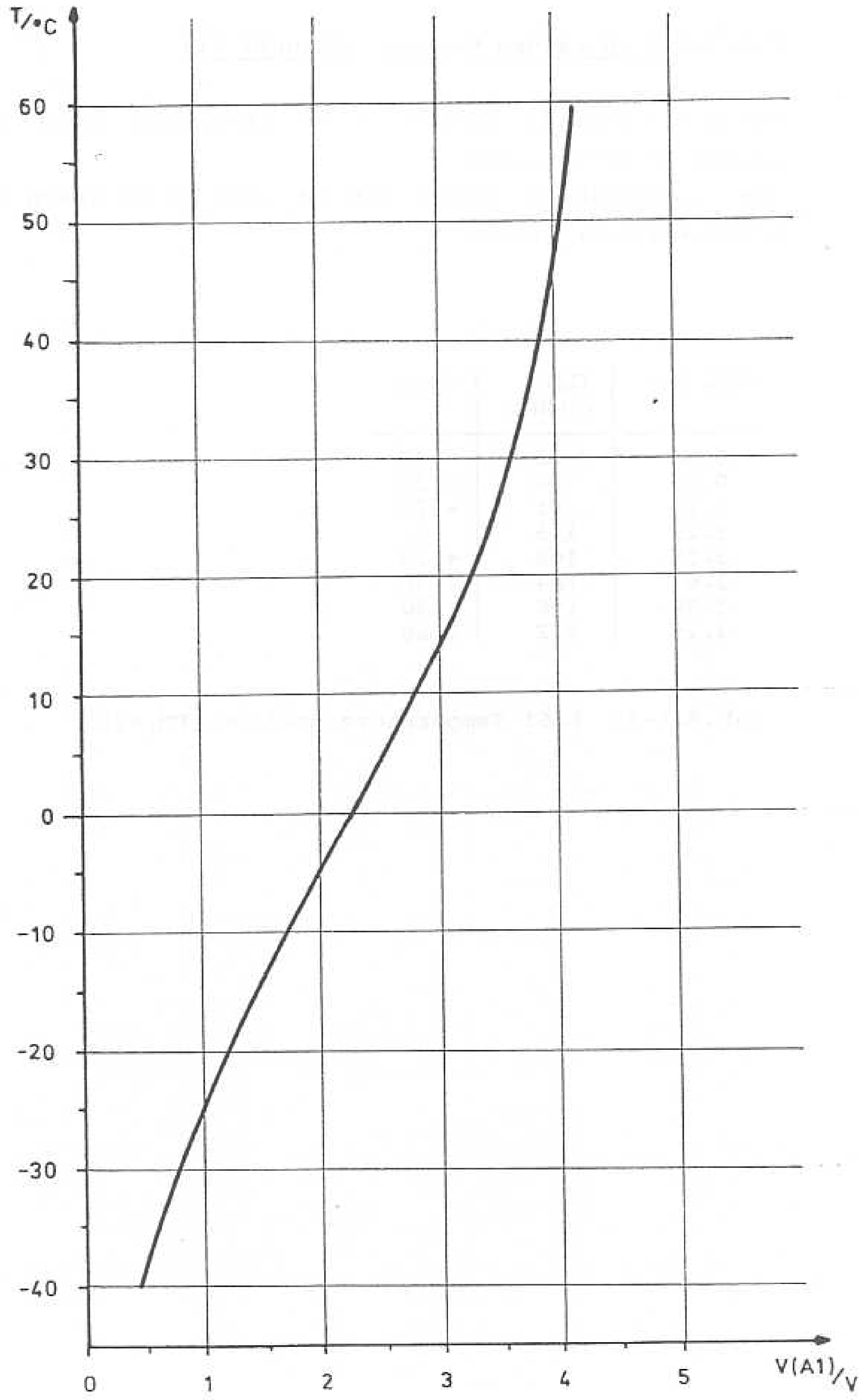


Fig. 3.5-3: GLG1 Temperature Monitor (FM, FS)

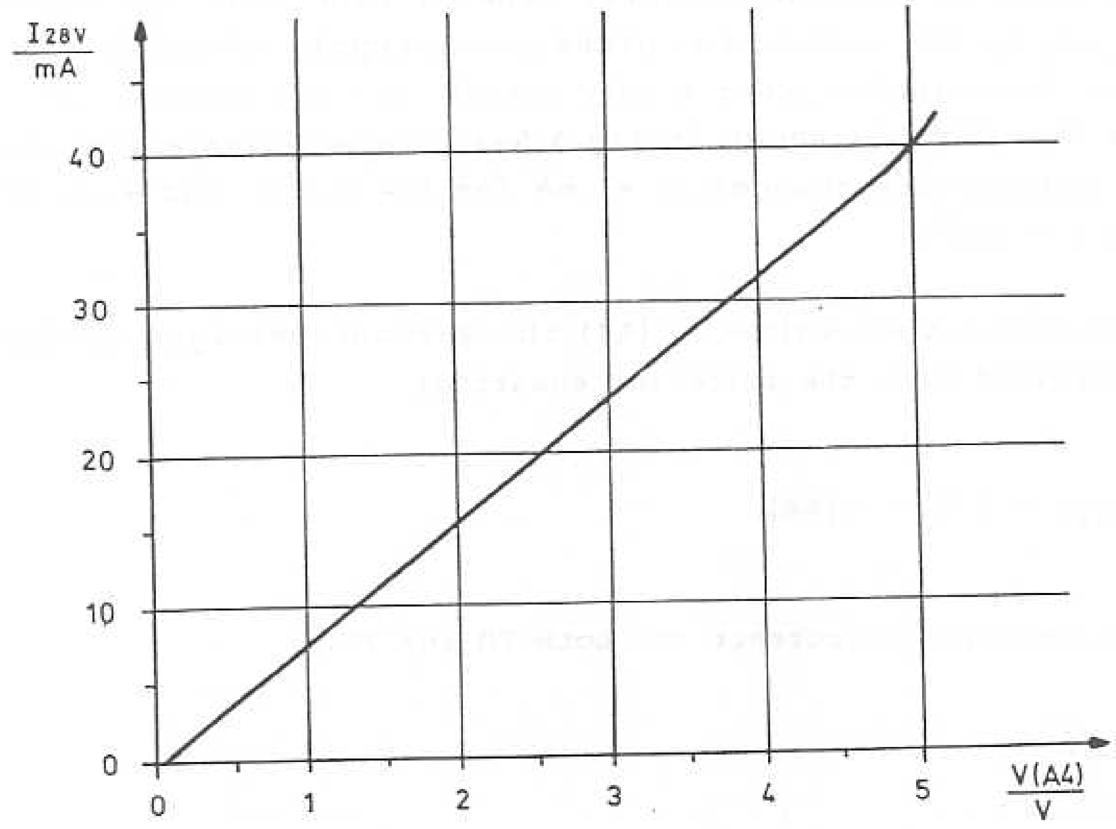
3.5.3.2 Current Monitor (Channel A4)

The current monitor measures the current from the +28V-supply to the deflection plate power supply (DPPS) and the post acceleration power supply (PAPS). The calibration curve for T = +20°C is shown in Fig 3.5-4. The maximum error due to temperature changes is -1 mA for T = -15°C and +0.5 mA for T = +30°C.

From the output voltage V(A4) the 28V-current I_{28V} can be determined with the following equation:

$$I_{28V} = 8 \frac{mA}{V} * V(A4)$$

This equation is correct for both FM and FS.



$V(A4)/V$	TLM-COUNTS	I_{28V}/mA
0	0	0
0.05	3	0
1	51	7.5
2	102	15.5
3	153	23.5
4	204	31.5
5	255	39.5

Fig. 3.5-4 : Current Monitor (+28V)

3.5.3.3. Voltage Monitor (channel A5)

The voltage monitor measures the secondary voltages of the dc-dc-converter. It is a subcommutated channel with the following subcommutation sequence:

0 - Identifier (A5/0) V(A5) > 5.2V 255 TLM COUNTS

1 - 28V Monitor (A5/1)
2 - 5V Monitor (A5/2)
3 - - 5V Monitor (A5/3)
4 - 10V Monitor (A5/4)
5 - 28V Monitor (A5/5)
6 - 5V Monitor (A5/6)
7 - - 5V Monitor (A5/7)

+28V MONITOR: A5/1, A5/5 } $V_{28V} = 8.3 * V(A5)$ FM; $V_{28V} = 8.4 * V(A5)$ FS

$V(A5)/V$	TLM COUNTS	V_{28V}/V
0	0	0
5	255	41.5

± 5V MONITOR: A5/2, A5/6 } $V_{+5V} = 1.35 * V(A5)$ FM/FS

$V(A5)/V$	TLM COUNTS	V_{+5V}/V
0	0	0
5	255	6.75

- 5V MONITOR: A5/3 $V_{-5V} = 1.345 * V(A5)$ FM

A5/7 $V_{-5V} = 1.37 * V(A5)$ FS

V(A5)/V	TLM COUNTS	V_{-5V}/V
0	0	0
5	255	-6.73

+10V MONITOR: A5/4 $V_{10V} = 2.52 * V(A5)$ FM

$V_{10V} = 2.54 * V(A5)$ FS

V(A5)/V	TLM COUNTS	V_{+10V}/V
0	0	0
5	255	12.6

4. Commands

4.1 Pulse Commands

There are two pulse commands for the SWICS experiment:

Exp. Code	S/C Code	Command Function
PC1	Z012	- 30 kV On
PC2	Z013	- 30 kV OFF

Pulse command PC1 (HV ON) is executed at the beginning of period n*16 (n = 0, 1, 2, 3) only. Pulse command PC2 (HV OFF) is executed at every period start.

To turn on the -30 kV Supply the pulse command PC1 and the appropriate ml-command (ML2.A) have to be sent.

4.2 Memory Load Commands

There are three ml-command groups: ML1, ML2 and ML3. Each group has its own enable line (ML CMD ADDR 1, ML CMD ADDR 2 and ML CMD ADDR 3) which shall remain low during the command transmission (Tab. 4.2-1).

Command Group	S/C Code	ML CMD ADDR 1	ML CMD ADDR 2	ML CMD ADDR 3
ML1	Z007	0	1	1
ML2	Z008	1	0	1
ML3	Z009	1	1	0

Tab. 4.2-1: Assigment of ML-Adresses to ML-Command Groups

The most significant bit (bit 15) of each ml-command is used to identify whether the following 4 bits (bit 14 to bit 11) are command bits or address bits. If bit 15 (identifier) is 1, bit 14 to bit 0 are command bits. If bit 15 is 0, bit 14 to bit 11 are address bits and bit 10 to bit 0 are command bits. A summary of all ml-commands is given in appendix A1.

Most of the ml-commands are executed at Cycle Start only. In Table 4.2-2 it is listed at which time the different ml-commands will be executed.

The memory load command receiver of the DPU is read at the beginning of each sector, i.e. every 1.5 sec at nominal spin period. Thus ml-commands must not be sent at a rate faster than 2 seconds.

Memory Load Command		Cycle Start	Period n x 16	Period n x 8	Period Start
ML1.0	Commands to Analog Electronics				
	a) Special Test Mode 1				X
to	b) Not Test Mode 1				
	Bit 2 = 0			X	
ML1.3	Bit 2 = 1	X			
ML2.A	Internal Heater on		X		
	Internal Heater off				X
	Deflection Plate Voltage Mode *	X			
	DPPS on		X		
	" off				X
	PAPS to -30 kV / -15 kV		X		
	PAPS enabled		X		
	PAPS disabled				X
	FSR for automatic step reversal *	X			
	Automatic step reversal on/off *	X			
	Data Compression Code	X			
ML2.0	Analog HV-Control		X		
ML2.1	Correction for Emergency Timer				X
ML2.2	Leave Emergency Mode "NO FRM PLS"	X			
	DV-Monitor enabled/disabled	X			
ML2.3	Special Test Modes	X			
ML2.4	Emin for Det. USS	X			
ML2.5	Emin for Det. MSS1	X			
ML2.6	Emin for Det. MSS2	X			
ML2.7	Emin for Det. MSS3	X			
ML3.A	DPU Mode	X			
	Automatic Calibration Cmd.	X			
	Sun Gating of R2	X			
	PHA Priority Mode	X			
ML3.0	Time Offset Correction	X			
ML3.1	ACA/ACP-Rates from sector	X			
ML3.2	Sector Adjustment	X			
ML3.3	Start Next Cycle				X
ML3.4	Sectoring of ME,MR,BR,PHA-Words	X			
ML3.5	Sector Adjustment if no Sun Pulse	X			
ML3.6	DV-Code (during DPU Mode 1 only)				X

Tab. 4.2-2: Execution of ML-Commands
* not executed during DPU Mode 1 (test mode)

4.2.1 Sector Adjustment Command

The sector adjustment command consists of two parts: the sun pulse sector SPS and the fine adjustment FA. The sun pulse sector determines within which sector the sun pulse shall occure. The fine adjustment determines the offset of the sun pulse from the center line of the sun pulse sector (Fig. 4.2-1).

The bit assignment of the sector change command is given in Table 4.2-3.

4.2.2 Sun Gating of Range R2

The sun gating command (bit 8, 9 and 10 of ML3.A) determines an angle or direction from which the DPU will not assemble PHA words from range R2 (mass zero events). Besides this, the basic rate BR2 will not be incremented while the sensor is in the gated sector. The angle is symetrical to the center line of sector 4, the nominal sun direction. In Table 4.2-4 the gated sectors are listed.

bit 10 9 8	gated sectors
0 0 1	4
0 1 1	3 4 5
1 0 1	2 3 4 5 6
1 1 1	1 2 3 4 5 6 7

Tab. 4.2-4: Bit Assignment of the Sun Gating Command ML3.A

If bit 8 of memory load command ML3.A is 0, the range R2 or both range R2 and R1 can be disabled. This means, that from the disabled range no PHA-words are assembled. The respective basic rates are not affected.

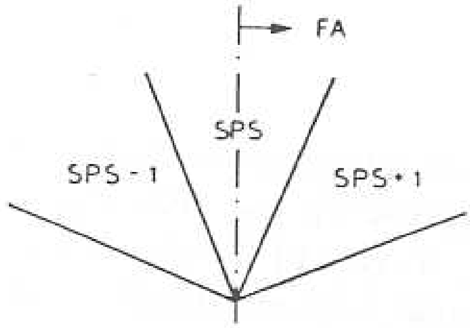


Fig. 4.2-1: Fine Adjustment of Sectoring

bit 9	8	7	6	Fine Adjustment FA
1	0	0	0	-22.5°
1	0	0	1	-19.6875°
1	0	1	0	-16.875°
1	0	1	1	-14.0625°
1	1	0	0	-11.25°
1	1	0	1	-8.4375°
1	1	1	0	-5.625°
1	1	1	1	-2.8125°
0	0	0	0	0°
0	0	0	1	2.8125°
0	0	1	0	5.625°
0	0	1	1	8.4375°
0	1	0	0	11.25°
0	1	0	1	14.0625°
0	1	1	0	16.875°
0	1	1	1	19.6875°

bit 5	4	3	Sun Pulse Sector SPS
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Tab.: 4.2-3: Bit Assignment of the SWICS Sector Adjustment Command ML3.2

5. Operation Modes

5.1 Status after Power On

After the main power (+28V) is switched on (command Z109) or after a general reset is executed by the DPU, the instrument will be in a 'save mode', i.e. all high voltage power supplies (PAPS,DPPS and MCPPS) are disabled. Besides this the heater and all detectors are off in order to reduce the power consumption to a minimum.

A housekeeping bit (bit 0 of HK2.12 (DPUCD4)) will indicate that a power on reset was performed and that the instrument is in the initial state. Besides this it also indicates that after some delay the instrument will enter automatically the 'normal mode' which is laid down in the program (see chapter 5.1.1).

A summary of the instrument status after power on is given in Table 5.1-1.

COMMAND	STATUS
Detector Status	all detectors off
TAC Slope	nominal
E-Calibration	off
T-Calibration	20 ns, off
USS Threshold Level	lower threshold level
MCP Power Supply	disabled, level 0
ADC Trigger	E + T
Execution of ML1 Commands	every 8^{th} period
Internal Heater	all heater off
Defl. Plate Voltage Mode	mode 1, DPPS off
Post Acc. Power Supply	15kV, MLDCMD:off, PLSCMD off
Auto. Step Reversal	FSR0, no step reversal
Data Compression	Code C (m = 4, 3)
Analog HV-Control	level 0
Correction for Emergency Timer	EMTC = 0
DV-Monitor	enabled
Special Test Mode	no special test mode
Emin for Threshold Measurement (AUTO CAL):	
Detector USS	channel: 1
" MSS1	" : 10
" MSS2	" : 10
" MSS3	" : 10
DPU Mode	mode 0 (normal)
Calibration Command	autom.calibr. once per week
Sun Gating of R2	45
PHA Priority Mode	normal
T-Offset Correction	0 channel
Sectoring of ACP/ACA-Rates	S1 = sector 4 (sun sector)
Sector Adjustment	SPS = sector 6; FA = 11.25
Sectoring of ME, MR, BR and PHA-Words	events from all sectors
DV-Code Command	DVC = $(00)_{hex}$

Tab. 5.1-1: Status of SWICS after Power On (Save Mode)

SPS = Sun Pulse Sector, FA = Fine Adjustment

5.1.1 Delayed Automatic High Voltage Switch On

If no m1-command is received during 175104 spins (175104 * 12 s = 48.64 hours) the DPU will enter the normal operation mode. The command status is changed as follows:

Detector Status	:	all detectors on
MCP Power Supply	:	enabled, level 2
Defl. Plate Power Supply	:	on
Post Acc. Power Supply	:	enabled, V_a = 15 kV
Analog HV-Control	:	level 7

The post acceleration voltage V_a is kept on 15 kV for at least 256 spins (256 * 12 s = 51.2 minutes). Then, provided that no m1-command was received, the post acceleration voltage is increased to 30 kV.

5.2 Telemetry Modes

From the S/C there are two static signals (Mode Line 1 and Mode Line 2) delivered to the DPU to identify the telemetry aquisition rate. Table 5.2-1 shows the relation between the telemetry mode and data accumulation time.

MD Line 2	MD Line 1	Bit Rate in bps	Telem. Mode	Spins per Period	Frames per EDB
0	0	128	STMC	4	6
0	1	256	STMB	2	6
1	0	512	STMA	1	6
1	1	1024	TRM	1	12

Tab. 5.2-1: Telemetry Modes

TRM = tracking mode
STMA = storage mode A
STMB = storage mode B
STMC = storage mode C

5.3 Modes of the SWICS Deflection System

Commands :	ML2.A	(voltage mode, step reversal)
	ML3.A	(DPU-Mode)
HK-words :	HK2.11	(DPUCD3)
	HK2.12	(DPUCD4)
	HK1.7	(STATUS)
Software :	subroutine "DVCON"	

5.3.1 Deflection Voltage Modes

A. DPU-Mode 0 or 2 (normal DV-Mode)

The deflection voltage is automatically stepped down or up (after step reversal) according to the mode selected by ml-command ML2.A (see Fig. 5.3-2 and Table 5.3-1).

DV-Mode	first step	last step	step width
0	127	1	2
1	138	12	2
2	64	1	1
3	75	12	1

Tab. 5.3-1: SWICS DV-Modes while DPU-Mode 0 or 2

In DPU-Mode 2 there will be no more data accumulation in the Counting Memory (ME, MR, BR) after step reversal. DPU-Mode 1 0 ? is considered as the normal mode.

B. DPU-Mode 1 (Test Mode)

At the beginning of each period the deflection voltage is set according to ml-command ML3.6 (DVC-Command). The bit assigment of DVC is shown in Fig. 5.3-1 and the step assigment in Tab. 5.3-2.

There is no automatic stepping in this mode.

C. DPU-Mode 3 (additional DV-Mode)

The deflection voltage is automatically stepped down or up (after step reversal). The step width is always 1. The highest voltage step can be selected by ml-command ML2.A. The stepping scheme is shown in Fig. 5.3-3 and Table 5.3-3.

DV-Mode	first step	last step	step width	HK-Info. (HK2.11)
1 or 3	138	75	1	DV-Mode 3
0 or 2	127	64	1	DV-Mode 2

Tab. 5.3-3 : SWICS DV-Modes while DPU-Mode 3

It should be noted, that in the DPU-Mode 3 the DPU does not care about bit 11 of ml-command ML2.A.

After step reversal data accumulation in the Counting Memory (ME, MR, BR) is continued (same as for DPU-Mode 0).

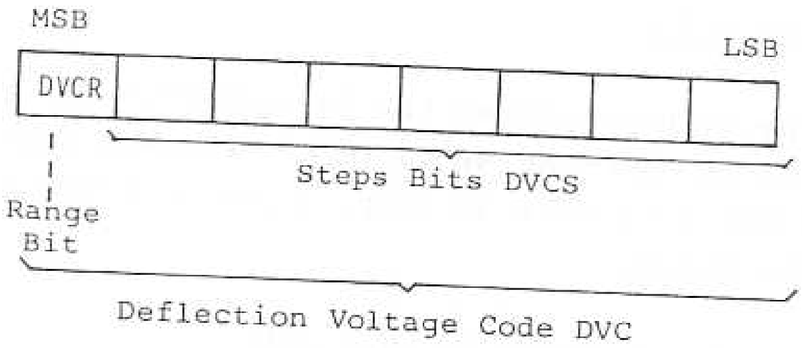


Fig. 5.3-1: Deflection Voltage Code DVC

Step Bits DVCS of DV-Code DVC LSB	Defl. Voltage Step DVS	
	Range Bit=0	Range Bit=1
~~1~~ 1 1 1 1 1 1 1	127	138
~~1~~ 1 1 1 1 1 1 0	126	137
~~1~~ 1 1 1 1 1 0 1	125	136
⋮	⋮	⋮
~~0~~ 0 0 0 0 0 1 1	3	14
~~0~~ 0 0 0 0 0 1 0	2	13
~~0~~ 0 0 0 0 0 0 1	1	12
~~0~~ 0 0 0 0 0 0 0	0	11

Tab. 5.3-2: Assignment of Step Numbers (DVS) to the binary Deflection Voltage Code DVC

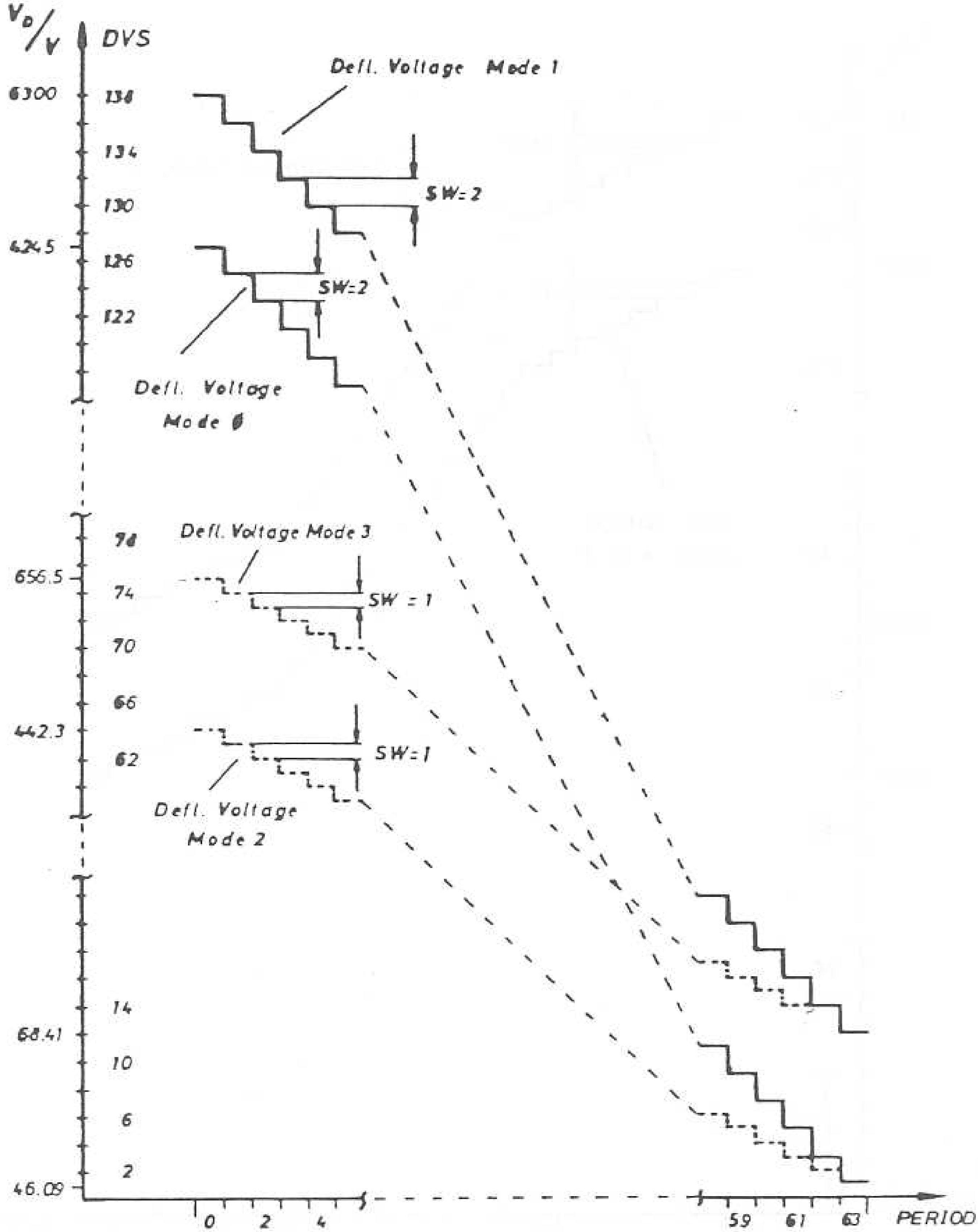


Fig. 5.3.-2 Deflection Voltage Modes (DPU MODE 0 or 2)
Deflection Voltage V_D during one voltage cycle (no step reversal)
SW = step width

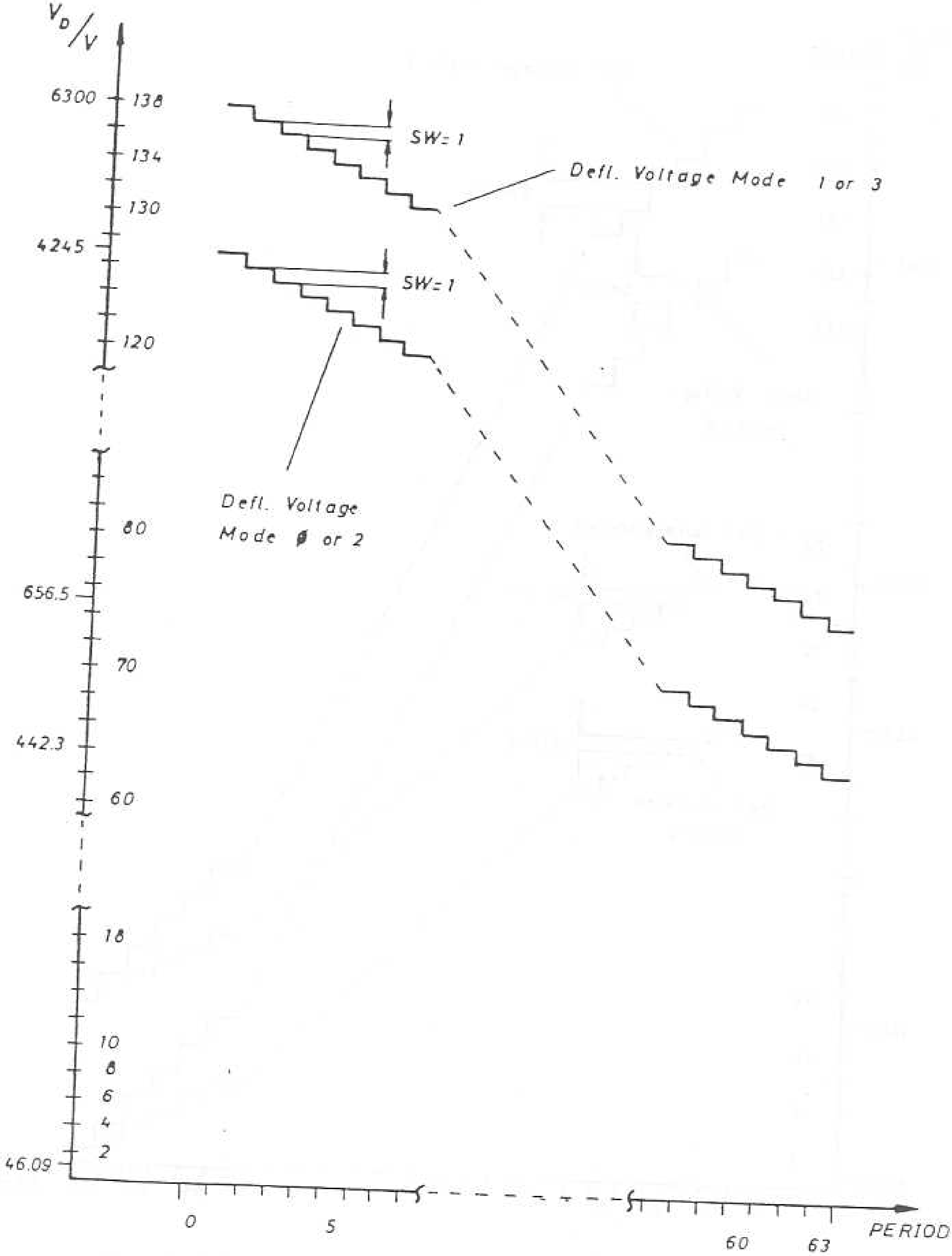


Fig. 5.3 - 3 Additional Deflection Voltage Modes (DPU MODE 3)
Deflection Voltage V_D during one voltage cycle (no step reversal)
SW = step width

5.3.2 Automatic Step Reversal

Command : ML2.A , Bit 3 ... 6

HK-word : HK1.0
HK2.12 (DPUCD4)

Software : subroutine "DVCON"

The step direction of the deflection voltage will be reversed if during one spin the front seda rate FSR is greater or equal to a value FSR_n that was selected by ml-command.

Step Reversal if: $FSR \geq FSR_n$ $(n = 0, 1, \ldots, 7)$

The possible values for FSR_n are shown in Tab. 5.3-3.

n	FSR_n
0	256
1	1024
2	4096
3	16384
4	65536
5	131072
6	262144
7	524288

Tab. 5.3-3: Selectable Front Seda Rates for the Automatic Step Reversal

During the voltage cycles n*64 (n = 0, 1, 2, 3) the automatic step reversal is disabled. Thus every 64^{th} voltage cycle (once within ≈ 14 hours if the instrument operates in the tracking mode or in the storage mode with 512 bps (STMA)) the deflection voltage is stepped through the complete range selected by telecommand.

5.4 Post Acceleration Voltages

Commands	:	pulse commands ML2.A ML2.0	(on/off) (range, on/off) (level)
HK-words	:	HK2.12 (DPUCD4) HK2.14 (DPUCD6)	
Software	:	subroutine "HVCON"	

To turn on the post acceleration power supply (PAPS) the pulse command PC1 (HV ON) and the appropriate ml-command (ML2.A) has to be sent. With ml-command ML2.A also the voltage range (15 kV or 30 kV) can be selected. The actual level of the post acceleration voltage V_a is determined by ml-command ML2.0. The possible values for V_a are listed in Tab. 5.4-1.

voltage Level (ML2.0)	15 kV - Range		30 kV - Range	
	V_a/kV	class. correct	V_a/kV	class. correct
0	7.5	no	10.0	no
1	11.1	"	17.5	yes
2	12.0	"	20.0	"
3	12.9	"	22.6	"
4	13.6	"	24.9	"
5	14.2	"	26.9	"
6	14.6	"	28.5	"
7	15.0	yes	30.0	"

Tab. 5.4-1: Post Acceleration Voltages of the SWICS Instrument

5.5 Calibration Modes

Commands	:	ML1.1	(E-Input)
		ML1.2	(T-Input)
		ML2.4	(Emin for Det. USS)
		ML2.5	(" " " MSS1)
		ML2.6	(" " " MSS2)
		ML2.7	(" " " MSS3)
		ML3.A	(Calibration Mode)
HK-words	:	HK1.3	(BUCD23)
		HK1.4	(BUCD45)
		HK1.7	(STATUS)
		HK2.7	(DPUCD8)
		HK2.8	(DPUCD0)
Software	:	routine	"CONTC"
		subroutines	"BUSRV", "DVCON"

5.5.1 Calibration by ml-command ML1

E-Input and T-Input for the calibration are selected by the respective ml-command (ML1.1 and ML1.2). The automatic calibration should be switched off.

5.5.2 Automatic Calibration

The automatic calibration sequence comprises 2*64=128 calibration steps. One calibration step is performed during one period. At the end of the automatic calibration sequence the DPU will go back to its previous configuration.

A. Automatic Calibration by Command

After sending the ml-command "AUTO CAL ON" (ML3.A) the DPU will start the automatic calibration sequence at the beginning of the next cycle. The calibration sequence is performed only one time.

B. Periodic Automatic Calibration

After sending the ml-command "Auto Cal Periodic" (ML3.A) the DPU will run the automatic calibration sequence once per week.

C. Automatic Calibration Sequence

Cal. Cycle 1: Linearity of Detectors

Linearity of Det.	USS	: period	0 ... 15	(16 steps)
" " "	MSS3	: "	16 ... 31	(16 steps)
" " "	MSS2	: "	32 ... 47	(16 steps)
" " "	MSS1	: "	48 ... 63	(16 steps)

Cal. Cycle 2: Threshold Measurement

Threshold of Det.	USS	: period	0 ... 23	(24 steps)
" " "	MSS3	: "	24 ... 31	(8 steps)
" " "	MSS2	: "	32 ... 39	(8 steps)
" " "	MSS1	: "	40 ... 47	(8 steps)
Linearity of Det.	MSS1	: period	48 ... 63	(16 steps)

While the automatic calibration sequence is performed, the ADC Trigger Condition is changed to CAL*(E+T).

During the linearity measurement the deflection voltage mode 1 (step 138 to 12) is used.
During the threshold measurement the deflection voltage is kept constant at the highest value (step 138).

In Tables 5.5-1 and 5.5-2 energy and time inputs are listed for all steps of the automatic calibration sequence.

Period	DVC (hex)	DVS	E-Input (channel)	T-Input channel	/ns	Detector
0	FF	138	9	102	20	USS
1	FD	136	25	307	60	
2	FB	134	41	512	100	
3	F9	132	57	716	140	
4	F7	130	73	102	20	
5	F5	128	89	307	60	
6	F3	126	105	512	100	
7	F1	124	121	716	140	
8	EF	122	137	102	20	
9	ED	120	153	307	60	
10	EB	118	169	512	100	
11	E9	116	185	716	140	
12	E7	114	201	102	20	
13	E5	112	217	307	60	
14	E3	110	233	512	100	
15	E1	108	249	716	140	
16	DF	106	9	102	20	MSS 3
17	DD	104	25	307	60	
18	DB	102	41	512	100	
19	D9	100	57	716	140	
20	D7	98	73	102	20	
21	D5	96	89	307	60	
22	D3	94	105	512	100	
23	D1	92	121	716	140	
24	CF	90	137	102	20	
25	CD	88	153	307	60	
26	CB	86	169	512	100	
27	C9	84	185	716	140	
28	C7	82	201	102	20	
29	C5	80	217	307	60	
30	C3	78	233	512	100	
31	C1	76	249	716	140	

Tab. 5.5-1a: Calibration Cycle 1
Linearity of Detectors USS and MSS 3

Period	DVC (hex)	DVS	E-Input (channel)	T-Input channel	/ns	Detector
32	BF	74	9	102	20	MSS 2
33	BD	72	25	307	60	
34	BB	70	41	512	100	
35	B9	68	57	716	140	
36	B7	66	73	102	20	
37	B5	64	89	307	60	
38	B3	62	105	512	100	
39	B1	60	121	716	140	
40	AF	58	137	102	20	
41	AD	56	153	307	60	
42	AB	54	169	512	100	
43	A9	52	185	716	140	
44	A7	50	201	102	20	
45	A5	48	217	307	60	
46	A3	46	233	512	100	
47	A1	44	249	716	140	
48	9F	42	9	102	20	MSS 1
49	9D	40	25	307	60	
50	9B	38	41	512	100	
51	99	36	57	716	140	
52	97	34	73	102	20	
53	95	32	89	307	60	
54	93	30	105	512	100	
55	91	28	121	716	140	
56	8F	26	137	102	20	
57	8D	24	153	307	60	
58	8B	22	169	512	100	
59	89	20	185	716	140	
60	87	18	201	102	20	
61	85	16	217	307	60	
62	83	14	233	512	100	
63	81	12	249	716	140	

Tab. 5.5-1b: Calibration Cycle 1
Linearity of Detectors MSS 2 and MSS 1

Period	DVC (hex)	DVS	E-Input (channel)	T-Input channel	T-Input /ns	Detector
0	FF	138	1	716	140	USS
1			3			
2			5			
3			7			
4			9			
5			11			
6			13			
7			15			
8			17			
9			19			
10			21			
11			23			
12			25			
13			27			
14			29			
15			31			
16			33			
17			35			
18			37			
19			39			
20			41			
21			43			
22			45			
23			47			
24			10			MSS 3
25			12			
26			14			
27			16			
28			18			
29			20			
30			22			
31	FF	138	24	716	140	

Tab. 5.5-2a: Calibration Cycle 2

Threshold of Det. USS (Emin = channel 1)
Threshold of Det. MSS 3 (Emin = channel 10)

Period	DVC (hex)	DVS	E-Input (channel)	T-Input channel	T-Input /ns	Detector
32	FF	138	10	716	140	MSS 2
33			12			
34			14			
35			16			
36			18			
37			20			
38			22			
39			24			
40			10			MSS 1
41			12			
42			14			
43			16			
44			18			
45			20			
46			22			
47	FF	138	24	716	140	
48	FF	138	9	102	20	MSS 1
49	FD	136	25	307	60	
50	FB	134	41	512	100	
51	F9	132	57	716	140	
52	F7	130	73	102	20	
53	F5	128	89	307	60	
54	F3	126	105	512	100	
55	F1	124	121	716	140	
56	EF	122	137	102	20	
57	ED	120	153	307	60	
58	EB	118	169	512	100	
59	E9	116	185	716	140	
60	E7	114	201	102	20	
61	E5	112	217	307	60	
62	E3	110	233	512	100	
63	E1	108	249	716	140	

Tab. 5.5-2b: Calibration Cycle 2

Threshold of Det. MSS 2 (Emin = channel 10)
" " " MSS 1 (Emin = channel 10)
Linearity " " MSS 1 (high DV-steps)

5.6 Special Test Modes

Command : ML2.3
HK-word : HK2.14 (DPUCD6)
Software : subroutines "BBLSRV" and "CLCON"

5.6.1 Classification Test

After sending the ml-command "CLASS TST" (ML2.3) the DPU will start the classification test at the beginning of the next cycle. The test comprises 64 steps and will be performed within one cycle.

The DPU utilizes the in-flight calibration capability of the analog electronics and the time offset correction to provide 64 selected E-T-pairs to the classification unit. The necessary E- and T-inputs for the analog electronics and the T-offset are listed in Table 5.6-1. The time offset correction word TOC which is determined by ml-command ML3.0 is not changed by the classification test. The time of flight T that is used by the classification unit has the following value: T = T-input + T-offset + TOC.

Period	E-Input channel	T-Input /ns	T-Input channel	T-Offset channel
0	0	140	716	64
1	128	100	512	-112
2	25	60	307	- 22
3	30	20	102	50
4	0	140	716	64
5	100	100	512	-112
6	25	60	307	- 22
7	23	20	102	50
8	0	140	716	64
9	100	100	512	-112
10	21	60	307	- 22
11	0	20	102	50
12	0	140	716	64
13	51	100	512	-112
14	119	60	307	- 22
15	19	20	102	50
16	59	100	512	-112
17	100	100	512	-112
18	181	60	307	- 22
19	67	100	512	-112
20	45	100	512	-112
21	100	100	512	-112
22	42	60	307	- 22
23	59	100	512	-112
24	67	100	512	-112
25	0	100	512	-112
26	85	60	307	- 22
27	100	100	512	-112
28	114	100	512	-112
29	51	100	512	-112
30	25	60	307	- 22
31	67	100	512	-112

Tab. 5.6-1a: E- and T-Input for Automatic Classification Test

Period	E-Input channel	T-Input /ns	T-Input channel	T-Offset channel
32	59	100	512	-112
33	0	100	512	-112
34	66	60	307	- 22
35	67	100	512	-112
36	51	100	512	-112
37	45	100	512	-112
38	30	60	307	- 22
39	100	100	512	-112
40	38	100	512	-112
41	67	100	512	-112
42	25	60	307	- 22
43	24	100	512	-112
44	59	100	512	-112
45	28	100	512	-112
46	21	60	307	- 22
47	100	100	512	-112
48	45	100	512	-112
49	33	100	512	-112
50	18	60	307	- 22
51	67	100	512	-112
52	38	100	512	-112
53	128	100	512	-112
54	18	60	307	- 22
55	59	100	512	-112
56	24	100	512	-112
57	45	100	512	-112
58	18	60	307	- 22
59	67	100	512	-112
60	51	100	512	-112
61	28	100	512	-112
62	16	60	307	- 22
63	59	100	512	-112

Tab. 5.6-1b: E- and T-Input for Automatic Classification Test

5.7 Emergency Modes

5.7.1 No Spin Rate

If the spin rate fails, no more sector change interrupts (L2-interrupts) will be generated. Therefore the DPU will stop all measurements and only zero frames (these are frames that do not belong to an EDB, all 11 bytes are zero) are transmitted to the telemetry. After 128 such zero frames are transmitted in series, the DPU will automatically enter the emergency mode No Spin Rate . In this mode the measuring program is controlled by the telemetry interrupts (L1-interrupts) and an internal software timer (Fig. 5.7-1).

The basic time grid is given by the telemtry interrupts. A telemetry interrupt is created by the leading edge of the sampling signal for the last word of each EDB frame. The internal timer devides the time between two telemetry interrupts into 2, 4, 8 or 16 equal intervals (dependend on telemetry mode). The lenght of these intervals is approximately 500 ms - EMTC * 2 ms, where EMTC is an integer between 0 and 15. After power on reset EMTC equals 0. It's value can be changed by memory load command ML2.1.

While in the emergency mode, the DPU operates almost in the same way as in one of the normal modes. The main differences to the normal mode are:

- The Sun Pulse can not be recognized by the DPU. The orientation of the sectoring can be changed by memory load command ML3.5.

- The power consumption will be higher because the power saving routine is executed only after the timer interrupt which is followed by a telemetry interrupt.

- The detector rates (FSR, DCR, etc.) are read every 500 ms (every 375 ms if not emergency mode).

The housekeeping word HK2.8 indicates whether the DPU was in the emergency mode 'No Spin Rate' at the beginning of period 8 * n where n = 0, 1, ... , 7. The error bit 'No Spin Rate' of HK1.6 (ERROR) indicates that the DPU was in the respective emergency mode at least for a short moment during the monitoring interval of the error word.

The DPU will leave this emergency mode automatically if a sector change interrupt (L2-interrupt) is detected.

5.7.2 No Frame Pulse

If there is no frame pulse for about 15 periods the DPU will automatically enter the emergency mod 'No Frame Pulse' . During these 15 periods only zero frames are transmitted. In this emergency mode, which is indicated by housekeeping word HK2.8 (DPUCDO), the DPU works in the same way as in any other mode.

To leave this emergency mode the appropriate memory load command ML2.2 has to be sent.

5.7.3 No Sun Pulse

If no sun pulse is detected during one spin the respective error bit of HK1.6 (ERROR) will be set. The operation of the DPU is not affected.

The orientation of the sectoring can be changed by memory load command ML3.5. This command will turn all sectors by n * 45 (n = 0, 1, ... , 7) in anticlockwise direction (the sector counter is set from 0 to n).

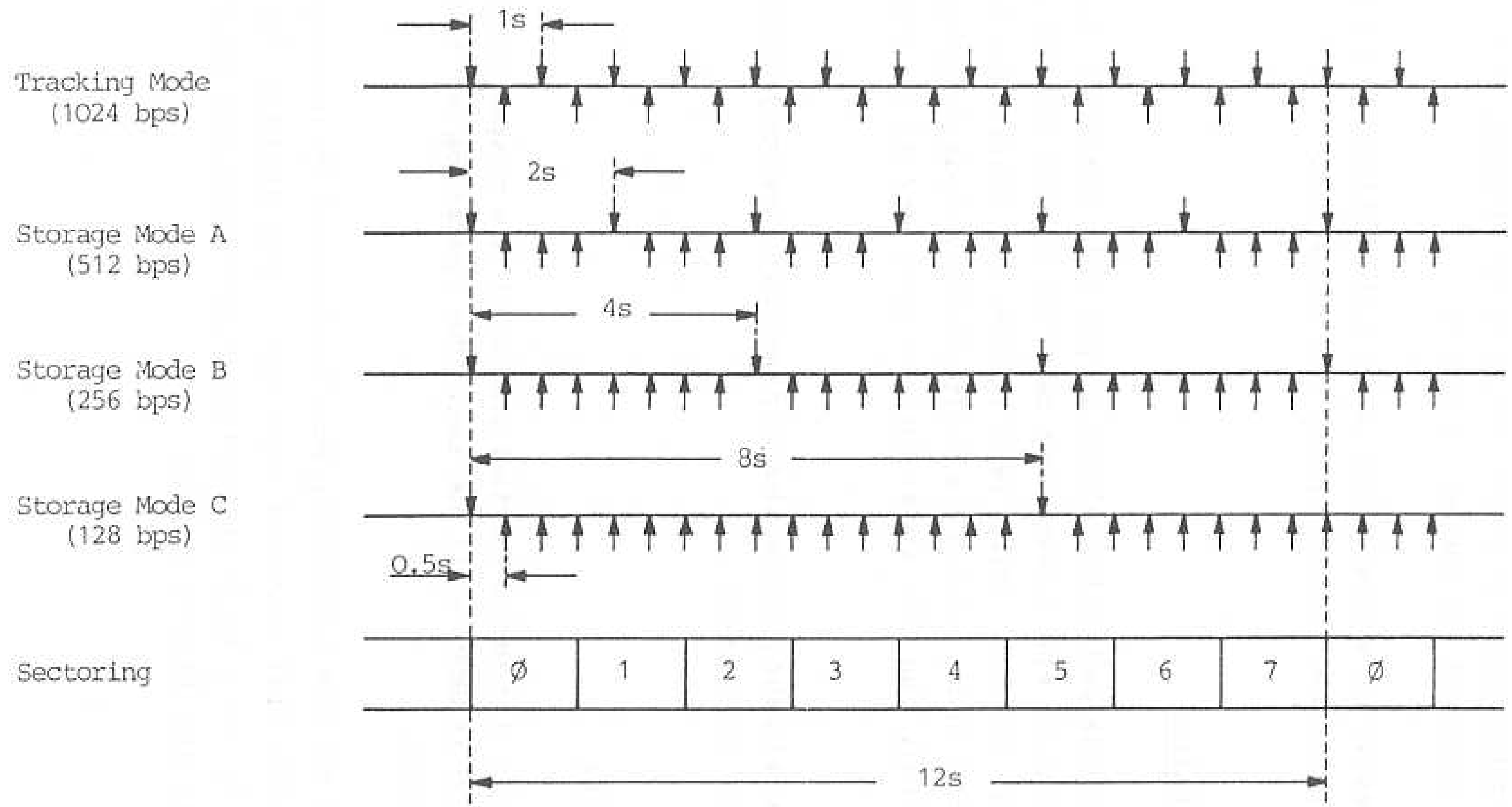
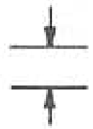


Fig. 5.7-1: SWICS Timing during Emergency Mode "No Spin Rate";
assumed is nominal telemetry clock



Telemetry Interrupt

Timer Interrupt (software)

6. Classification

- real-time classification of E-T events up to 20 kHz event rate

- an E-T event will be classified if
  1. 10 clock pulses have been received
  2. a minimum gap of 2 clock pulses has been recognized

- The classification procedure includes
  - computation of NM and NQ
  - allotment of one fine bin address (ME), one basic rate address (BR) and one co~~u~~arse bin address (MR)

  For most of the E-T events the accuracy of the computed NM and NQ is ± 1 grid element of the NM-NQ matrix.

- Correct classification for the following post acceleration voltages : V_a = 0, 15, 17.5 , 20, 22.6 , 24.9, 26.9, 28.5 and 30 kV.

  For V_a = 0 kV classification is limited to deflection voltage steps DVS $\geq$ 100.

A comprehensive description of the classification is given in /1/ and /2/.

6.1 Equations used to generate Look-up Tables

The following equations are valid for both FM and FS.

$$\frac{m}{q} = C1 * \left(\frac{E}{q} + V_a - 1.5 \right) * ToF^2$$

$C1 = 1.9159 * 10^{-5}$

E/q = keV/e value of a given voltage step

V_a = post acceleration voltage in kV

ToF = time of flight in nanoseconds

$$\ln(m) = A1 + A2*X + A3*Y + A4*X*Y + A5*X^2 + A6*Y^3$$

X = ln (measured energy in keV)

Y = ln (time of flight in nanoseconds)

A1 = 5.81090

A2 = -1.50052

A3 = -3.01352

A4 = 0.471113

A5 = 0.0804588

A6 = 0.0731559

lower bounds of NM, NQ:

$m = 0.69 * 1.2^{(NM-1)}$ $\qquad$ $\frac{m}{q} = 0.82 * 1.03^{(NQ-1)}$

main ch: $\frac{E}{q} = \overset{a}{0.4271} * \overset{b}{1.036547}^S$ $\qquad$ $S = \frac{1}{\log b}\left(\log E/q - \log a\right)$

$T = 1023 * \frac{ToF}{200\ ns}$ $\qquad$ $S = 641.5\left(\log E/q + 0.3695\right)$

$$E = 255 * \frac{E_{meas}}{610.78\ keV}$$

aux ch: $\frac{E}{q} = 0.1029 * 1.036547^S$

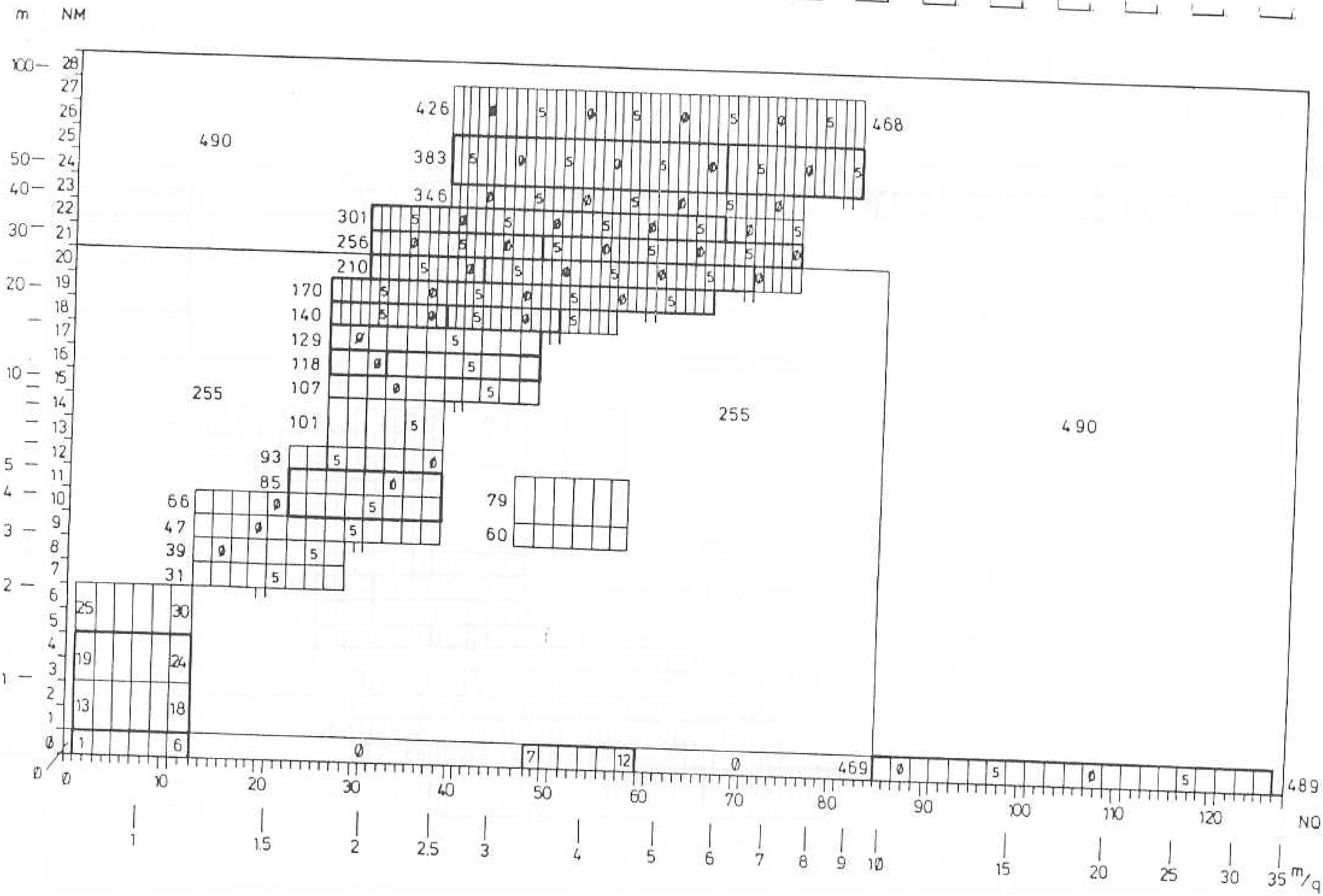


Fig. 6.1 : Allotment of the NM-NQ Matrix

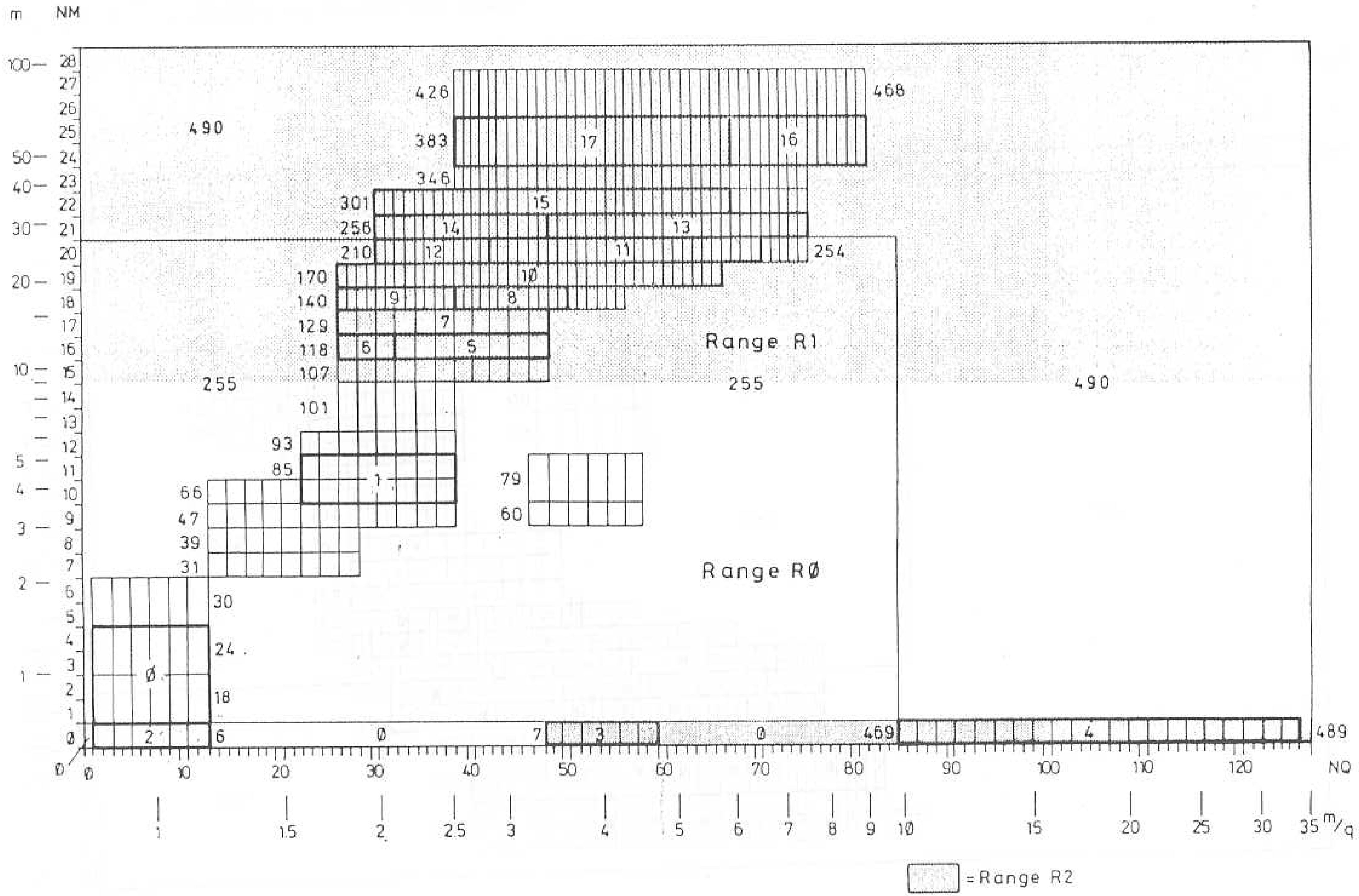


Fig. 6.2 · Matrix Rates and Priority Ranges

Matrix Rate	Bin	Particle	Charge [e]
0	491	Proton	
1	492	$^{4}He^{+2}$	
2	493	"Mass Zero" Proton	
3	494	"Mass Zero" Helium	
4	495	"Mass Zero" M/Q 9.872 to 36.2	
5	496	C	4, 5
6	497		6
7	498	N	5, 6, 7
8	499	O	5, 6
9	500		7, 8
10	501	Ne	4 to 10
11	502	Mg	4 to 10
12	503	Mg	9 to 11
13	504	Si	4 to 8
14	505		9 to 12
15	506	S	6 to 14
16	507	Fe	7 to 9
17	508		10 to 14

Basic Rate	Bin	Range	
BR Ø	509	R Ø	
BR 1	510	R 1	
BR 2	511	R 2	

Fig. 6.3: Bin Assignment of Matrix Rates and Basic Rates

References

/1/ F. Gliem, H.Dinse, W.Rieck, "Real Time Classification of Solar Wind Ions", Zeitschrift für Flugwissenschaften und Weltraumforschung, vol. 7, May/June 1983

/2/ F.Gliem, H.Dinse, W. Rieck, "The Classification of Ions in the ISPM-SWICS Instrument", May 1985, unpublished

APPENDIX

A1 Memory Load Command Description

Exp Code	S/C Code	Address: Lines	Address: Octal	Verification
ML1	Z007	N/A	113	GLG DS 1

Note: MSB is shifted out first to experiment

Bit Assignment	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
Lin Ch MSS 1 ON	0	0	0	0	0	1										
Lin Ch MSS 1 OFF	0	0	0	0	0	0										
Lin Ch MSS 2 ON	0	0	0	0	0		1									
Lin Ch MSS 2 OFF	0	0	0	0	0		0									
Lin Ch MSS 3 ON	0	0	0	0	0			1								
Lin Ch MSS 3 OFF	0	0	0	0	0			0								
Lin Ch USS ON	0	0	0	0	0				1							
Lin Ch USS OFF	0	0	0	0	0				0							
TAC Slope -10%	0	0	C	0	0					X	0	1	0			
" " -5%	0	0	0	0	0					X	0	1	1			
" " Nominal	0	0	0	0	0					X	0	0	0			
" " +5%	0	0	0	0	0					X	0	0	1			
" " +10%	0	0	0	0	0					X	1	1	0			
E Cal Lowest Ampl.	0	0	0	0	1	0	0	0	0	0	0	0	1			
E Cal Highest Ampl.	0	0	0	0	1	1	1	1	1	1	1	1	1			
E Cal OFF	0	0	0	0	1	0	0	0	0	0	0	0	0			
T Cal t = 20nS	0	0	0	1	0	0	0		1							
" " t = 60nS	0	0	0	1	0	0	1		1							
" " t = 100nS	0	0	0	1	0	1	0		1							
" " t = 140nS	0	0	0	1	0	1	1		1							
" " OFF	0	0	0	1	0	X	X		0							
MCP PS Level 0 (Off)	0	0	0	1	0					1	0	0	0			
" " " 1 (Vmin)	0	0	0	1	0					1	0	0	1			
" " " 2	0	0	0	1	0					1	0	1	0			
" " " 3	0	0	0	1	0					1	0	1	1			
" " " 4	0	0	0	1	0					1	1	0	0			
" " " 5	0	0	0	1	0					1	1	0	1			
" " " 6	0	0	0	1	0					1	1	1	0			
" " " 7 (Vmax)	0	0	0	1	0					1	1	1	1			
MCP PS Disabled	0	0	0	1	0					0	X	X	X			
Higher Threshold Levels	0	0	0	1	0			1								
Lower " "	0	0	0	1	0			0								
	IDENTIFIER	ADDRESS				COMMAND				COMMAND						

Cont/

A1 Memory Load Command Description

Exp Code	S/C Code	Address		Verification
		Lines	Octal	
ML1 (cont)	Z007	N/A	113	GLG DS 1

Note: MSB is shifted out first to experiment

Bit Assignment	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
ADC Trigger E + T	0	0	0	1	1	0	0	0	0							
" " E . T	0	0	0	1	1	0	1	0	0							
" " E	0	0	0	1	1	1	0	0	0							
" " T	0	0	0	1	1	1	1	0	0							
CAL ADC Trigger E + T	0	0	0	1	1	0	0	1	0							
" " " E . T	0	0	0	1	1	0	1	1	0							
" " " E	0	0	0	1	1	1	0	1	0							
" " " T	0	0	0	1	1	1	1	1	0							
Trigger Inhibit	0	0	0	1	1	X	X	X	1							
Subfr. Seq. Hold	0	0	0	1	1					0	0					
" " Increment	0	0	0	1	1					0	1					
" " Reset	0	0	0	1	1					1	0					
No EVD Transf.	0	0	0	1	1							0	0			
Trans. Subseq. to Rec	0	0	0	1	1							1	1			
Cmd Exec. Every 8th Period	0	X	X	X	X									0		
" " at Cycle Start	0	X	X	X	X									1		
	IDENTIFIER	ADDRESS				COMMAND				COMMAND						

A1 Memory Load Command Description

Exp Code	S/C Code	Address		Verification
		Lines	Octal	
ML2	Z008	N/A	153	GLG DS 1

Note: MSB is shifted out first to experiment

Bit Assignment	MSB	Bit 2^n														LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Internal Heater 1 ON	1	1														
" " 1 OFF	1	0														
" " 2 ON	1		1													
" " 2 OFF	1		0													
" " 3 ON	1			1												
" " 3 OFF	1			0												
Defl. Pl. Volt. Mode Ø	1				0	0	1									
" " " " 1	1				0	1	1									
" " " " 2	1				1	0	1									
" " " " 3	1				1	1	1									
Defl. Pl. PS OFF	1				X	X	0									
-30kV ON	1							1	1							
-15kV ON	1							0	1							
-30kV PS OFF	1							X	0							
Step Rev at FSR 0	1									0	0	0	1			
" " " " 1	1									0	0	1	1			
" " " " 2	1									0	1	0	1			
" " " " 3	1									0	1	1	1			
" " " " 4	1									1	0	0	1			
" " " " 5	1									1	0	1	1			
" " " " 6	1									1	1	0	1			
" " " " 7	1									1	1	1	1			
No Auto Step Rev	1									X	X	X	0			
Data Comp A (m = 4)	1													0		
" " C (m = 4, 3)	1													1		

Continued/

IDENTIFIER

Note : The -30kV/-15kV power supply will be enabled only when the pulse command "-30kV ON" has been sent and the relevant HV On ML Cmd bit has been set. Disabling of the -30kV/-15kV power supply will occur either by pulse command "-30kV OFF or ML Cmd "-30kV PS OFF".

A1 Memory Load Command Description

Exp Code	S/C Code	Address		Verification
		Lines	Octal	
ML2 (cont)	Z008	N/A	153	GLG DS1

Note: MSB is shifted out first to experiment

Bit Assignment	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
Analog HV Control																
Level 0	0	0	0	0	0	X	X	X	X	0	0	0	X			
" 1	0	0	0	0	0	X	X	X	X	0	0	1	X			
" 2	0	0	0	0	0	X	X	X	X	0	1	0	X			
" 3	0	0	0	0	0	X	X	X	X	0	1	1	X			
" 4	0	0	0	0	0	X	X	X	X	1	0	0	X			
" 5	0	0	0	0	0	X	X	X	X	1	0	1	X			
" 6	0	0	0	0	0	X	X	X	X	1	1	0	X			
" 7	0	0	0	0	0	X	X	X	X	1	1	1	X			
Correction for Em. Timer	0	0	0	0	1	EMTC				EMTC						
Do not care	0	0	0	1	0	0										
Leave Em. Mode "NO FRM PLS"	0	0	0	1	0	1										
DV Monitor Disabled	0	0	0	1	0		0									
" " Enabled	0	0	0	1	0		1									
Special Test Modes:																
Mode 0: No Special Test	0	0	0	1	1	0	0	0	0	0	0	0	0			
Mode 1: Clsfction Test	0	0	0	1	1	0	1	1	0	1	0	0	1			
Mode 2: ML1 Exec Evry Prd	0	0	0	1	1	1	0	1	1	0	1	0	0			
Emin for AUTO CAL:																
Det USS Lowest Ampl.	0	0	1	0	0	0	0	0	0	0	0	0	1			
" " Highest "	0	0	1	0	0	1	1	1	0	1	0	0	0			
Det MSS1 Lowest Ampl.	0	0	1	0	1	0	0	0	0	0	0	0	1			
" " Highest "	0	0	1	0	1	1	1	1	1	0	0	0	0			
" MSS2 Lowest "	0	0	1	1	0	0	0	0	0	0	0	0	1			
" " Highest "	0	0	1	1	0	1	1	1	1	0	0	0	0			
" MSS3 Lowest "	0	0	1	1	1	0	0	0	0	0	0	0	1			
" " Highest "	0	0	1	1	1	1	1	1	1	0	0	0	0			

IDENTIFIER ADDRESS

A1 <u>Memory Load Command Description</u>

Exp Code	S/C Code	Address Lines	Address Octal	Verification
ML3	Z009	N/A	123	GLG DS 1

Note: MSB is shifted out <u>first</u> to experiment

Bit Assignment	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
DPU MODE Ø (Normal)	1	0	0													
DPU MODE 1 (Test)	1	0	1													
DPU MODE 2	1	1	0													
DPU MODE 3	1	1	1													
Auto Cal (1 x per week)	1			0	X											
Auto Cal ON	1			1	1											
Auto Cal OFF	1			1	0											
Sun Gating of R2 0°	1					0	0	1								
" " " " 45°	1					0	1	1								
" " " " 135°	1					1	0	1								
" " " " 225°	1					1	1	1								
R2 Disabled	1					X	1	0								
R2 and R1 Disabled	1					X	0	0								
Normal PHA Pty Mode	1								0							
Rotating PHA Pty Mode	1								1							
T-Offset Corr. High Val.	0	0	0	0	0	0	1	1	1	1	1	1	1			
" " Low Val	0	0	0	0	0	1	0	0	0	0	0	0	0			
ACP/ACA Rates frm Sctr 7	0	0	0	0	1	1										
" " " " " 6	0	0	0	0	1		1									
" " " " " 5	0	0	0	0	1			1								
" " " " " 4	0	0	0	0	1				1							
" " " " " 3	0	0	0	0	1					1						
" " " " " 2	0	0	0	0	1						1					
" " " " " 1	0	0	0	0	1							1				
" " " " " 0	0	0	0	0	1								1			
Sector Adjustment	0	0	0	1	0	X	FA				SPS					
Start Next Cycle	0	0	0	1	1	0	1	0	1	0	0	1	0			

IDENTIFIER (bit 15) ADDRESS (bits 14–11)

SPS = Sun Pulse Sector

FA = Fine Adjustment

Continued/

A1 Memory Load Command Description

Exp Code	S/C Code	Address		Verification
		Lines	Octal	
ML3 (cont)	Z009	N/A	123	GLG DS 1

Note: MSB is shifted out first to experiment

Bit Assignment	MSB	Bit 2^n														LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sectoring of ME,MR,BR,																
and PHA Words:																
Data from Sector 7	0	0	1	0	0	1										
" " " 6	0	0	1	0	0		1									
" " " 5	0	0	1	0	0			1								
" " " 4	0	0	1	0	0				1							
" " " 3	0	0	1	0	0					1						
" " " 2	0	0	1	0	0						1					
" " " 1	0	0	1	0	0							1				
" " " 0	0	0	1	0	0								1			
Sector Adjustment if no																
Sun Pulse:																
Sectoring changed by 0°	0	0	1	0	1	1	1	0	0	0	0	0	0			
" " " 45°	0	0	1	0	1	1	1	0	0	0	0	0	1			
" " " 90°	0	0	1	0	1	1	1	0	0	0	0	1	0			
" " " 135°	0	0	1	0	1	1	1	0	0	0	0	1	1			
" " " 180°	0	0	1	0	1	1	1	0	0	0	1	0	0			
" " " 225°	0	0	1	0	1	1	1	0	0	0	1	0	1			
" " " 270°	0	0	1	0	1	1	1	0	0	0	1	1	0			
" " " 315°	0	0	1	0	1	1	1	0	0	0	1	1	1			
DV-Code	0	0	1	1	0	DV - CODE										

IDENTIFIER (bit 15) ADDRESS (bits 14–11)

A2 HK-WORD DESCRIPTION

HK-Word : HK1.0

subcom. state : X000

Bit Assignment	MSB	Bit 2^n						LSB
	7	6	5	4	3	2	1	0
NO STEP REVERSAL	0							
AUTOMATIC STEP REVERSAL	1							
DATA COMPRESSION A(m=4)		0						
DATA COMPRESSION C(m=4,3)		1						
PERIOD COUNTER (PCH)			PC5	PC4				
DEFL. VOLTAGE CODE (DVH)					DV7	DV6	DV5	DV4
m = Mantissa								
PC <n> = Bit n of Period Counter								
DV <n> = Bit n of Defl. Voltage Code								

(X = don't care)

A2 HK-WORD DESCRIPTION

HK-Word : HK1.2 (BUCD1, BUCD0)
subcom. state : X010

Bit Assignment	MSB 7	6	5	4	3	2	1	LSB 0
BUCD0: Detector Status								
LIN. CHANNEL MSS1 ON					0			
" " " OFF					1			
" " MSS2 ON						0		
" " " OFF						1		
" " MSS3 ON							0	
" " " OFF							1	
" " USS ON								1
" " " OFF								0
BUCD1: TAC Gain Adjust.								
TAC SLOPE: -10%	1	0	1	0				
" " : - 5%	1	0	1	1				
" " : NOMINAL	1	0	0	0				
" " : + 5%	1	0	0	1				
" " : +10%	1	1	1	0				

(X = don't care)

A2 HK-WORD DESCRIPTION

HK-Word : HK1.3 (BUCD2, BUCD3)

subcom. state : X011

Bit Assignment	MSB	Bit 2^n						LSB
	7	6	5	4	3	2	1	0
BUCD23: E Calibration								
Lowest Ampl. ($E \approx 2.4$keV)	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
Highest Ampl.($E \approx 610.8$keV)	1	1	1	1	1	1	1	1
E CAL OFF	0	0	0	0	0	0	0	0

(X = don't care)

A2 HK-WORD DESCRIPTION

HK-Word : HK1.4 (BUCD4, BUCD5)

subcom. state : X100

Bit Assignment	MSB	Bit 2^n						LSB
	7	6	5	4	3	2	1	0
BUCD4: T Calibration								
t = 20 ns	0	0		1				
t = 60 ns	0	1		1				
t = 100 ns	1	0		1				
t = 140 ns	1	1		1				
T CAL OFF	X	X		0				
LOWER USS THRESH. LEVELS			0					
HIGHER " " "			1					
BUCD5: MCP Bias Supply								
MCP PS LEVEL 0 (OFF)					1	0	0	0
" " " 1 (Vmin)					1	0	0	1
" " " 2					1	0	1	0
" " " 3					1	0	1	1
" " " 4					1	1	0	0
" " " 5					1	1	0	1
" " " 6					1	1	1	0
" " " 7 (Vmax)					1	1	1	1
" " DISABLED					0	X	X	X

(X = don't care)

A2 HK-WORD DESCRIPTION

HK-Word : HK1.5 (BUCD6, BUCD7)

subcom. state : X101

Bit Assignment	MSB	Bit 2^n						LSB
	7	6	5	4	3	2	1	0
BUCD6: ADC Trigger								
EVENT ANALYSIS ON E+T	0	0	0	0				
" " " E T	0	1	0	0				
" " " E	1	0	0	0				
" " " T	1	1	0	0				
" " " CAL(E+T)	0	0	1	0				
" " " CAL E T	0	1	1	0				
" " " CAL E	1	0	1	0				
" " " CAL T	1	1	1	0				
" " INHIBITED	X	X	X	1				
BUCD7: Subframe Sequence								
HOLD SUBFR.SEQU.COUNTER					0	0		
INCREM. " " "					0	1		
RESET " " "					1	0		
NO EVENT DATA TRANSFER							0	0
EVENT DATA TRANSFER SUB-SEQU. TO CMD RECEPTION							1	1

(X = don't care)

A2 HK-WORD DESCRIPTION

HK-Word : HK1.6 (ERROR)
subcom. state : X110

Bit Assignment	MSB 7	6	5	4	3	2	1	LSB 0
	Bit 2^n							
INTERRUPT ERROR 1	1							
INTERRUPT ERROR 2		1						
NO BBL-HK-IDENTIFIER			1					
NO BBL-SYNC-WORD				1				
NO SPIN RATE					1			
ML ADDRESS WRONG						1		
SUN PLS NOT WITHIN SPS							1	
NO SUN PLS								1

A2 HK-WORD DESCRIPTION

HK-Word : HK1.7 (DPU-STATUS)

subcom. state : X111

Bit Assignment	MSB	Bit 2^n						LSB
	7	6	5	4	3	2	1	0
Telemetry Mode:								
STORAGE MODE C (128bpc)	0	0						
" " B (256bpc)	0	1						
" " A (512bpc)	1	0						
TRACKING MODE (1024bpc)	1	1						
Calibration Mode:								
NO CALIBRATION			0	0				
CAL. CYCLE 1 } AUTOMATIC			0	1				
CAL. CYCLE 2 } CALIBR.			1	0				
CALIBRATION BY ML1 CMD			1	1				
EXEC. ML1 EVERY 8^{th} PERIOD					0			
" " " CYCLE START					1			
NO PLS CMD OR ML CMD ACCEP						0		
PLS CMD OR ML CMD ACCEPTED						1		
DPU MODE 0(NORMAL)							0	0
" " 1(NO DV STEPPING)							0	1
" " 2(NO ACCUM. AFTER STEP REVERSAL)							1	0
" " 3(ADDITIONAL DV-MODE)							1	1

A2 HK-WORD DESCRIPTION

HK-Word : HK2.7 (DPUCD8)

subcom. state : 0111

Bit Assignment	MSB 7	Bit 2^n 6	5	4	3	2	1	LSB 0
Emin for threshold measurement during AUTOMATIC CALIBRATION								
Emin (6 l.s. bits of the 8 bit command):	E5	E4	E3	E2	E1	E0		
Detector Identification:								
MSS3							0	0
MSS2							0	1
MSS1							1	0
USS							1	1

A2 HK-WORD DESCRIPTION

HK-Word : HK2.8 (DPUCDO)

subcom. state : 1000

Bit Assignment	MSB 7	6	5	4	3	2	1	LSB 0
NORMAL OPERATION	0	0						
EMERGEN. MODE NO FRAME PLS	1							
" " NO SPIN RATE		1						
AUTO CAL 1x PER WEEK			0	X				
AUTO CAL ON			1	1				
AUTO CAL OFF			1	0				
SUN GATING OF R2: 0°					0	0	1	
" " " " : 45°					0	1	1	
" " " " : 135°					1	0	1	
" " " " : 225°					1	1	1	
R2 DISABLED					X	1	0	
R2 AND R1 DISABLED					X	0	0	
NORMAL PHA PRIORITY MODE								0
ROTATING PHA " "								1

(Bit 2^n)

(X = don't care)

A2 HK-WORD DESCRIPTION

HK-Word : HK2.9 (DPUCD1)
subcom. state : 1001

Bit Assignment	MSB	Bit 2^n						LSB
	7	6	5	4	3	2	1	0
Sector S1 Definition: ACP-/ACA-Rates from indicated Sector are accum. as ACPS1 and ACAS1 respectiv.								
SECTOR 7	1							
" 6		1						
" 5			1					
" 4				1				
" 3					1			
" 2						1		
" 1							1	
" 0								1

A2 HK-WORD DESCRIPTION

HK-Word : HK2.10 (DPUCD2)

subcom. state : 1010

Bit Assignment		MSB	Bit 2^n						LSB
		7	6	5	4	3	2	1	0
TIME OFFSET CORRECTION: T-Measurement is corrected by the number indicated (2's COMPLEMENT)									
lowest value	-128	1	0	0	0	0	0	0	0
	-127	1	0	0	0	0	0	0	1
	-1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0
	+1	0	0	0	0	0	0	0	1
highest value	+127	0	1	1	1	1	1	1	1

A2 HK-WORD DESCRIPTION

HK-Word : HK2.11 (DPUCD3)

subcom. state : 1011

Bit Assignment	MSB 7	6	5	4	3	2	1	LSB 0
INTERNAL HEATER 1 ON	1							
" " 1 OFF	0							
" " 2 ON		1						
" " 2 OFF		0						
" " 3 ON			1					
" " 3 OFF			0					
DEFL. PLATE VOLTAGE MODE 0				0	0	1		
" " " 1				0	1	1		
" " " 2				1	0	1		
" " " 3				1	1	1		
" " P.S. OFF				X	X	0		
HIGH PRIORITY: RANGE 0							0	0
" " : " 1							0	1
" " : " 2							1	0
NOT DEFINED							1	1

(X = don't care)

A2 HK-WORD DESCRIPTION

HK-Word : HK2.12 (DPUCD4)

subcom. state : 1100

Bit Assignment	MSB 7	Bit 2^n 6	5	4	3	2	1	LSB 0
-(15/30)kV PS OFF-PLS CMD			0					
" " " ON - " "			1					
" " " OFF-MLD CMD		0						
" " " ON - " "		1						
-15kV ON	0	1	1					
-30kV ON	1	1	1					
AUTO STEP REVER. AT RATE 0				0	0	0	1	
" " " " " 1				0	0	1	1	
" " " " " 2				0	1	0	1	
" " " " " 3				0	1	1	1	
" " " " " 4				1	0	0	1	
" " " " " 5				1	0	1	1	
" " " " " 6				1	1	0	1	
" " " " " 7				1	1	1	1	
NO STEP REVERSAL				X	X	X	0	
NO AUTO HV ON								0
DELAYED AUTO HV ON								1

(X = don't care)

A2 HK-WORD DESCRIPTION

HK-Word : HK2.13 (DPUCD5)

subcom. state : 1101

Bit Assignment	MSB	Bit 2^n						LSB
	7	6	5	4	3	2	1	0
Sector Adjustment:								
SUN PULSE WITHIN SECTOR 0						0	0	0
" " " " 1						0	0	1
" " " " 2						0	1	0
" " " " 3						0	1	1
" " " " 4						1	0	0
" " " " 5						1	0	1
" " " " 6						1	1	0
" " " " 7						1	1	1
Fine Adjustment:								
-22.5°		1	0	0	0			
-19.6875°		1	0	0	1			
-16.875°		1	0	1	0			
-14.0625°		1	0	1	1			
-11.25°		1	1	0	0			
- 8.4375°		1	1	0	1			
- 5.625°		1	1	1	0			
- 2.8125°		1	1	1	1			
0°		0	0	0	0			
2.8125°		0	0	0	1			
5.625°		0	0	1	0			
8.4375°		0	0	1	1			
11.25°		0	1	0	0			
14.0625°		0	1	0	1			
16.875°		0	1	1	0			
19.6875°		0	1	1	1			
DV-MONITOR DISABLED	0							
" " ENABLED	1							

A2 HK-WORD DESCRIPTION

HK-Word : HK2.14 (DPUCD6)

subcom. state : 1110

Bit Assignment	MSB			Bit 2^n				LSB
	7	6	5	4	3	2	1	0
Analog HV-Control:								
LEVEL 0						0	0	0
" 1						0	0	1
" 2						0	1	0
" 3						0	1	1
" 4						1	0	0
" 5						1	0	1
" 6						1	1	0
" 7 (Highest Value)						1	1	1
Error Messages:								
NO ERROR			0	0	0			
FORMATING ERROR					1			
PHA ERROR				1				
MODE STATUS ERROR			1					
Special Test Modes:								
NO TEST MODE	0	0						
MODE1: CLASSIFICATION TEST	0	1						
MODE2: ML1 EXEC.EVERY PER.	1	0						

A2 HK-WORD DESCRIPTION

HK-Word : HK2.15 (DPUCD7)
subcom. state : 1111

Bit Assignment	MSB	Bit 2^n						LSB
	7	6	5	4	3	2	1	0
Sectoring of ME, MR, BR and PHA-Words								
EVENTS FROM SECTOR 7	1							
" " " 6		1						
" " " 5			1					
" " " 4				1				
" " " 3					1			
" " " 2						1		
" " " 1							1	
" " " 0								1
ME, MR and BR are accumulated and PHA-Words are stored during the sectors indicated.								

A3. Status Channel Description

Channel Name: PERIOD COUNTER   PC

Channel ID :

EDB-Word : a) HK0
b) HK1 if SID = X000

Bits : a) 4 ... 7 (PCL)
b) 4,5 (PCH)

Range : 0 ... 63

PC: $\underbrace{\boxed{5}\,\boxed{4}}_{\substack{\text{(PCH)} \\ \text{HK1}}}\,\underbrace{\boxed{7}\,\boxed{6}\,\boxed{5}\,\boxed{4}}_{\substack{\text{(PCL)} \\ \text{HK0}}}$

This channel contains the value of the period counter PC. It indicates which step in the 64 voltage cycle is being read out.

The period counter is incremented at the beginning of each period.

A3. Status Channel Description

Channel Name: REVOLUTION COUNTER RC
Channel ID :
EDB-Word : HK1 if SID = X001
Bits : 0 ... 7
Range : 0 ... 255

This housekeeping word contains the value of the revolution counter at the beginning of the previous period with the subcommutation identifier SID = X000 (i.e. period n*8, with n = 0, 1, ... , 7).

The revolution counter is incremented at the beginning of sector 0 of each spin.

A3. <u>Status Channel Description</u>

Channel Name: DELAY D

Channel ID :

EDB-Word : ME3 of EDB 61 (PC = 61)

Bits : 0 ... 7

Range : 0 ... 255

The delay D is the time when the first EDB of a cycle (EDB0, PC=0) is formatted until it begins to be read out. The re~~v~~solution of D is 1/32 spin (nominal 375 ms).

A3. Status Channel Description

Channel Name: DEFL. VOLTAGE CODE DVC
Channel ID :
EDB-Word : a) HK0
b) HK1 if SID = X000
Bits : a) 0 ... 3 (DVL)
b) 0 ... 3 (DVH)
Range : 0 ... 138

DVC:

HK1 (DVH)				HK0 (DVL)			
3	2	1	0	3	2	1	0
	6	5	4	3	2	1	0
Range Bit DVCR	Step Bits DVCS						

Calculation of the defl. voltage step DVS for EDB n :

if Range Bit = 0 : DVS(n) = DVC(n)
if Range Bit = 1 : DVS(n) = DVC(n) - 117

if SID = X000, then
  if DVS(n) - DVS(n-1) > +2 , then DVS(n) := DVS(n) - 16
  if DVS(n) - DVS(n-1) < -2 , then DVS(n) := DVS(n) + 16
else continue

A3. <u>Status Channel Description</u>

Channel Name: DATA COMPRESSION

Channel ID :

EDB - Word : HK1 if SID = XOOO

Bits : 6

Range : 0...1

The DATA COMPRESSION bit indicates the compression mode for all rates of one cycle.

It should be noted that an EDB contains data of two cycles : all hk-data (including the DATA COMPRESSION BIT) ans all rates except the Matrix Elements ME are belonging to the actual cycle, the Matrix Elements are from the previous cycle.

After the change of the compression mode there will be one cycle in which Matrix Elements are compressed in a different way than all other rates, i.e. if the compression mode changed from mode A to mode C, the Matrix Elements are compressed with mode A and all other rates with mode C.