



2023 Digital IC Design Homework 3

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Simulation Result			
Functional simulation	100	Gate-level simulation	100
<div><div><div>Pattern 54 : f-(f'1)+(f'2)= Expected answer: 30 get: 30 --> Pass Pattern 55 : a'a+a+b-(a'b)= Expected answer: 11 get: 11 --> Pass Pattern 56 : f'5-5'5+(1-1)= Expected answer: 50 get: 50 --> Pass Pattern 57 : (1+2)= Expected answer: 3 get: 3 --> Pass Pattern 58 : (1+2)+(2'3)= Expected answer: 9 get: 9 --> Pass Pattern 59 : (1-1)*(c-a)+3-1= Expected answer: 2 get: 2 --> Pass Pattern 60 : ((2-1)*(c-a))= Expected answer: 2 get: 2 --> Pass</div><div><p>Congraultaions!!! You past all patterns! Your score is 100. Total use 2128 cycles to complete simulation.</p><p>** Note: \$finish : C:/modeltech64_10.1c/examples/IC_hw3/testfixture.sv(190) Time: 25536 ns Iteration: 1 Instance: /testfixture</p></div></div></div>		<div><div><div>Pattern 54 : f-(f'1)+(f'2)= Expected answer: 30 get: 30 --> Pass Pattern 55 : a'a+a+b-(a'b)= Expected answer: 11 get: 11 --> Pass Pattern 56 : f'5-5'5+(1-1)= Expected answer: 50 get: 50 --> Pass Pattern 57 : (1+2)= Expected answer: 3 get: 3 --> Pass Pattern 58 : (1+2)+(2'3)= Expected answer: 9 get: 9 --> Pass Pattern 59 : (1-1)*(c-a)+3-1= Expected answer: 2 get: 2 --> Pass Pattern 60 : ((2-1)*(c-a))= Expected answer: 2 get: 2 --> Pass</div><div><p>Congraultaions!!! You past all patterns! Your score is 100. Total use 2188 cycles to complete simulation.</p><p>** Note: \$finish : C:/modeltech64_10.1c/examples/IC_hw3/testfixture.sv(190) Time: 26256 ns Iteration: 1 Instance: /testfixture</p></div></div></div>	
Synthesis Result			
Total logic elements	749		
Total memory bits	0		
Embedded multiplier 9-bit elements	1		
Total cycle used	2188		
Clock width	12		
<div><div><div>Flow Status</div><div>Quartus Prime Version</div><div>Revision Name</div><div>Top-level Entity Name</div><div>Family</div><div>Device</div><div>Timing Models</div><div>Total logic elements</div><div>Total registers</div><div>Total pins</div><div>Total virtual pins</div><div>Total memory bits</div><div>Embedded Multiplier 9-bit elements</div><div>Total PLLs</div></div><div><div>Successful - Tue Mar 28 19:23:13 2023</div><div>20.1.1 Build 720 11/11/2020 SJ Lite Editio</div><div>AEC</div><div>AEC</div><div>Cyclone IV E</div><div>EP4CE55F23A7</div><div>Final</div><div>749 / 55,856 (1 %)</div><div>345</div><div>19 / 325 (6 %)</div><div>0</div><div>0 / 2,396,160 (0 %)</div><div>1 / 308 (< 1 %)</div><div>0 / 4 (0 %)</div></div></div>			
Description of your design			

我用三個 buffer 去記錄數據，並用 5 個狀態去處理(如下圖)

```
reg [2:0] current_state;
reg [2:0] next_state;
parameter INIT = 0;
parameter READ = 1;
parameter TRANSFER = 2;
parameter CALCULATION = 3;
parameter OUTPUT = 4;
reg [7:0] stack [0:7];
reg [7:0] output_buffer [0:15];
reg [7:0] input_buffer [0:15];
```

讀到 ready 進到狀態 1，按照順序將 ascii_in 依序讀進 input

讀到=後進到狀態 2，用三個 pointer 去指向三個 buffer 的 tail 跟 stack 的 top，將 infix 轉為 postfix，依照作業說明去排序，最後結果放在 output_buffer，如果目前指向的 input[tail_in]是:

數字:放進 output 內，繼續往後找

*:若 stack[top]是乘號，將其移出來 output，指標維持在原地;反之直接放進 stack
+,:stack 內的其他運算符號優先度一定都更大(除了左括號)，所以一直移出來到 output 直到 stack 為空或者遇到左括號

=:把所有 stack 內的東西拿出來後進到狀態 3，並把=放進 output
進到狀態 3 後，此時排序已完成，開始依序去讀 output，如果是:

數字:直接放進 stack

符號:把 stack 最頂端兩個拿出來運算，遇到=就結束進到狀態 4

進到狀態 4 後，將 valid 訊號拉起來，並把 stack[0]的值給到 result 輸出

狀態轉換時，須將下一階段 buffer 或 stack 要用到的指標歸零

$$\text{Scoring} = \text{Area cost} * \text{Timing cost}$$

$$\text{Area cost} = \text{Total logic elements} + \text{Total memory bits} + 9 * \text{Embedded multipliers 9-bit elements}$$

$$\text{Timing cost} = \text{Total cycle used} * \text{Clock width}$$

*** Total logic elements must not exceed 1500.**

$$\text{Area cost} = 749 + 0 + 9 * 1 = 758$$

$$\text{Timing cost} = 2188 * 12 = 26256$$

$$\text{Scoring} = 758 * 26256 = 19902048$$