Department of Computer Science and Information Engineering

National Cheng Kung University

LAB - 02

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Outline (10/14)

- 期中考規則說明
- Lab2-1
- Lab2-2 (Half adder)
- Lab2-3 (Comparator)

期中考規則說明

- **考試日期：**
  - **10/21(四) 9:10-10:00**
  - **10/21(四) 10:10-11:00**
  - **10/21(四) 11:10-12:00**
  - **10/21(四) 19:10-20:00**
  - **10/21(四) 20:10-21:00**
- **考試方式：以個人為單位**
- **考試時間：50 min**
- **補充：**
  - **不可使用電腦，但可攜帶1張A4的參考資料**

Three representations for a circuit

1. Boolean Algebra

$F_1 = x + y'z$

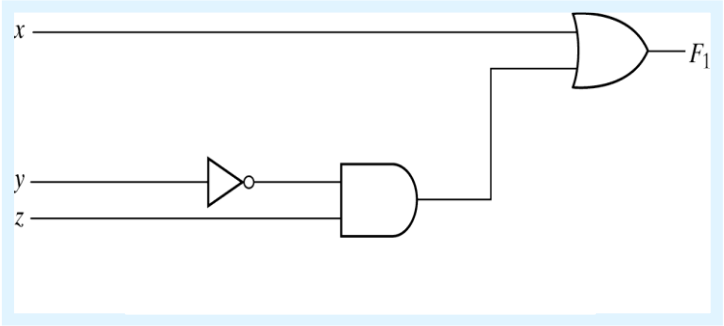
2. Truth Table

真值表

n input variables ➔ 2^n combinations

Inputs					
x	y	z	y'	$y'z$	F_1
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	0	0	1

3. Circuit Diagram



Equipment

Names	Amount
Solerless Breadboard	×1
74LS00	×1
74LS04	×1
74LS08	×1
74LS32	×1

Lab notice

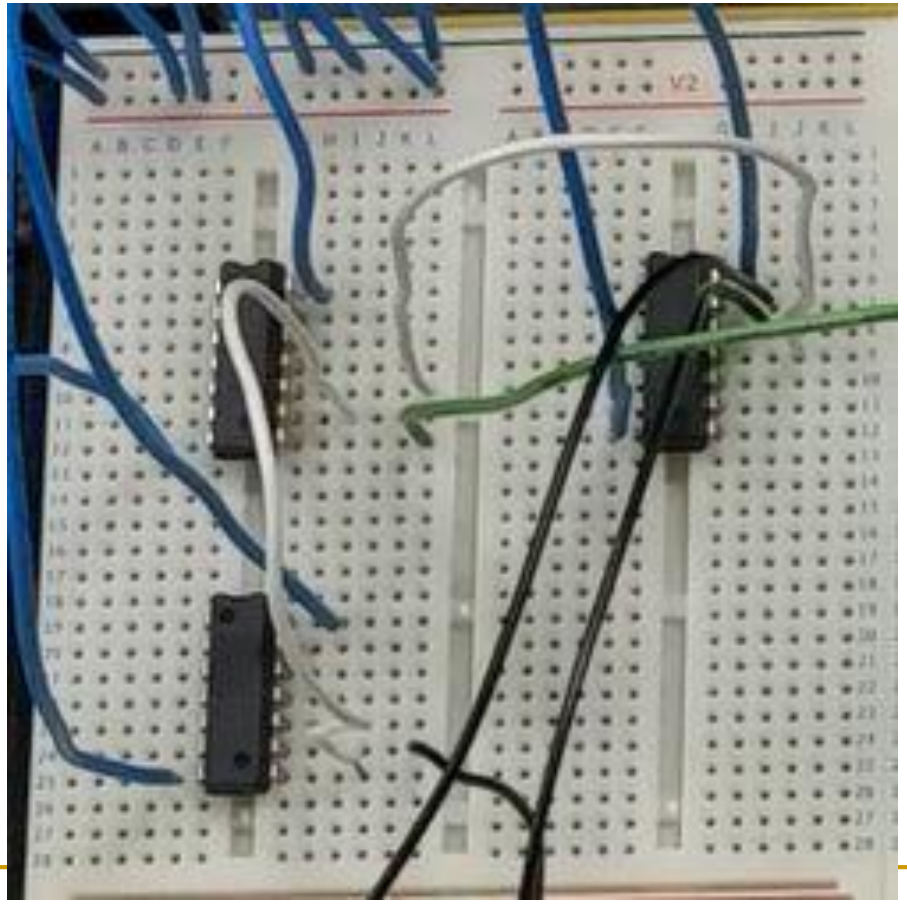
- **Input**

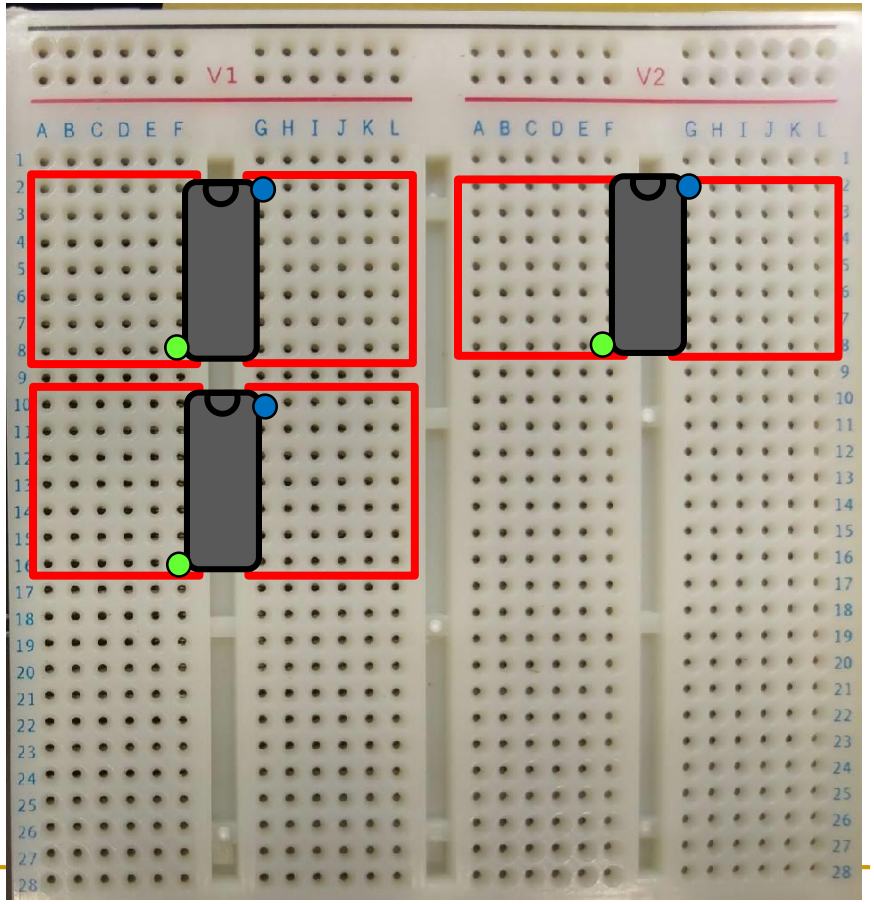
- **Output**

Lab notice

Correct

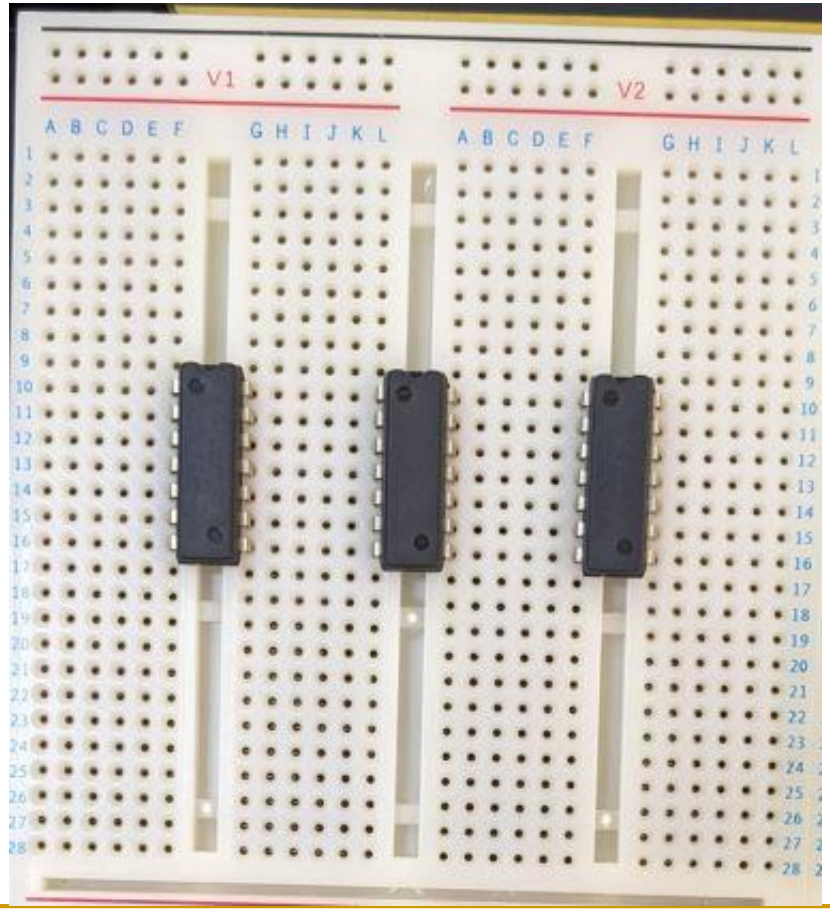
VCC : ●　　GND : ●



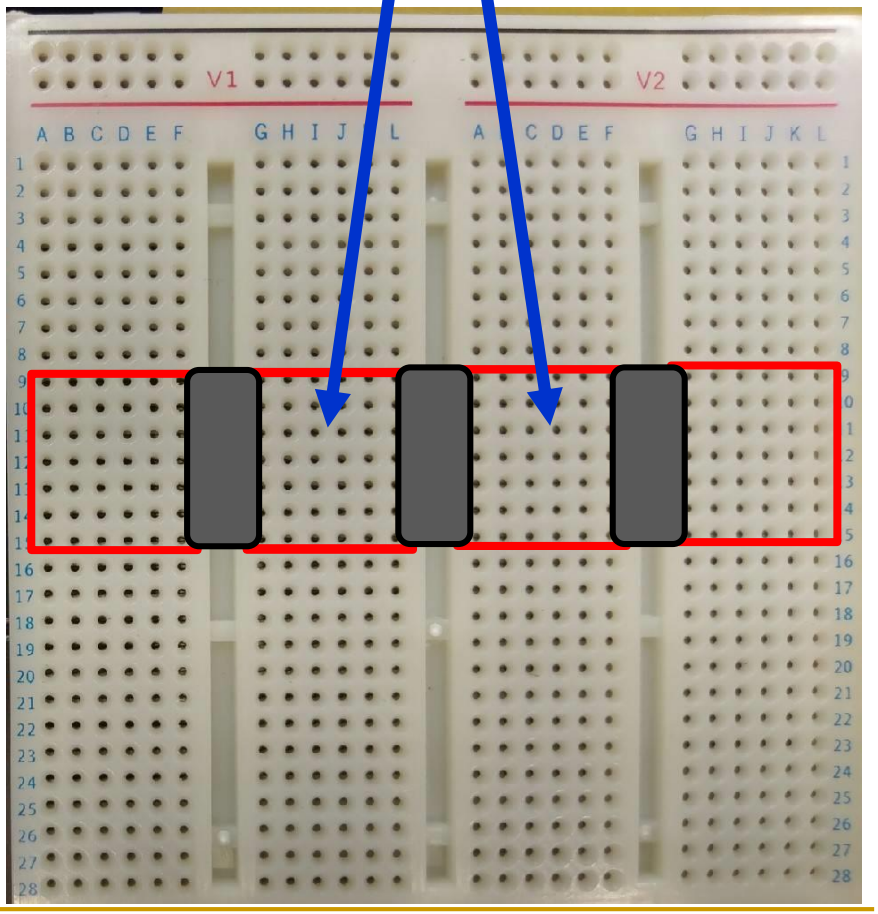


Lab notice

Wrong

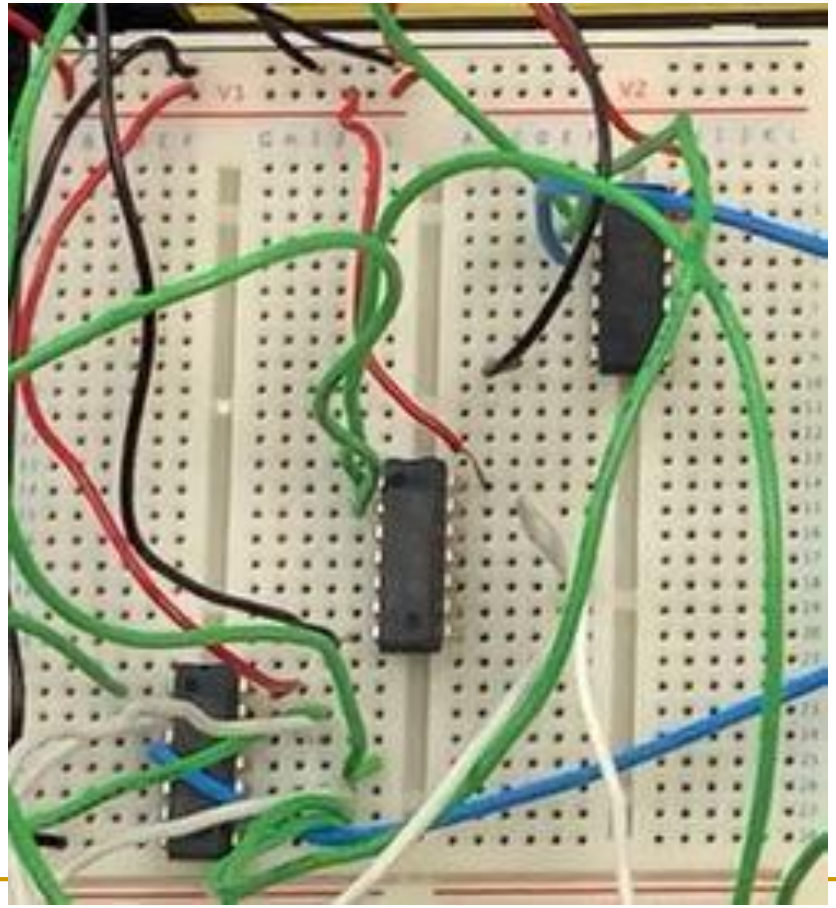


Overlap

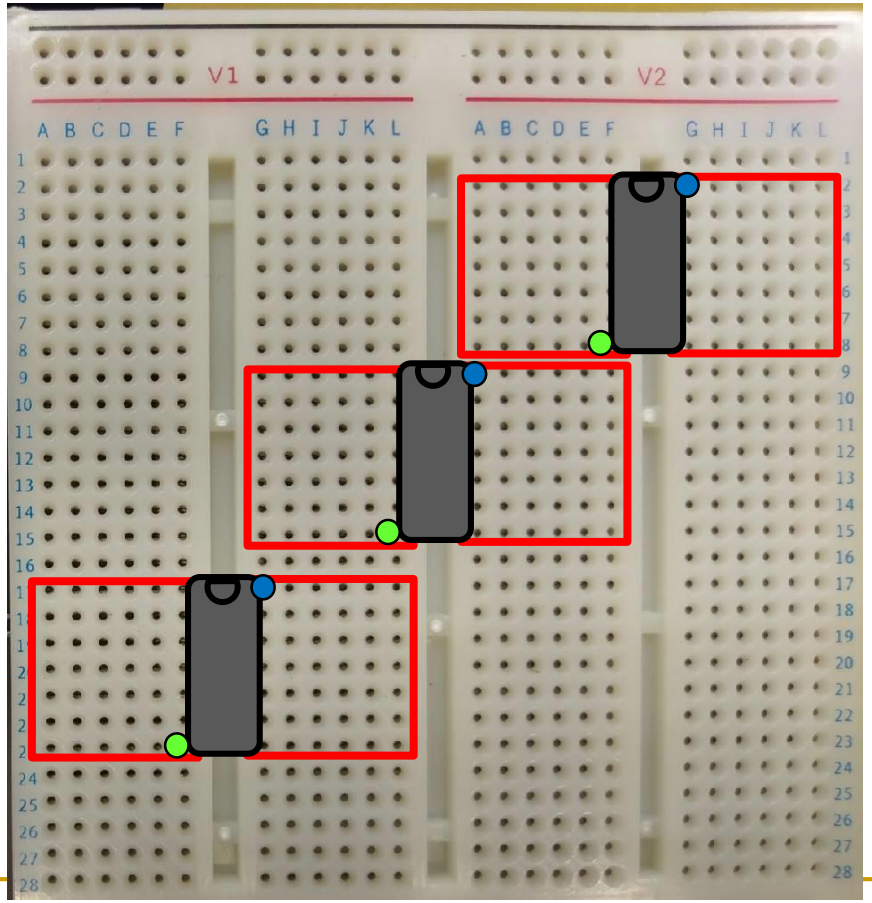


Lab notice

Correct



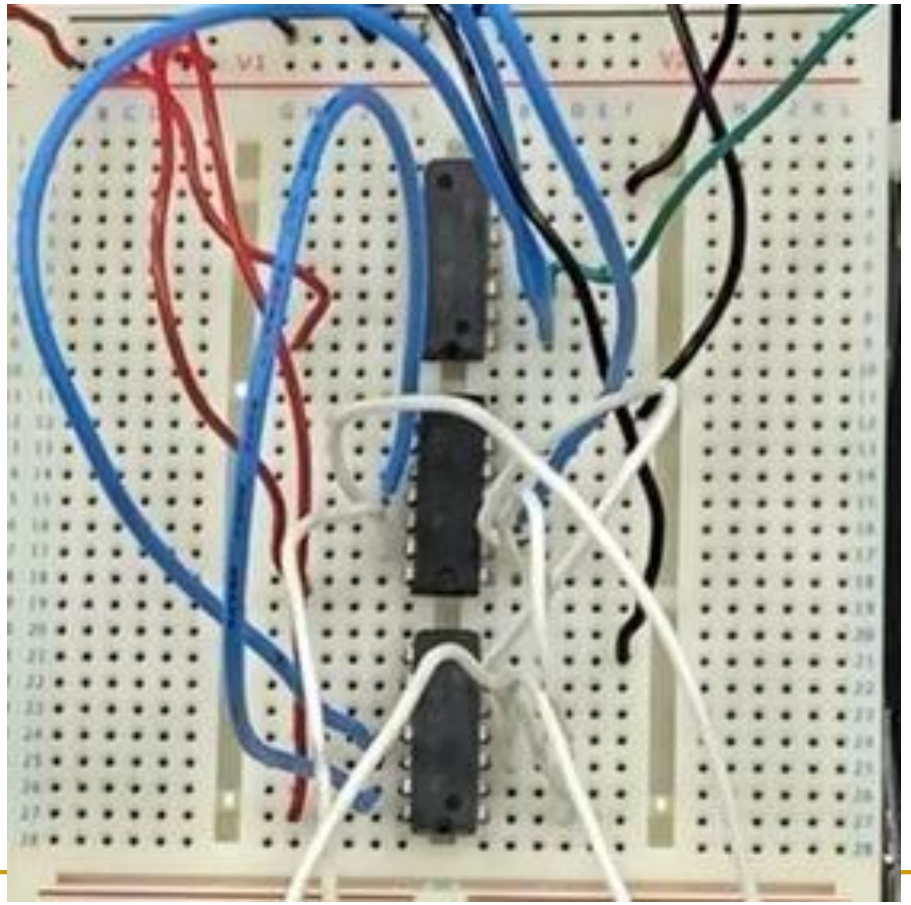
VCC : GND :

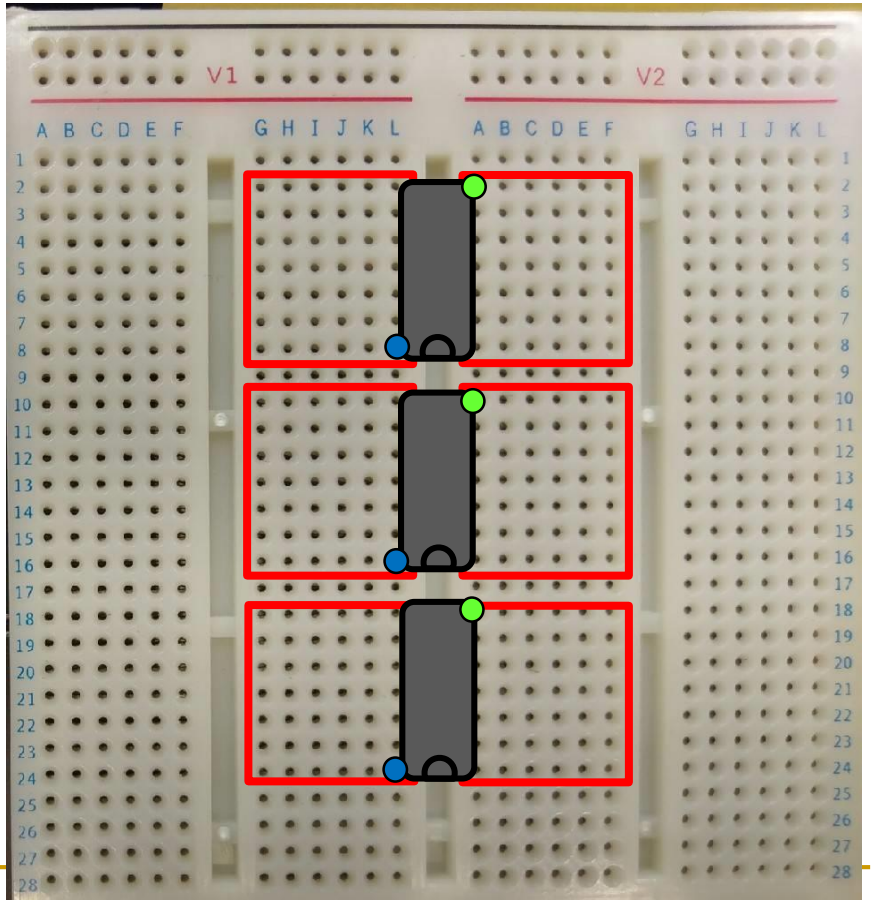


Lab notice

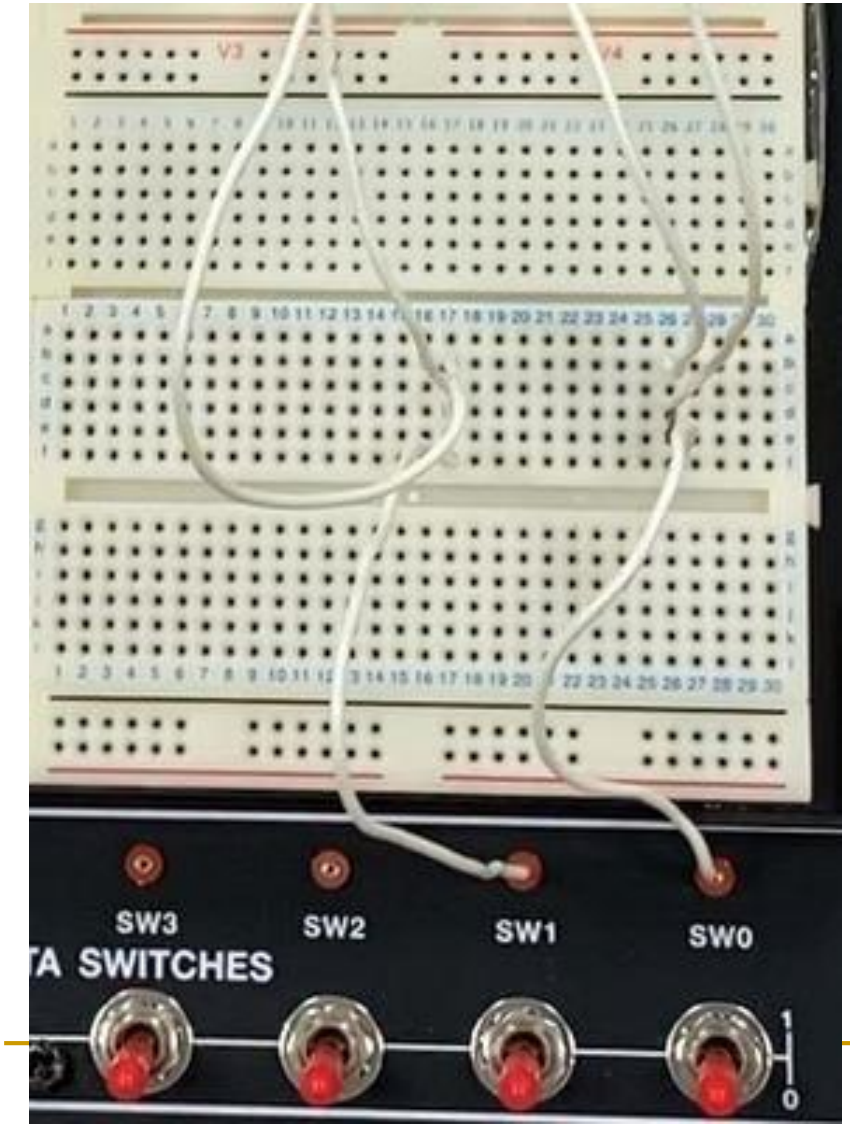
Correct

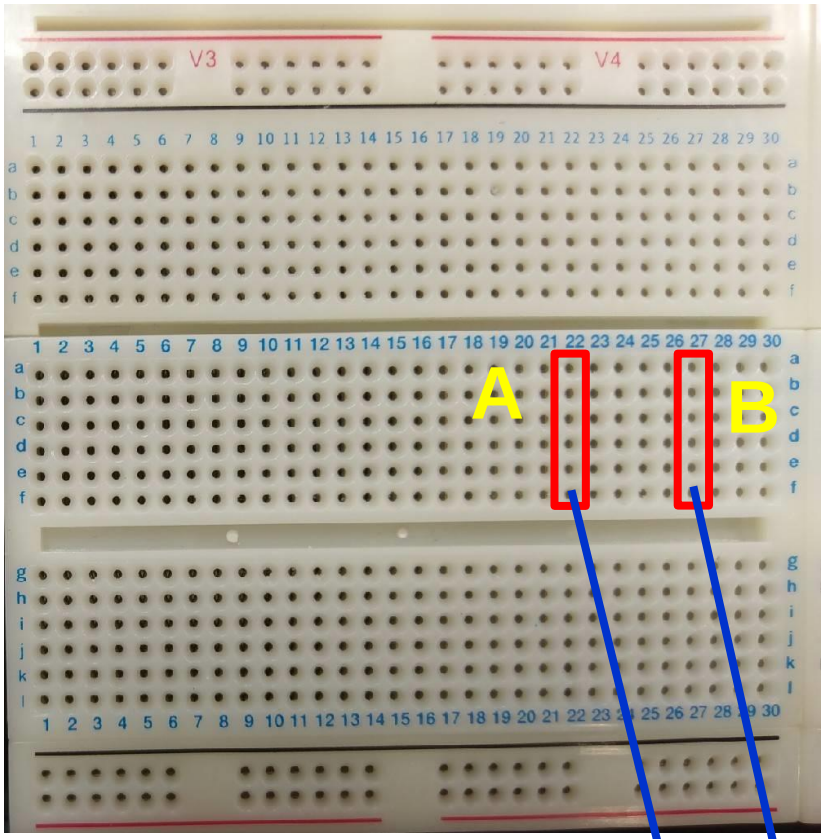
VCC : GND :





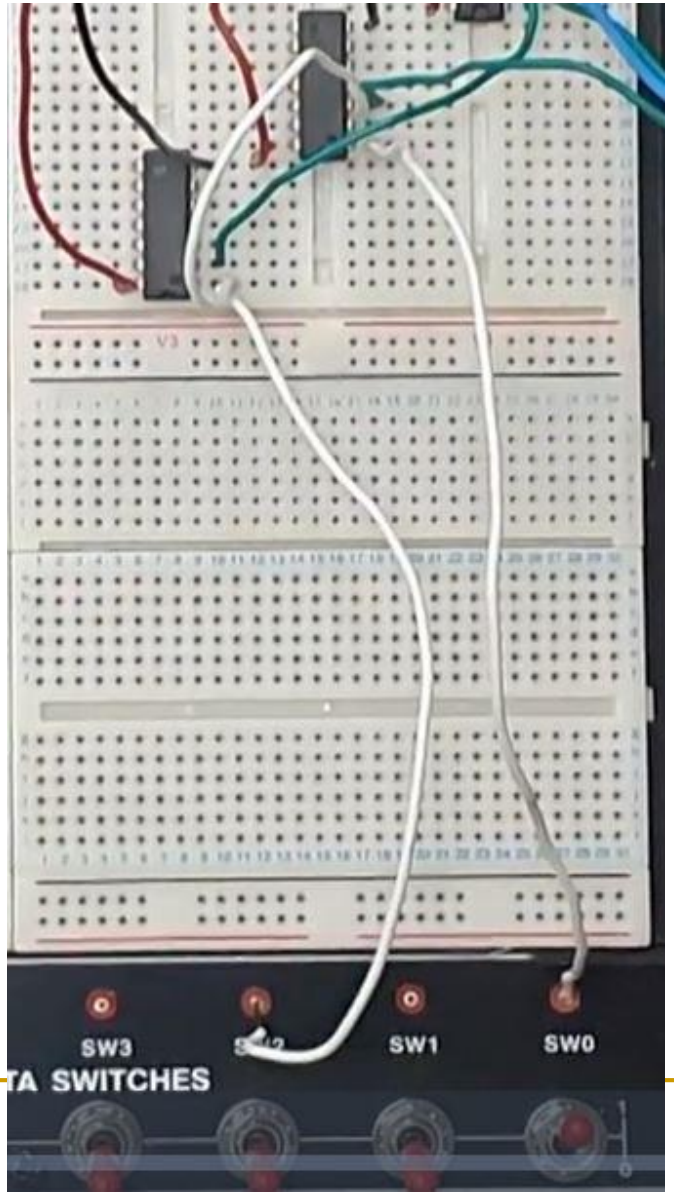
Lab notice

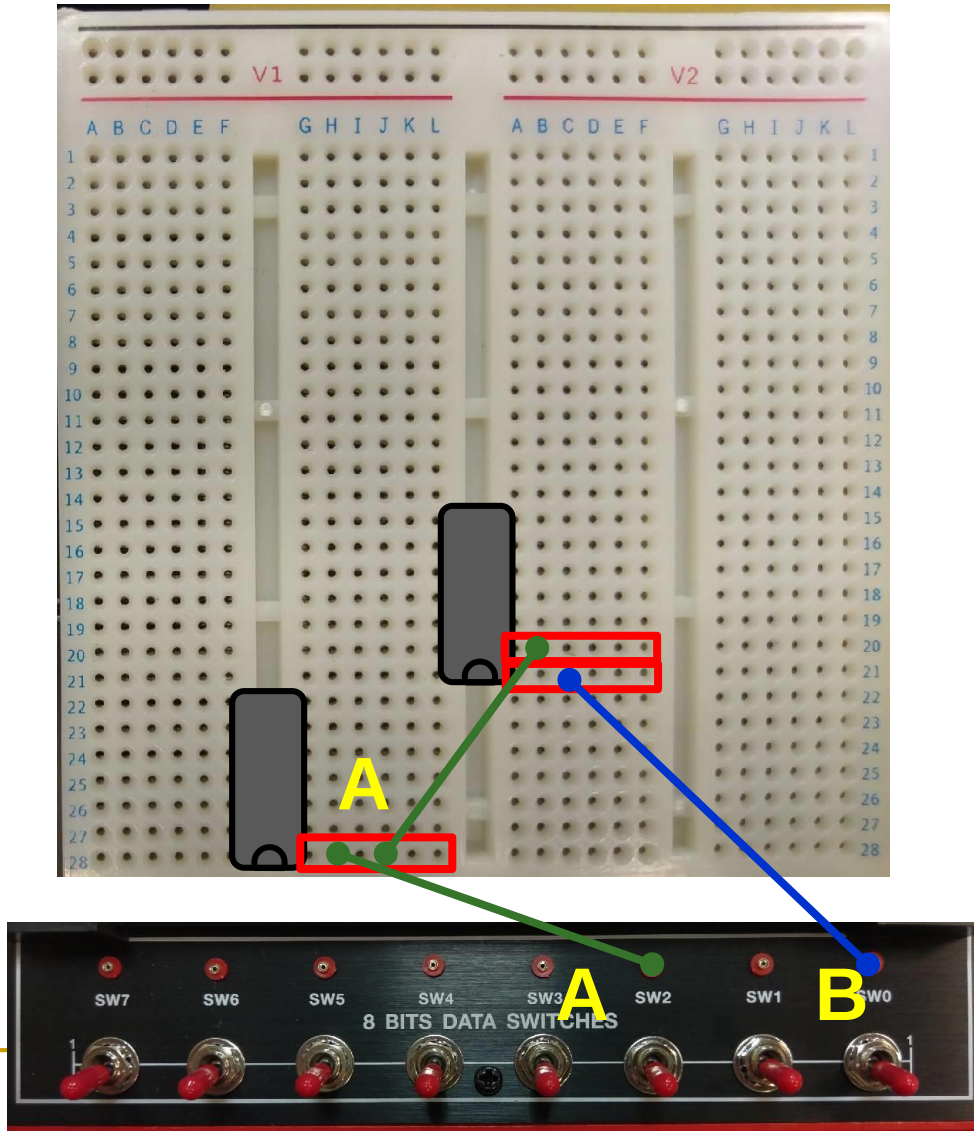

SW3
SW2
SW1
SW0
TA SWITCHES
1
0


V3
V4
A
B


SW7
SW6
SW5
SW4
SW3
SW2
A
SW1
B
SW0
8 BITS DATA SWITCHES

Lab notice


SW3
SW1
SW0
TA SWITCHES


V1
V2
A B C D E F G H I J K L
A
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
A
B
8 BITS DATA SWITCHES

Lab 02-1

- **Please draw their Truth Tables and implement the circuits with breadboard.**
  - **$F_1(A, B) = (A + B)'(A' + B')$**
  - **$F_2(A, B) = A' + AB$**

Lab 02-1

- $F_1(A, B) = (A + B)'(A' + B')$
  - 迪摩根定律
    $(A + B)'(A' + B') \rightarrow (A'B')(A' + B')$
  - 分配律
    $(A'B')(A' + B') \rightarrow A'B'A' + A'B'B'$
  - 等冪性
    $A'B'A' + A'B'B' \rightarrow A'B' + A'B'$
  - 等冪性
    $A'B' + A'B' \rightarrow A'B'$

化簡前：

A	B	F_1
0	0	1
0	1	0
1	0	0
1	1	0

化簡後：

A	B	F_1
0	0	1
0	1	0
1	0	0
1	1	0

Lab 02-1

- $F_2(A, B) = A' + AB$
  - 迪摩根定律
    $A' + AB \rightarrow A' + (A' + B')'$
  - 迪摩根定律
    $A' + (A' + B')' \rightarrow (A(A' + B'))'$
  - 分配律
    $(A(A' + B'))' \rightarrow (AA' + AB')'$
  - 補數性
    $(AA' + AB')' \rightarrow (0 + AB')' \rightarrow (AB')'$
  - 迪摩根定律
    $(AB')' \rightarrow A' + B$

化簡前：

A	B	F_2
0	0	1
0	1	1
1	0	0
1	1	1

化簡後：

A	B	F_2
0	0	1
0	1	1
1	0	0
1	1	1

Lab 02-2 – Half Adder (1/2)

- **A half adder (HA) consists of two inputs (A and B) and two outputs (Sum and Carry). "A" denotes the summand and "B" is the addend. Sum and Carry mean the output sum and carry for input "A" and "B". The truth table and Boolean algebra for the half adder are as follows.**

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\text{Carry} = A \cdot B$$

$$\text{Sum} = \overline{A} \cdot B + A \cdot \overline{B}$$

F(A, B) = A'B' + A'B + AB' + AB

Lab 02-2 – Half Adder (2/2)

Please

(a) draw the circuit diagram of the half adder according to the truth table shown in previous page.

(b) implement the circuit on the breadboard.

Lab 02-3 – Comparator(1/2)

- **There are two inputs denoted as A and B. Both A and B are 1-bit value. A comparator is designed to determine whether A is equal to B or not. The output results are represented with E .**
- **The function of the comparator is described as follows.**

$$E = \begin{cases} 1 & , if\ A\ is\ equal\ to\ B \\ 0 & , else \end{cases}$$

Lab 02-3 – Comparator(2/2)

Please

(a) draw the truth table of the comparator.

(b) draw the circuit diagram of the comparator.

(c) implement the circuit on the breadboard.

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

F(A, B) = (A'B') + (AB)

F(A, B) = A'B' + A'B + AB' + AB