2023 Digital IC Design Homework 4

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Simulation Result

Functional simulation	100	Gate-level simulation	100

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START!!! Simulation Start .....

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Layer 0 output is correct !
Layer 1 output is correct!

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---------------------- S U M M A R Y ----------------

Congratulations! Layer 0 data have been generated successfully! The result is PASS!!

Congratulations! Layer 1 data have been generated successfully! The result is PASS!!

terminate at      60422 cycle
----------------------------------------------------

** Note: $finish    : C:/modeltech64_10.1c/examples/IC_hw4/testfixture.v(178)
   Time: 3021100 ns  Iteration: 0  Instance: /testfixture
```

```
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START!!! Simulation Start .....

----------------------------------------------------

Layer 0 output is correct !
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Congratulations! Layer 0 data have been generated successfully! The result is PASS!!

Congratulations! Layer 1 data have been generated successfully! The result is PASS!!

terminate at      60422 cycle
----------------------------------------------------

** Note: $finish    : C:/modeltech64_10.1c/examples/IC_hw4/testfixture.v(178)
   Time: 3021108253 ps  Iteration: 0  Instance: /testfixture
```

Synthesis Result

Total logic elements	317
Total memory bits	0
Embedded multiplier 9-bit elements	2
Total cycle used	60422

Flow Status	Successful - Thu Apr 27 20:01:40 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	317 / 55,856 (< 1 %)
Total registers	124
Total pins	82 / 325 (25 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

根據不同的座標去設計要跟 image_mem 要的記憶體位置，由於有 replicate padding，所以邊緣座標要取的值需要特別去判斷處理，以左上角的值來說，當 x 且 y 座標小於 2 時，左斜上方 2 的地方會超出取值邊界，此時就直接取(0,0)位置的值即可。
取得值後同時做 convolution，最後存到 L0，當把所有座標的值都算出來之後，依順序讀取 4 個 L0 的值做最大池化，輸出到 L1 時需要無條件進位到下一個整數。

*Scoring = (Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements) X Total cycle used*
*= (317 + 0 + 9*2) * 60422 = 20,241,370*
*** Total logic elements must not exceed 1000.**