2023 Digital IC Design Homework 3

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| **Simulation Result** | | | | | |
| Functional simulation | | 100 | | Gate-level simulation | 100 |
|  | | | |  | |
| **Synthesis Result** | | | | | |
| Total logic elements | | | 749 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 1 | | |
| Total cycle used | | | 2188 | | |
| Clock width | | | 12 | | |
|  | | | | | |
| **Description of your design** | | | | | |
| 我用三個buffer去記錄數據，並用5個狀態去處理(如下圖)    讀到ready進到狀態1，按照順序將ascii\_in依序讀進input  讀到=後進到狀態2，用三個pointer去指向三個buffer的tail跟stack的top，將infix轉為postfix，依照作業說明去排序，最後結果放在output\_buffer，如果目前指向的input[tail\_in]是:  數字:放進output內，繼續往後找  \*:若stack[top]是乘號，將其移出來output，指標維持在原地；反之直接放進stack  +.-:stack內的其他運算符號優先度一定都更大(除了左括號)，所以一直移出來到output直到stack為空或者遇到左括號  =:把所有stack內的東西拿出來後進到狀態3，並把=放進output  進到狀態3後，此時排序已完成，開始依序去讀output，如果是:  數字:直接放進stack  符號:把stack最頂端兩個拿出來運算，遇到=就結束進到狀態4  進到狀態4後，將valid訊號拉起來，並把stack[0]的值給到result輸出  狀態轉換時，須將下一階段buffer或stack要用到的指標歸零 | | | | | |

*Scoring = Area cost \* Timing cost*

*Area cost = Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used \* Clock width*

**\* Total logic elements must not exceed 1500.**

*Area cost = 749 + 0 + 9 \* 1 = 758*

*Timing cost = 2188 \* 12 = 26256*

*Scoring = 758 \* 26256 = 19902048*