2023 Digital IC Design Homework 4

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| **Simulation Result** | | | | | |
| Functional simulation | | 100 | | Gate-level simulation | 100 |
|  | | | |  | |
| **Synthesis Result** | | | | | |
| Total logic elements | | | 317 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 2 | | |
| Total cycle used | | | 60422 | | |
|  | | | | | |
| **Description of your design** | | | | | |
| 根據不同的座標去設計要跟image\_mem要的記憶體位置，由於有replicate padding，所以邊緣座標要取的值需要特別去判斷處理，以左上角的值來說，當x且y座標小於2時，左斜上方2的地方會超出取值邊界，此時就直接取(0,0)位置的值即可。  取得值後同時做convolution，最後存到L0，當把所有座標的值都算出來之後，依順序讀取4個L0的值做最大池化，輸出到L1時需要無條件進位到下一個整數。 | | | | | |

*Scoring = (Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements) X Total cycle used*

*= (317 + 0 + 9\*2) \* 60422 = 20,241,370*

**\* Total logic elements must not exceed 1000.**