Computer Organization Exam 1 2020/4/13 (Scope: Ch1&Ch 2)

(It's a closed book exam. All electronic devices must be turned off. Be sure to answer the questions in order. You will lose at least 5 points for each violation.

Part 1: Short Answers (20 %)

1. (2%) Explain "Response time" and "Throughput". Explain why "Response time" is not a good metric to evaluate computer performance.
2. (3%) What is the meaning of power wall, and what is the current solution to achieve higher performance under the power wall problem.
3. (3%) Assume a 15 cm diameter wafer has a cost of 54 dollars, contains 120 dies, and the yield is 90%. Find the cost per die.
4. (3%) If multiplication accounts for 80s of 100s total operation, how much improvement can be achieved if in multiplication performance is improved by 10X.
5. (3%) The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. Find the average capacitive loads of the processor.
6. (3%) What is the rang of address for jump and jump and link in MIPS? Explain why
   (a) Address between 0 and 64M -1
   (b) Address between 0 and 256M -1
   (c) Address up to about 32M before the branch to about 32M after
   (d) Addresses up to about 128M before the branch to about 128M after
   (e) Anywhere within a block of 64M addresses where the PC supplies the upper 6 bits
   (f) Anywhere within a block of 256M addresses where the PC supplies the upper 4bits
7. (3%) What are the addressing modes used in the following instruction?

   lw $t3, 0($s1)

Part 2 (80%):

1. (10%) Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
   a. Which processor has the highest performance expressed in instructions per second?
   b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
   c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?
2. (5%) Given the following table, what are the SPECratios for Biz2 and Gcc?

Benchmark Name	Instruction Count x 10^9	CPI	Clock cycle time (ns)	Execution Time (s)	Reference Time (s)
Bzip2	2,389	0.85	0.4	817	9650
Gcc	1,050	1.72	0.4	724	8050

3. (10%) Consider the following two computers.

Processor	**Clock Rate**	**CPI**
P1	**4.5 GHz**	**1.5**
P2	**3.2 GHz**	**0.8**

   a. Which processor has higher clock frequency and which processor has higher performance?
   b. A common fallacy is to use MIPS (millions of instructions per second) to compare the performance of two different processors, and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P 1 and P2.

4. (5%) Assume the following register contents:

   $t0 = 0xAAAAAAAA, $t1 = 0x12345678

For the register values shown above, what is the value of $t2 for the following sequence of instructions?

```
sll $t2, $t0, 4
or $t2, $t2, $t1
```

5. (5%) For the MIPS assembly instructions below, what is the corresponding C statement ? Assume that the variables f, g, h, i, and j are assigned to registers $s0,$s1,$s2,$s3, and $s4, respectively . Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively.

	MIPS Instruction	
1.	sll $t0, $s0 , 2	$t0 = f * 4
2.	add $t0, $s6 , $t0	$t0 = &A[f]
3.	sll $t1, $s1 , 2	$t1 = g * 4
4.	add $t1, $s7 , $t1	$t1 = &B[g]
5.	lw $s0, 0($t0)	f= A[f]
6.	addi $t2, $t0 , 8	
7.	lw $t0, 0($t2)	
8.	sub $t0, $t0 , $s0	
9.	sw $t0, 0($t1)	

6. (5%) Provide the type and assembly language instruction for the following binary value : 0x02119021

7. (5%) show the bit-level representation of each instruction.
   lw $t3, 0($s1)
   and $t1, $t2, $t3

8. (5%) Sketch the layout for the MIPS memory allocation. Briefly explain what the purpose of each section is.

9. (10%) Translate the following program in to MIPS assembly codes. Assume that i and k correspond to registers $s3 and s5, and the base of the array save is in $s6, what is the MIPS assembly code corresponding to this C segment?

```
while (save[i] == k)
    i +=1;
```

10. (5%) Suppose the program counter (PC) is set to 0x2000 0000.
    a. Is it possible to use the jump (j) MIPS assembly instruction to set the PC to the address as 0x4000 0000? Explain why
    b. Is it possible to use the branch-on-equal (beq) MIPS assembly instruction to set the PC to this same address? Explain why

11. (5%) Write the MIPS assembly code that creates the 32-bit constant
    0010 0000 0000 0001 0100 1001 0010 0100_2 and stores that value to register $t1.

12. (10%) Rewrite the following MIPS instructions on the right to match the C source codes on the left. Fix errors in the MIPS instructions if there are any errors.

C codes	Line No.	MIPS instructions

int fact (int n)
{
if (n < 1) return 1;
else return n * fact(n - 1);
}
	1
	2
	3
	4
	5
	6
	7
	8
	9
	10
	11
	12
	13
	14
	15
	16
		fact:
		addi $sp, $sp, -8
		beq $t0, $zero, L1
		addi $v0, $zero, 1
		slti $t0, $a0, 1
		jr $ra
		addi $sp, $sp, 8
		L1: addi $a0, $a0, -1
		jal fact
		lw $a0, 0($sp)
		lw $ra, 4($sp)
		jr $ra
		addi $sp, $sp, 8
		mul $v0, $a0, $v0
		sw $ra, 4($sp)
		sw $a0, 0($sp)

Instruction Decoding Table

Op(31:26)								
28-26 / 31-29	0(000)	1(001)	2(010)	3(011)	4(100)	5(101)	6(110)	7(111)
0(000)	R-format	Bltz/gez	Jump	Jump &link	Branch eq	Branch ne	blez	bgtz
1(001)	Add immediate	Addiu	Set less than imm.	Set less than imm. Unsigned	andi	ori	xori	Load upper imm.
2(010)	TLB	FlPt						
3(011)								
4(100)	Load byte	Load half	Lwl	Load word	Load byte unsigned	Load half unsigned	lwr	
5(101)	Store byte	Store half	Swl	Store word			swr	
6(110)	Load linked word	lwcl						
7(111)	Store cond. word	swcl						

Op(31:26)=000000 (R-format), funct(5:0)								
2-0 / 5-3	0(000)	1(001)	2(010)	3(011)	4(100)	5(101)	6(110)	7(111)
0(000)	Shift left logical		Shift right logical	Sra	sllv		srlv	srav
1(001)	jump register	jalr			Syscall	Break		
2(010)	mfhi	mthi	mflo	mtlo				
3(011)	Mult	Multu	div	Divu				
4(100)	Add	Addu	Subtract	Subu	And	Or	Xor	Not or (nor)
5(101)			Set l.t.	Set l.t. unsigned				
6(110)								
7(111)								

Name	Fields						Comments
Field size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions are 32 bits long
R-format	op	rs	rt	rd	shamt	funct	Arithmetic instruction format
I-format	op	rs	rt	address/immediate			Transfer, branch, imm. format
J-format	op	target address					Jump instruction format

Name	Register Number	Usage	Preserve on call?
$zero	0	constant 0 (hardware)	n.a.
$at	1	reserved for assembler	n.a.
$v0 - $v1	2-3	returned values	No
$a0 - $a3	4-7	Arguments	Yes
$t0 - $t7	8-15	temporaries	No
$s0 - $s7	16-23	saved values	Yes
$t8 - $t9	24-25	temporaries	No
$gp	28	global pointer	Yes
$sp	29	stack pointer	Yes
$fp	30	frame pointer	Yes
$ra	31	return addr (hardware)	Yes