Disclaimer: The solutions are just for your reference. They may contain some errors. DO TRY to solve the problems by yourself before checking the solutions. Please also pay attentions to the course moodle website for the updates.

Selected Exercise

1.5.a~ 1.5.c, 1.6.a ~ 1.6.b, 1.7.a~1.7.b, 1.8.1~1.8.2, 1.10.1~1.10.2, 1.11.1~1.11.3, 1.12, and 1.13

1.5

a. performance of P1 (instructions/sec) = $3 \times 10^9/1.5 = 2 \times 10^9$

performance of P2 (instructions/sec) = $2.5 \times 10^9/1.0 = 2.5 \times 10^9$

performance of P3 (instructions/sec) = $4 \times 10^9/2.2 = 1.8 \times 10^9$

b. cycles(P1) = $10\times 3\times10^9= 30\times10^9$s

cycles(P2) = $10 \times2.5 \times10^9 = 25\times10^9$ s

cycles(P3) = $10 \times 4 \times10^9 = 40\times10^9$ s

No. instructions(P1) =$30\times10^9 /1.5 =20\times10^9$

No. instructions(P2) =$25\times10^9 /1=25\times10^9$

No. instructions(P3) = $40\times10^9/2.2=18.18 \times 10^9$

c.

$CPI_{new} =CPI_{old} \times1.2$, then CPI(P1) = 1.8, CPI(P2)= 1.2, CPI(P3) =2.6

f=No. instr. × CPI/time, then

f(P1) = $20\times10^9\times1.8/7 = 5.14$ GHz

f(P2) = $25\times10^9\times 1.2/7 = 4.28$ GHz

f(P1) = $18.18\times10^9\times2.6/7 = 6.75$ GHz

1.6

a. Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.

Time= No. instr. × CPI/clock rate

Total time P1 = $(10^5+ 2 \times10^5\times 2+ 5 \times10^5\times 3 + 2\times 10^5 \times 3)/(2.5 \times 10^9) =10.4\times 10^{-4}$ s

Total time P2 = $(10^5\times 2 +2 \times10^5 \times2+5 \times 10^5 \times 2 + 2 \times10^5 \times2)/(3\times10^9) = 6.66 \times10^{-4}$s

P2 is faster.

CPI(P1) = $10.4 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 2.6$

CPI(P2) = $6.66 \times 10^{-4}\times 3 \times10^9/10^6= 2.0$

b. clock cycles(P1) = $10^5\times1+ 2 \times10^5\times 2 + 5 \times10^5 \times3 +2 \times10^5 \times3 =26 \times 10^5$

clock cycles(P2)= $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

1.7

a. $\text{CPI} = \frac{Cycles}{Inst.Count} = \frac{time * clock\ rate}{Inst.count}$

Compiler A CPI = $1.1 * 10^9/10^9 = 1.1$

Compiler B CPI = $1.5*10^9/1.2*10^9=1.25$

b.

	Inst. Count	Time	CPI
Program by Compiler A	10^9	1.1	1.1
Program by Compiler B	$1.2*10^9$	1.5	1.25

Freq A= Instr Count(B) × CPI(B)/ time(B) = $10^9 * 1.1$ /time

Freq B= Instr Count(A) × CPI(A)/ time(A)= $1.2*10^9 * 1.25$/time

f_B/f_A = (No. instr.(A) × CPI(A))/(No. instr.(B) × CPI(B)) = 1.37

c.

$$\text{CPI} = \frac{Cycles}{Inst.Count} = \frac{time * clock\ rate}{Inst.count}$$

Time = $1.1 * 6.0*10^8 / 10^9 = 0.66$ s

Speedup of new compiler over compiler A =

Perf(New)/Perf(A)=Time(A)/Time(new) = 1.1 /0.66 = 1.67

Speedup of new compiler over compiler B =

Perf(New)/Perf(B)=Time(B)/Time(new) = 1.5 /0.66 = 2.27

1.8.1

$$\textbf{Dynamic Power} = \frac{1}{2}CV^2$$

	Clock rate	Voltage	Static power	Dynamic Power
P4	3.6	1.25	10	90
Ivy Bridge	3.4	0.9	30	40

C =2× Dynamic Power/(V^2*F)= 2 * 90 /(1.25*1.25*3.6*10^9)

Pentium 4: C =3.2E–8F

Core i5 Ivy Bridge: C = 2.9E–8F

1.8.2 Pentium 4: 10/100= 10%. Ratio of static power to dynamic power = 1/9
Core i5 Ivy Bridge: 30/70= 42.9%. Ratio of static power to dynamic power = 3/4

1.10.1 die $area_{15cm}$=wafer area/dies per wafer = $pi*7.5^2$ / 84= 2.10 cm^2
$yield_{15cm}$ = $1/(1+(0.020*2.10/2))^2$ =0.9593
die $area_{20cm}$ = wafer area/dies per wafer =$pi*10^2/100$ = 3.14 cm^2
$yield_{20cm}$ =$1/(1+(0.031*3.14/2))^2$ = 0.9093

1.10.2 $cost/die_{15cm}$ = 12/(84*0.9593) =0.1489
$cost/die_{20cm}$= 15/(100*0.9093)= 0.1650

11.1
1.11.1
CPI= clock rate × CPU time/instr. Count
clock rate = 1/cycle time = 3 GHz
CPI(bzip2) = $3\times 10^9 \times 750/(2389 \times 10^9)$= 0.94
1.11.2 SPEC ratio = ref. time/execution time
SPEC ratio(bzip2) =9650/750 =12.86
1.11.3. CPU time = No. instr. × CPI/clock rate
If CPI and clock rate do not change, the CPU time increase is equal to the increase in the of number of instructions, that is 10%.

1.12.1 $\text{CPI} = \frac{Cycles}{Inst.Count} = \frac{time*clock\ rate}{Inst.count}$

	Clock Rate	CPI	Inst. Count	
P1	4GHz	0.9	5E9	
P2	3	0.75	1E9	

$T(P1) = 5 \times 10^9 \times 0.9 / (4 \times 10^9) = 1.125$ s
$T(P2) = 10^9 \times 0.75 / (3\times 10^9) = 0.25$ s
clock rate (P1)> clock rate(P2), but performance(P1) < performance(P2). Therefore, it is false
1.12.2 T(P1)= No. instr. × CPI/clock rate= 1E9 * 0.9 / 4E9 =

$T(P1) = 0.225s$

$T(P2) = N \times 0.75/(3 \times 10^9)$, then $N = 9 \times 10^8$

1.12.3 MIPS= Clock rate /(CPI*10^6)

$MIPS(P1) = 4 \times 10^9 \times 10^{-6}/0.9= 4.44 \times 10^3$

$MIPS(P2) = 3 \times 10^9 \times 10^{-6}/0.75 = 4.0\times 10^3$

MIPS(P1) > MIPS(P2), but performance(P1) <performance(P2) (from 11a). Therefore, it is false

1.12.4 MFLOPS = No. FP operations $\times 10^{-6}$/T

MFLOPS(P1) =0.4 ×5E9 × 10^{-6}/1.125 = 1.78E3

MFLOPS(P2) =0.4 × 1E9 × 10^{-6}/0.25 = 1.60E3

MFLOPS(P1) > MFLOPS(P2), performance(P1) < performance(P2) (from 11a)

1.13 Another pitfall cited in Section 1.10 is expecting to improve the overall performance of a computer by improving only one aspect of the computer. Consider a computer running a program that requires 250s, with 70s spent executing FP instructions, 85s executed INT instructions, 55s executed L/S instructions, and 40s spent executing branch instructions.

1 .13.1 [5] <§1.10> By how much is the total time reduced if the time for FP operations is reduced by 20%?

1.13.2 [5] <§1.10> By how much is the time for INT operations reduced if the total time is reduced by 20%?

1.13.3 [5] <§1.10> Can the total time can be reduced by 20% by reducing only the time for branch instructions?

	FP instr.	INT instr.	L/S instr.	Branch instr.	Total time
	70 s	85 s	55s	40 s	250 s

1.13.1 $T_{fp} = 70 \times 0.8 = 56$ s. $T_{new} = 56+85+55+40 = 236$ s. Reduction: 5.6% (1-236/250)

1.13.2 $T_{new} = 250 \times 0.8 = 200$ s, $T_{fp}+T_{l/s}+T_{branch}=70+85=165$ s, $T_{int} = 35$ s. Reduction time INT: 58.8% =(85-35)/85

1.13.3 $T_{new} = 250 \times 0.8 = 200$ s, $T_{fp}+T_{int}+T_{l/s} = 210$ s. NO