Computer Organization Exam 1 202*0/4/*13 (Scope: Chl&Ch 2) (It's a closed book exam. All electronic devices must be turned off. Be sure to answer the questions in order.

You will lose at least 5 points for each violation. Part 1: Short Answers *(*20 %) 1. (2%) Explain “Response time” and “Throughput”. Explain why “Response time” is not a good metric to

evaluate computer performance. 2. (3%) What is the meaning of power wall, and what is the current solution to achieve higher performance

under the power wall problem. 3. (3*%*) Assume a 15 cm diameter wafer has a cost of 54 dollars, contains 120 dies, and the yield is 90*%*.

Find the cost per die. 4. (3%) If multiplication accounts for 80s of 100s total operation, how much improvement can be achieved

if in multiplication performance is improved by 10X. 5. (3%) The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of

1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. Find

the average capacitive loads of the processor. 6. (3%) What is the rang of address for jump and jump and link in MIPS? Explain why

(a) Address between 0 and 64M -1 (b) Address between 0 and 256M-1 (c) Address up to about 32M before the branch to about 32M after (d) Addresses up to about 128M before the branch to about 128M after (e) Anywhere within a block of 64M addresses where the PC supplies the upper 6 bits

(f) Anywhere within a block of 256M addresses where the PC supplies the upper 4bits *7.* (3%) What are the addressing modes used in the following instruction?

lw $t3, 0($sl)

Part 2 (80%): 1. (10%) Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has a 3

GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock **rat**e and has a CPI of 2.2. a. Wh*i*ch processor has the highest performance expressed in instructions per second? b. *If* the processors each execute a program in 10 seconds, find the number of cycles and the number of

**instructions.** c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI.

What clock rate should we have to get this time reduction? 2. *(*5%) Given the following table, what are the SPECratios for Biz2 and Gcc?

924

8050

Benchmark Name | Instruction Count | CPI | Clock cycle | Execution Reference

x 10°

time (ns) Time (s) Time (s) Bzip2

2,389

0.85

10.4

**817**

| 9650 Gcc

1,050

1.72 10.4

72*4*

8050 3. (10%) Consider the following two computers.

**Processor**

**Clock Rate**

**CPI P1**

**4.5 GHz**

**1.5 P2**

**3.2 GHZ**

**0.8** a. Which processor has higher clock frequency and which processor has higher performance? b. A common fallacy is to use MIPS (millions of instructions per second) to compare the performance

of two different processors, and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P 1 and P2.

4. (5%) Assume the following register contents:

$t0 = 0xAAAAAAAA, $t1 = 0x12345678 For the register values shown above, what is the value of $t2 for the following sequence of instructions?

sll $t2, $t0,4 or $t2, $t2, $t1

*5*. (5%) For the MIPS assembly instructions below, what is the corresponding C statement ? Assume that

the variables f, g, h, i, and j are assigned to registers $50,$s1,$s2,$s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $87, respectively.

MIPS Instruction

sll $t0,$50,2

$t0=f\*4 add $t0,$s6 , $t0

$t0=&Asf] sll $t1, $s1 , 2

$t1 = g \* 4 add $t1, $s7,$t1

$t1 = &B[g] lw $50, 0($t0)

f=Alf] addi $t2, $t0,8 lw $t0, 0($t2) sub $t0,$t0,$s0 sw $t0,($t1)

6. (5%) Provide the type and assembly language instruction for the following binary value: 0x02119021

*7.* (5%) show the bit-level representation of each instruction.

lw $t3, 0($s1) and $t1, $t2, $t3

8. (5%) Sketch the layout for the MIPS memory allocation. Briefly explain what the purpose of each

section is.

9. *(*10*%*) Translate the following program in to MIPS assembly codes. Assume that i and k correspond to

**regist**ers $s3 and s5, and the base of the array save is in $s6, what is the MIPS assembly code corresponding to this C segment?

while (save[i] == k)

it=1; 10. (5%) Suppose the program counter (PC) is set to 0x2000 0000.

a. Is it possible to use the jump (i) MIPS assembly instruction to set the PC to the address as 0x4000

0000? Explain why b. Is it possible to use the branch-on-equal (beq) MIPS assembly instruction to set the PC to this same

address? Explain why

11. (5%) Write the MIPS assembly code that creates the 32-bit constant

0010 0000 0000 0001 0100 1001 0010 01002 and stores that value to register $t1.

12. (10%) Rewrite the following MIPS instructions on the right to match the C source codes on the left. Fix

errors in the MIPS instructions if there are any errors.

C codes

Line No. MIPS instructions int fact (int n)

fact:

addi $sp,$sp, -8 if(n< 1) return 1;

beq $t0, $zero, L1 else return n \* fact(n - 1);

addi $v0, $zero, 1 slti $t0, $a0, 1 jr $ra

addi $sp,$sp, 8 Ll: addi $a0, $a0, -1

jal fact lw $a0, 0($sp) lw $ra, 4($sp) jr $ra addi $sp,$sp, 8 mul $v0, $a0, $v0 SW $ra, 4($sp) SW $a0, 0($sp)

Instruction Decoding Table

Op(31:26) 3(011)

0(000)

1(001)

2(010)

4(100)

5(101)

6(110) 7(111)

28-26 31-29

0(000)

**R-format**

Branch ne

Bltz*/g*ez

Addiu

Branch eq **andi**

blez **xori**

bgtz Load upper

1(001)

A*dd*

**ori**

| Jump Jump &link

**Set less Set less than than imm.imm.**

Unsigned

**immediate**

**imm.**

2(010)

TLB

**FIPT**

3(011) 4(100)

Load byte

Load half

Lwl

Load word

| lwr

| Load byte | Load half unsigned unsigned

Swl

Store word

**sw*r***

5(101) 6(110)

| Store half

wel

Store byte Load linked **word** Store cond. word

7(111)

*s*wc

Op(31:26)=000000 (R-format), funct(5:0) | 1(001) 2(010) 3(011) 4(100) 5(101)

2-0 0(000)

6(110)

7(111)

*5*-3

*0(000)*

**Sra**

**slly**

**srlv**

**srav**

*S****hift l*eft** *logic*al

**Shift right** logical

*j*alr

Syscall

Break

*1(*001) jump

**re*gi*ster** 2(010) mfhi 3(011) | Mult 4(100) | *A*dd

mthi Multu

mflo **diy** Subtract

mtlo Divu Subu

Addu

And

**Or**

**Xor**

Not or (nor)

5(101)

Set l.t.

Set l.t. unsigned

6(110) 7(111)

Name

6 bits **op**

Field size R-format l-format **J-format**

Fields 5 bits 5 bits 5 bits 1 5 bits 6 bits

**rt**

***r*d |** shamt funct **rsrt**

address/Immediate target address

**rs**

**Commonts** All MIPS Instructions are 32 bits long Arithmetic instruction format

Transfer, branch, imm. format Jump Instruction format

**op**

**op**

**Name**

**| Register Number**

**Usage**

**Preserve on call?**

$zero

constant 0 (hardware)

n.a.

**n.a.**

$at $10 - $vi

$a0 - $a3

**res**erved for assembler

returned values

2-3

No

***4-*7**

Arguments

Yes

$t0 - $t7

8-15

temporaries

No

**16-23**

saved values

Yes

$50 - $s7 $t8 - $t9

$gp

temporaries

No

global pointer

Yes

$sp

24-25 28

29 . 30

31

stack pointer

frame pointer

return addr (hardware)

Yes **Yes**

**$fp** $ra

Yes