WizFi360 Hardware Design Guide
(Version 1.03)

WIZnet

Document Revision History

Date	Revision	Changes
2019-09-02	1.0	Initial Release
2019-09-03	1.01	Edited "Figure 6. UART Level Shifter"
2019-09-20	1.02	Added "4. PCB Footprint" Edited "Figure 2. Reference Schematic"
2019-11-27	1.03	Edited "Figure 1. WizFi360 Pinout" Edited "Table 1. Pin Definitions" Added "3.4 SPI"

Table of Contents

1. Overview

This document is the WizFi360 hardware design guide. If you are designing hardware using the WizFi360 you must refer to this document. This document includes a reference circuit diagram and a PCB guide.
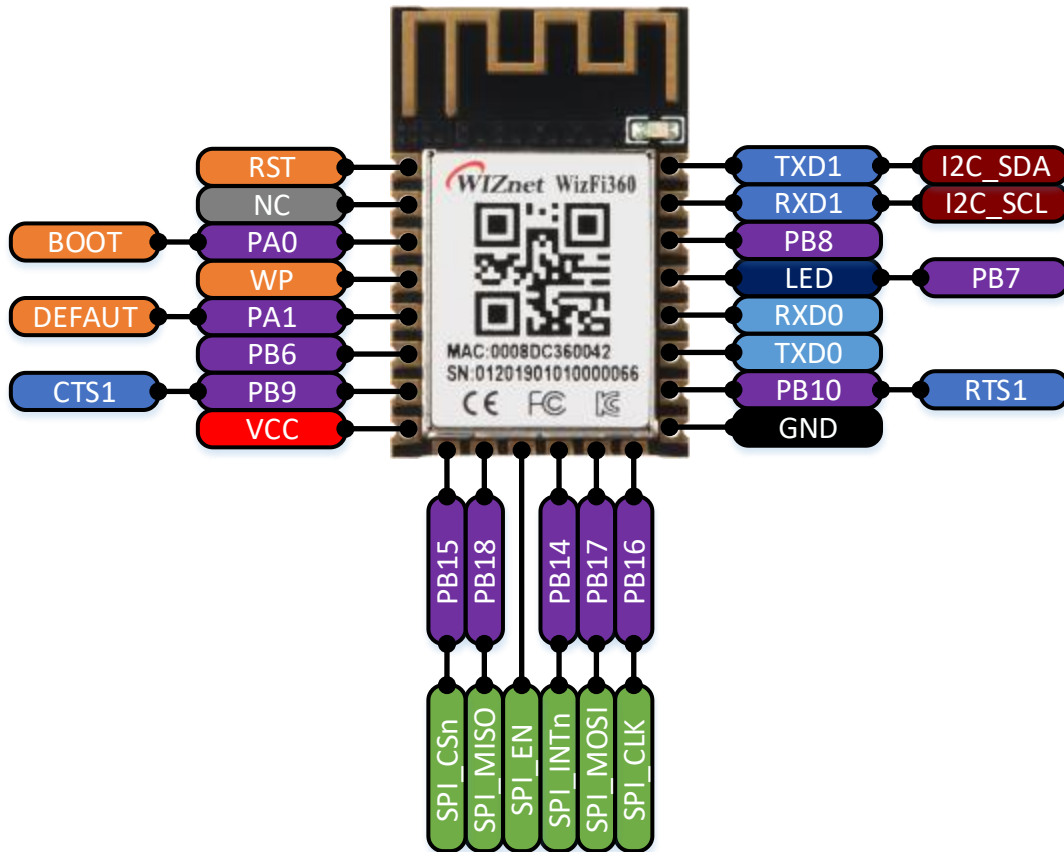
2. Pin Definitions

Figure 1. WizFi360 Pinout

No	Pin Name	Type	Pin Function
1	RST	I	Module Reset Pin (Active Low)
2	NC	-	Reserved
3	PA0	I/O	BOOT Pin (Active low) **When power on or reset is low, it operates in Boot mode.** In the normal operating mode, this pin can be controlled by AT command.
4	WP	I	WAKE-UP Pin (Active High) If the wake-up pin is high in Standby mode, the WizFi360 is reset to the normal operating mode.
5	PA1	I	Pull down over 3s for taking effect. **UART1's current parameter changes to default value (please refer to the AT+UART_CUR command in WizFi360 AT command manual).**

6	PB6	I/O	This pin can be controlled by AT command.
7	PB9	I	CTS Pin of UART1 If you don't use the CTS function, this pin can be controlled by AT command.
8	VCC	P	Power Pin (Typical Value 3.3V)
9	PB15	I/O	CSn Pin of SPI If you don't use the SPI function, this pin can be controlled by AT command.
10	PB18	I/O	MISO Pin of SPI If you don't use the SPI function, this pin can be controlled by AT command.
11	PB13 / SPI_EN	I/O	Enable Pin of SPI When power is applied or reset, this pin is checked to set the module mode. **Low or NC – UART Mode (Default)** High – SPI Mode
12	PB14	I/O	INTn Pin of SPI If you don't use the SPI function, this pin can be controlled by AT command.
13	PB17	I/O	MOSI Pin of SPI If you don't use the SPI function, this pin can be controlled by AT command.
14	PB16	I/O	CLK Pin of SPI If you don't use the SPI function, this pin can be controlled by AT command.
15	GND	I/O	Ground Pin
16	PB10	O	RTS Pin of UART1 If you don't use the RTS function, this pin can be controlled by AT command.
17	TXD0	O	TXD Pin of UART0
18	RXD0	I	RXD Pin of UART0
19	PB7	O	LED Light output (Active low). Go to Low while each TX/RX packet and then back to high. Note: It has been connected to onboard LED for WizFi360-PA
20	PB8	I/O	This pin can be controlled by AT command.
21	**RXD1**	**I**	**RXD Pin of UART1**
22	**TXD1**	**O**	**TXD Pin of UART1**

Table 1. Pin Definitions

*Note: UART1 is used for AT command and data communication. UART0 is used for debugging and firmware upgrade.

2.1. Initial Value of GPIO Pins

This is the initial value of GPIO when using AT command to use GPIO on the WizFi360.

Pin Name	Initial Mode	Initial Value
PA0	I	High
PB6	O	Low
PB9	O	Low
PB15	O	Low
PB18	O	Low
PB14	O	Low
PB17	O	Low
PB16	O	Low
PB10	O	Low
PB07	O	Low
PB08	O	Low

Table 2. Initial Value of GPIO Pins

3. Circuit

3.1. System

The WizFi360 has a very simple circuit. You can connect power to the WizFi360 and send and receive data through UART1. And you have to pay attention to the four pins.
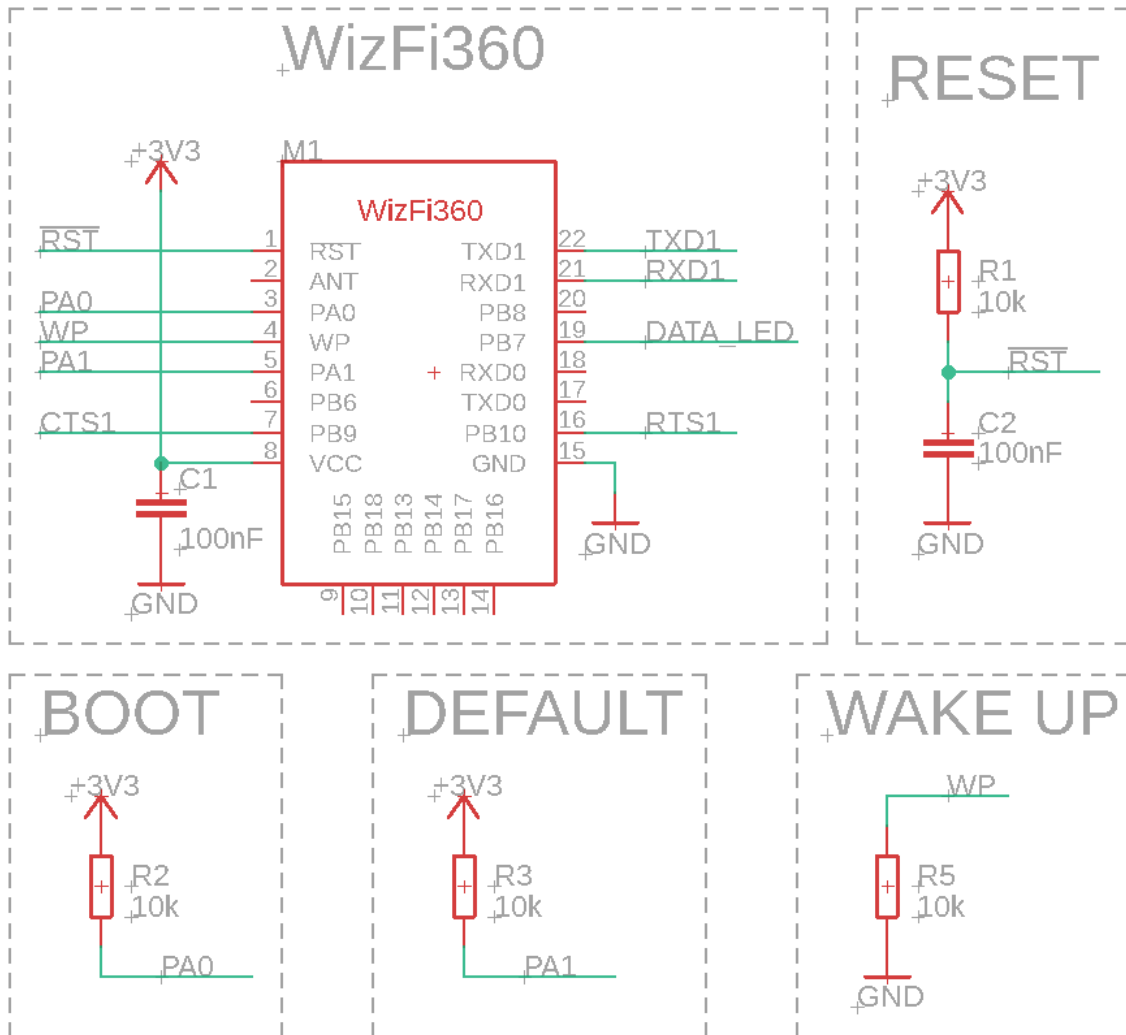
Figure 2. Reference Schematic

- **Reset**

Reset circuit offers to design with RC circuit. WizFi360 reset automatically by low level power. If RESET pin controlled by external circuit, the WizFi360 will reset when the level is below 2.0V. The low level needs to last more than 100μs.

- **PA0**

PA0 circuit offers to design 10k pull-up. PA0 is used as a boot pin, but it's use unlikely for normal users. This pin is used at the factory stage. (Module production)

- **PA1**

PA1 circuit offers to design 10k pull-up. If PA1 is Low for 3 seconds, UART1's current parameter changes to default value (please refer to the AT+UART_CUR command in WizFi360 AT command manual).

- **WP**

WP circuit offers to design user configuration. You must control this pin if you are using standby mode. If this pin is high in Standby mode, the WizFi360 is reset to the normal operating mode.

3.2. Power

WizFi360 requires the use of a power supply capable of supplying 3.0V to 3.6V and more than 500mA. Because WizFi360 operates normally from 3.0V to 3.6V, it consumes up to 230mA of instantaneous current. The wiring width should not be less than 30mil.

The power stabilizing capacitor (100nF) should be placed close to the VCC pin.

3.3. UART

The WizFi360 supports UART communication mode. When the power is turned on or reset, If the PB13 pin remains High or NC, it operates in UART communication mode.
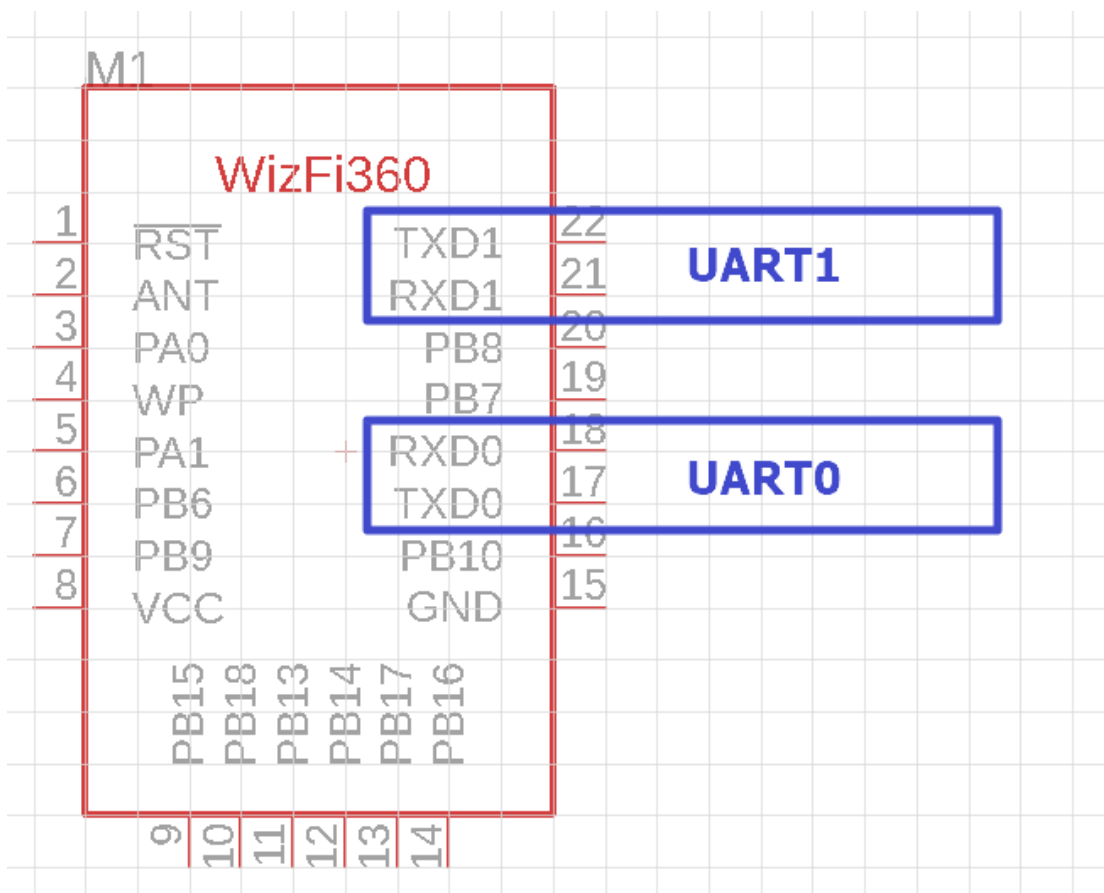
Figure 3. UART

- **UART1**

UART1 is the main communication UART. AT command communication is possible with UART1 and data communication is possible.

- **UART0**

UART0 is not available to normal users. This UART is used at the factory stage (Module production) and intended for internal firmware developers of the WizFi360.

3.4. SPI

The WizFi360 supports SPI communication mode. When the power is turned on or reset, If the **PB13(SPI_EN)** pin remains low, it operates in SPI communication mode.
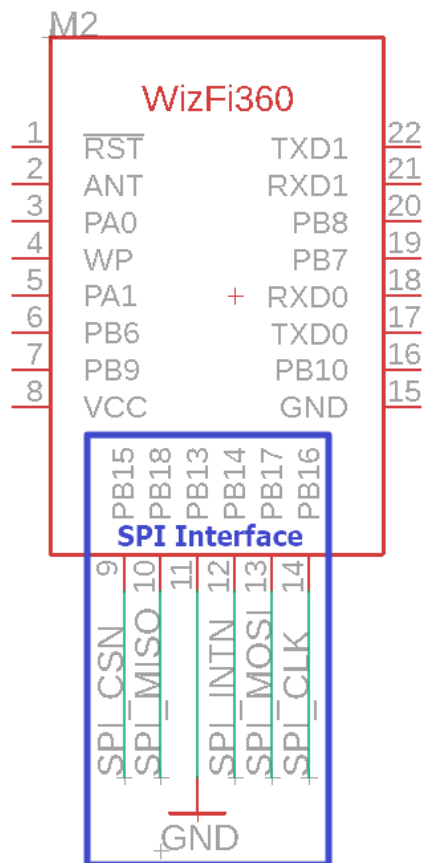

Figure 4. SPI Interface

3.5. ETC

This session is an additional circuit guide for using the WizFi360. You don't have to keep this session. But if you need it, you design it.

● **UART Flow Control**

If you want to use UART Flow Control, you need to design a circuit as shown in Figure 3. PB9 is CTS1, PB10 is RTS1.
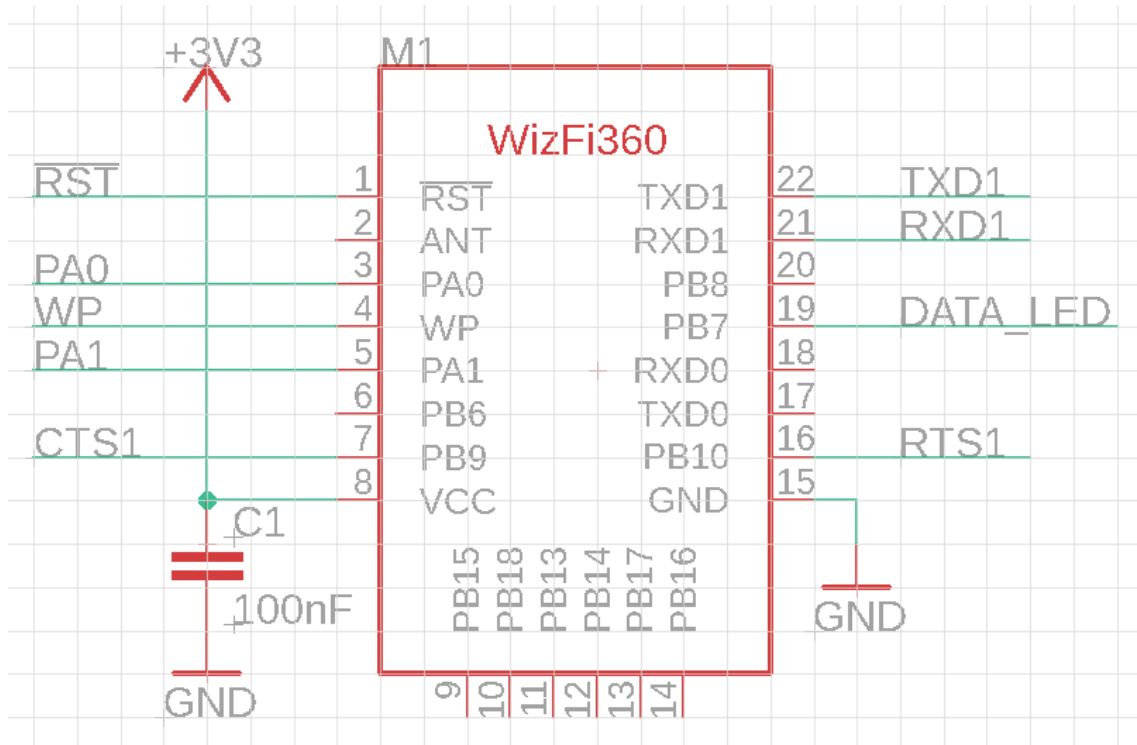
Figure 5. UART Flow Control

● **UART Level Shifter**

The UART voltage on the WizFi360 is 3.3V. However, your MCU may not have a voltage of 3.3V. If so you need a Level Shifter to connect the WizFi360 to your MCU. You can design a Level Shifter circuit by referring to Figure 4. Connect your MCU's UART voltage to the VCCIO at Figure 4.
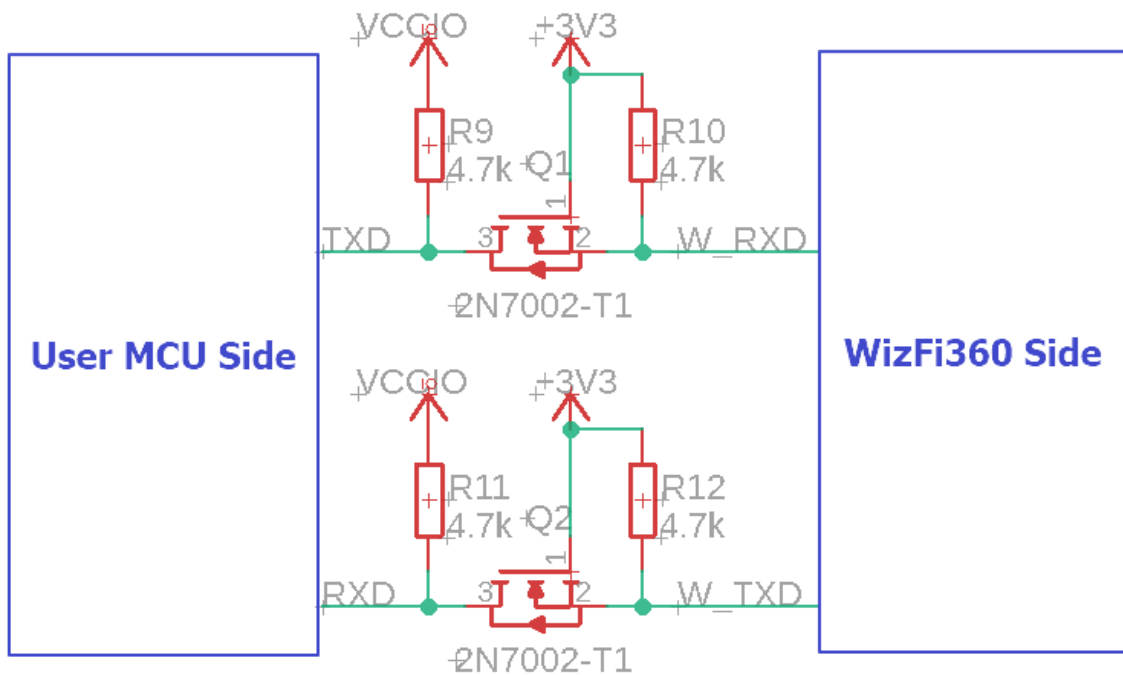
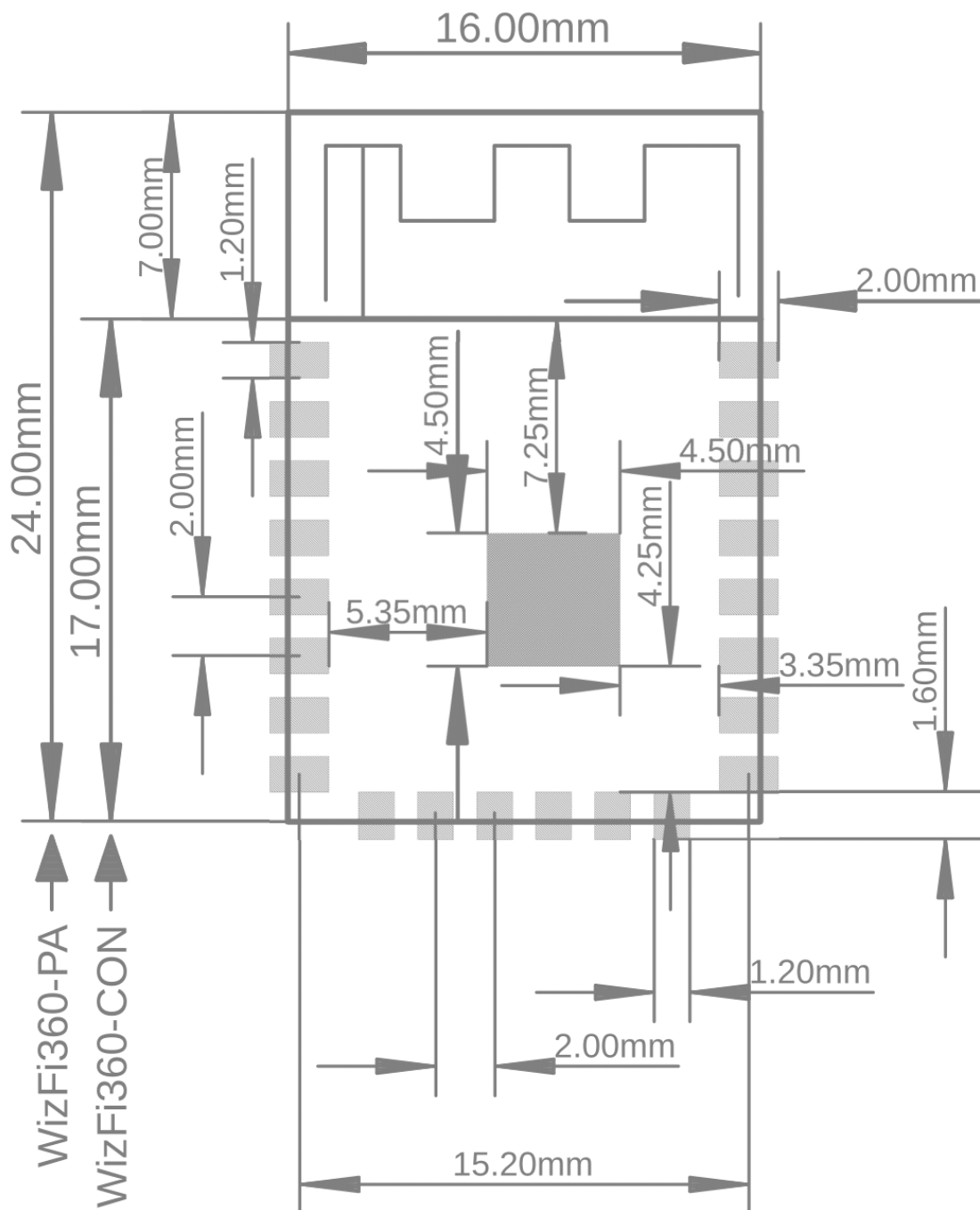

Figure 6. UART Level Shifter

4. PCB Footprint

Figure 7. Recommended PCB Land Pattern of WizFi360

5. PCB layout

- Power wiring width should not be less than 30mil.
- Except for the antenna portion of WizFi360, the bottom layer of the shield can must have a GND plane.
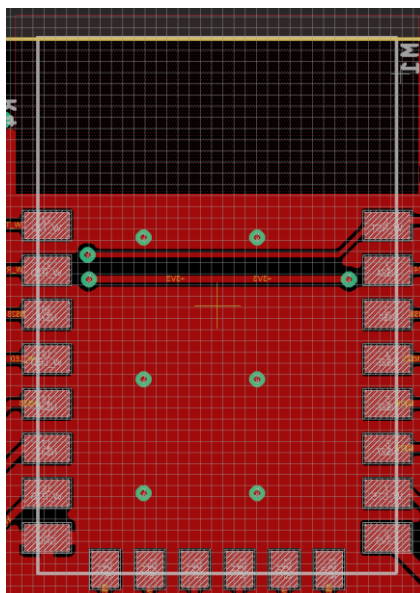

Figure 8. GND

- Figures. 6 and Figures. 7 are 2 antenna placement which can best performance of antenna. We suggest customers to choose one of these 2 modes to design the placement. For the second placement mode, PCB antenna should be at least 5.0mm from both sides of the bottom board.
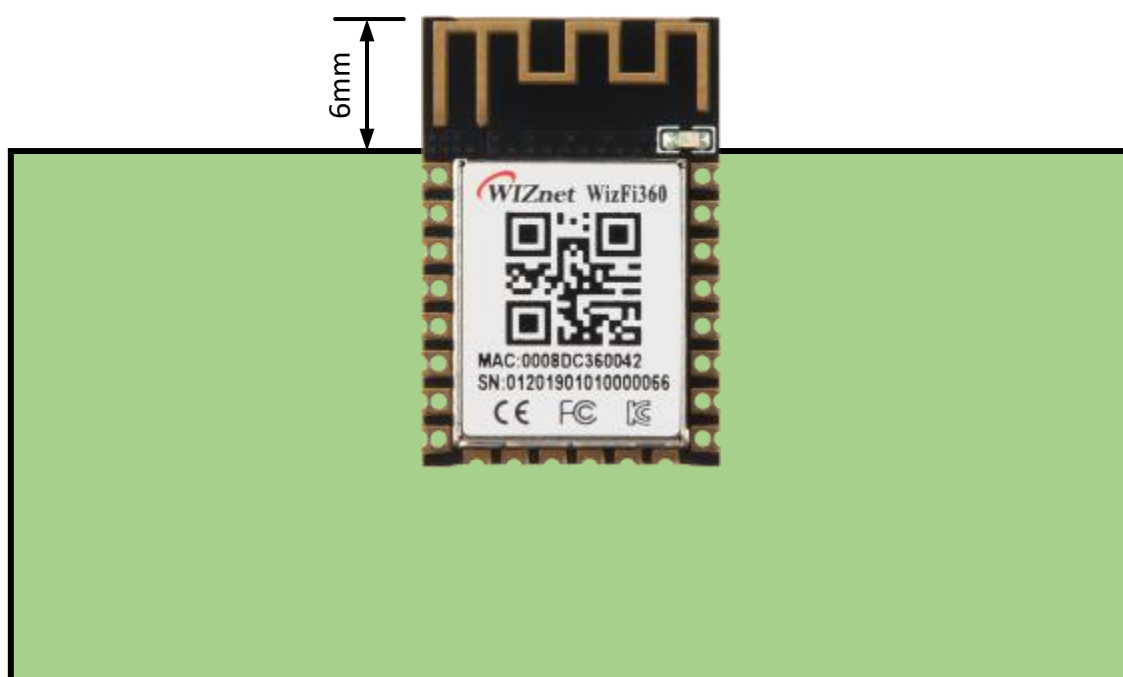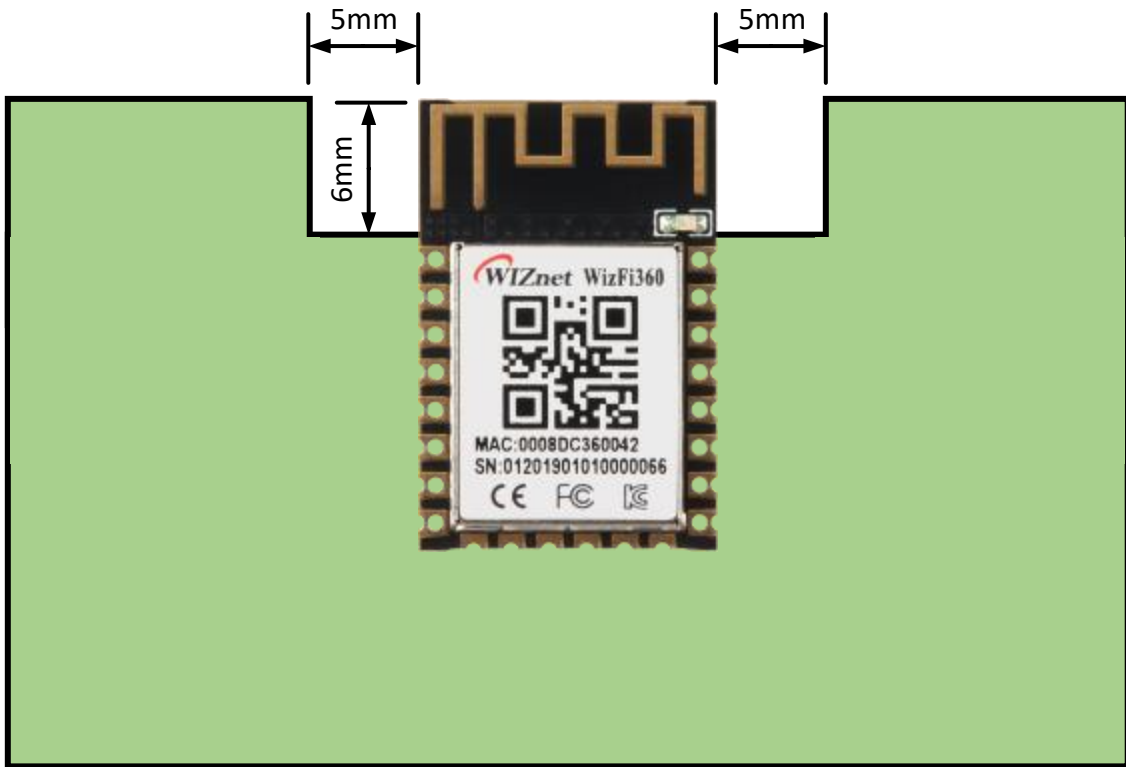

Figure 9. Best Placement 1

Figure 10. Best Placement 2

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