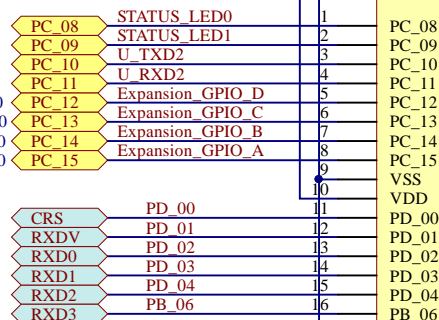


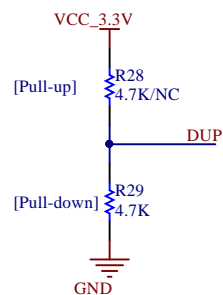
PHY link status
TCP connection status

Optional_I2C_SCL0
Optional_I2C_SDA0
Optional_SPI_SSEL0
Optional_SPI_SCLK0
Optional_SPI_MISO0
Optional_SPI_MOSI0



MDIO(PB_14),MDC(PB_15) pin is should be handled as GPIOs.

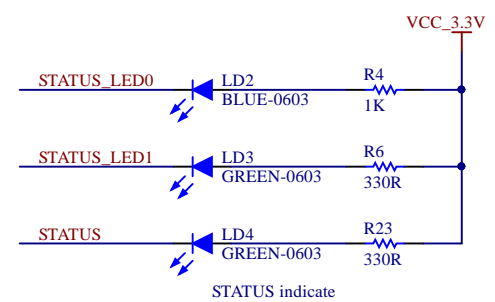
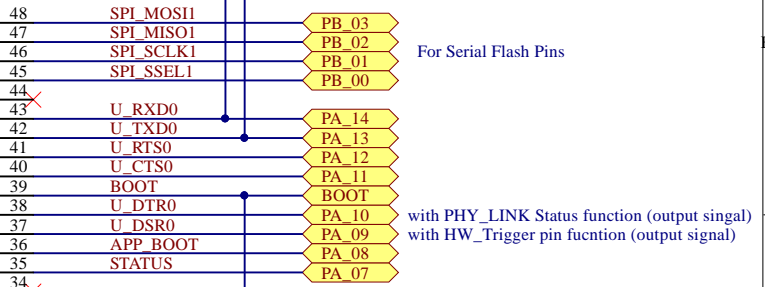
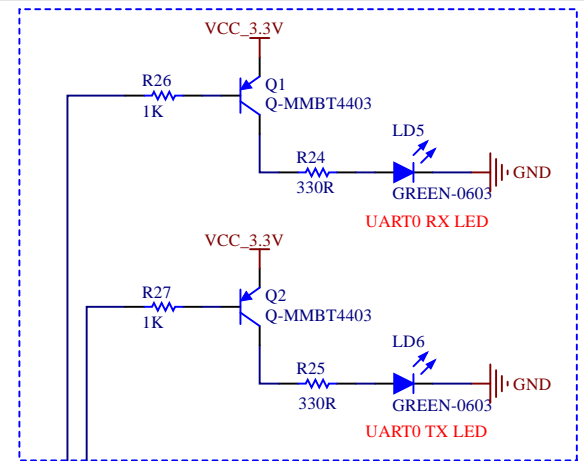
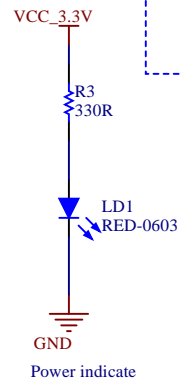
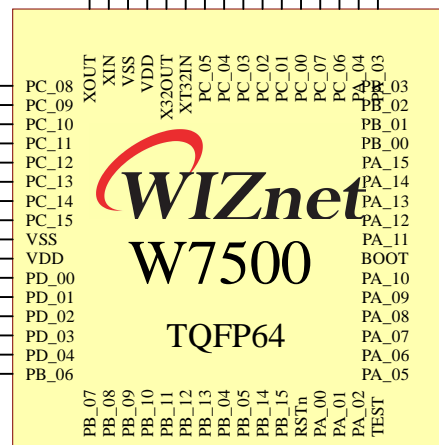
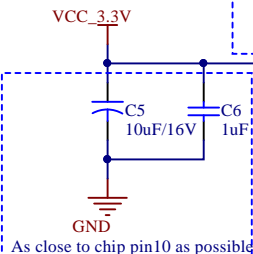
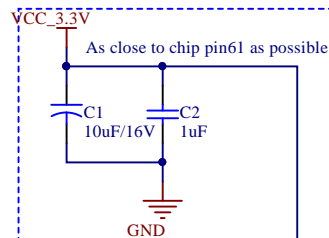
PA_00 is PHY LINK check pin(input). This pin checks PHY link from peer
This pin should be connected to the LINK status signal of the RJ-45.




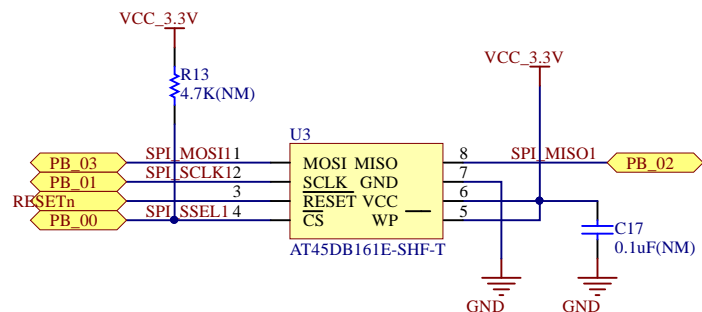
To use Half mode, you must set up pull up.
To use Full mode, you must set up pull down.(Default)

There is no pull-up or pull-down in the circuit, make sure W7500 internal register is set as below
1. Set as GPIO (Alternative function)
2. Set as Input pin. (IE in PADCON)
3. Set as Pull up or pull down. (PADCON)

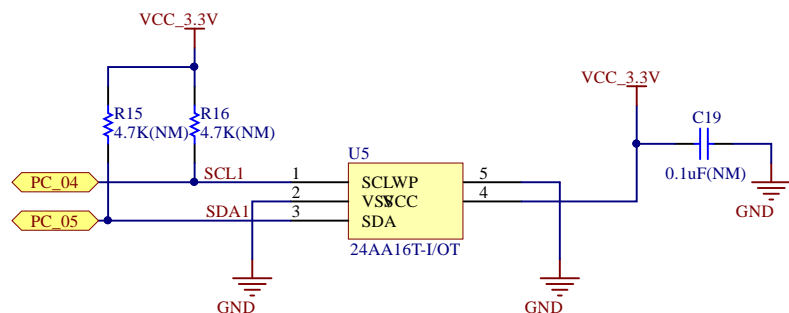
For more information, refer to the W7500 reference manual.



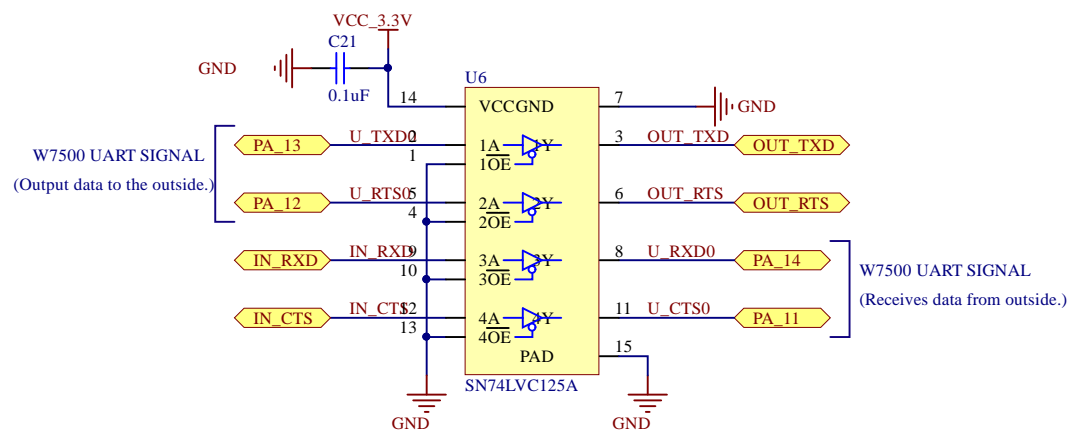
Title WIZ750SR-100			WIZnet Co., Ltd. 5F, Humax Village Hwangseaul-ro, Bundang-gu Seongnam-si, Gyeonggi-do South Korea		
Size: A4	Number:*	Revision:V1.1			
Date: 2018-04-17		Sheet 1 of 5			
Team: CS	Drawn By: Edward				



Serial Data Flash(Not Mount)




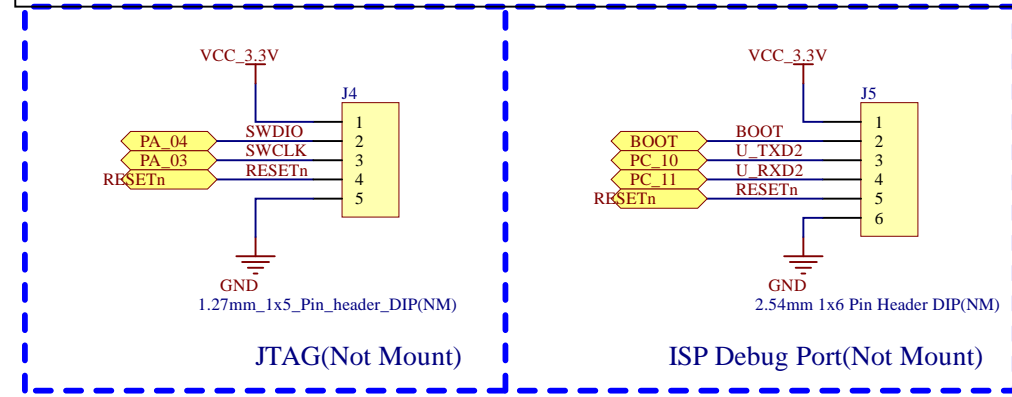
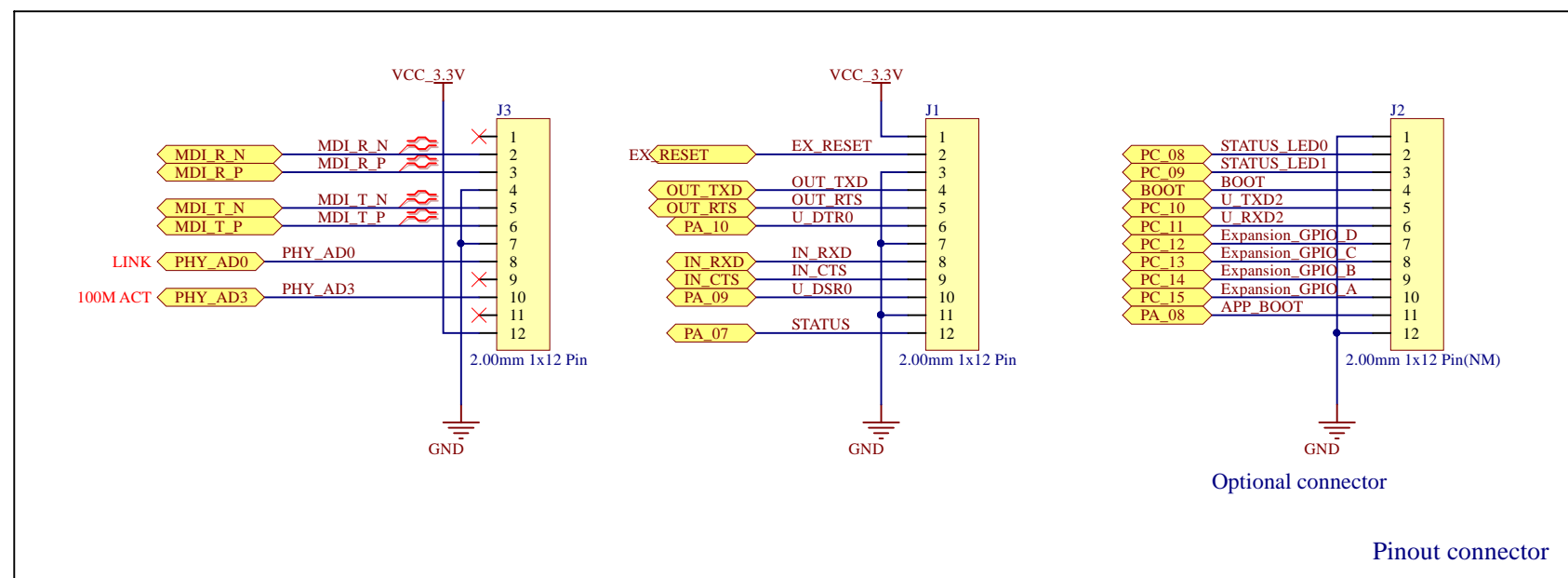
EEPROM(Not Mount)




The buffer is used for impedance separation purposes.

UART CONVERSION

Title WIZ750SR-100			WIZnet Co., Ltd. 5F, Humax Village Hwangseaul-ro, Bundang-gu Seongnam-si, Gyeonggi-do South Korea	
Size: A4	Number:*	Revision: V1.1		
Date: 2018-04-17		Sheet 3 of 5		
Team: CS	Drawn By: Edward			



Title WIZ750SR-100			WIZnet Co., Ltd. 5F, Humax Village Hwangseaul-ro, Bundang-gu Seongnam-si, Gyeonggi-do South Korea	
Size: A4	Number:*	Revision:V1.1		
Date: 2018-04-17		Sheet 4 of 5		
Team: CS	Drawn By: Edward			

