W7500 Document History

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1 Reference Document History Information

Version	Date	Descriptions
Ver. 1.0.0	01MAY2015	1. Initial Release
Ver. 1.0.1	12JUNE2015	1. Corrected typing error: I2C block
Ver. 1.0.2	17AUG2015	1. Deleted 1.1 List of abbreviations. 2. Corrected Register acronym in Table 3. Offset Address for Common Register : PSID -> PSIDR 3. Deleted PP mode with Figure 6 operation of boot code & Table 5 operation of mode selection in Chapter 8. Booting Sequence. 4. Changed words : polling INT bit -> checking INT register in 17.3.2 Operation ADC with interrupt. 5. Deleted unneeded content in 9.2.2 Read operations. 6. Corrected nUARTRTS asserted condition : HIGH -> LOW , Corrected the sentence, 'When nUARTCTR is re-asserted(to a low value) the transmitter sends the next byte.' : de-asserted -> re-asserted in 22.3.4 Hardware flow control. 7. Added contents about 19.4.7 Timer0_0 Background Load Register(DUALTIMER0_0TimerBGLoad) / 19.6.7/ 19.10.7/ 19.12.7.
Ver. 1.0.3	08JAN2016	1. Bit rate in SPI interface changed 'up to 2MHz and higher' to 'up to 20MHz. 2. Bit rate generation example changed in 23.3.11 Programming the SSPCR1 Control Register.
Ver. 1.0.4	08MAR2016	1. In , GPIO0,1,2,3 changed to GPIOA,B,C,D
Ver. 1.0.5	22APR2016	1. Added UART2 Description and Register in 23 Universal Asynchronous Receive Transmit(UART2) 2. Deleted the greater part of I^2C, set up the Errata Sheet Link (http://wizwiki.net/wiki/doku.php?id=products:w7500:documents)
Ver. 1.0.6	06JAN2017	1. Corrected Sn_DHAR1 bit R/W information

Ver. 1.0.7	02MAR2017	1. Modified Mode Register and Changed MD in simplified form to MR in 7.5.8 MR(Mode Register)
Ver. 1.0.8	21MAR2017	1. Modified the Example value in 7.5.2 TCKCNTR(Ticker Counter Register).

2 Datasheet Document History Information

Version	Date	Descriptions
Ver. 1.0.0	01MAY2015	1. Initial Release
Ver. 1.0.1	12JUNE2015	1. Corrected typing error: I2C block
Ver. 1.0.2	17AUG2015	1. Deleted 1.1 List of abbreviations. 2. Corrected Register acronym in Table 3. Offset Address for Common Register : PSID -> PSIDR. 3. Deleted PP mode with Figure 6 & Table 5 in 8. Booting Swquence. 4. Changed words : polling INT bit -> checking INT register in 17.3.2 Operation ADC with interrupt. 5. Deleted unneeded content in 9.2.2 Read operation. 6. Corrected nUARTRTS asserted condition : HIGH -> LOW , Corrected the sentence, 'When nUARTCTR is re-asserted(to a low value) the transmitter sends the next byte.' : de-asserted -> re-asserted in22.3.4 Hardware flow control. 7. Deleted RTCCLK.
Ver. 1.0.3	14DEC2015	1. Corrected Package diagram error.
Ver. 1.0.4	08JAN2016	1. Bit rate in SPI interface changed 'up to 2MHz and higher' to 'up to 20MHz'. 2. Bit rate generation example changed in 23.3.11 Programing the SSPCR1 Control Register.
Ver. 1.0.5	08MAR2016	1. In 2.2.2 Memory map, GPIO 0,1,2,3 changed to GPIO A,B,C,D.
Ver. 1.0.6	03JUN2016	1. Added UART2 description in 23 Universal Asynchronous Receive Transmit 2(UART2).

		2. Deleted the greater part of I^2C with data receiving problem, set up the Errata Sheet Link. (http://wizwiki.net/wiki/doku.php?id=products:w7500:documents)
Ver. 1.0.7	13JAN2017	1. Corrected External Oscillator Clock circuit information (see 10.3.1 External Oscillator Clock). 2. Corrected Package Footprint information (see Figure 76. Footprint Information).
Ver. 1.0.8	09FEB2017	1. Add W7500 Pin Assignment (see 25 Pin Assignment).
Ver. 1.0.9	16FEB2017	1. Corrected W7500 Pin Assignment the wrong Type.
Ver. 1.1.0	10APR2017	1. Corrected W7500 System Architecture (see Figure 1. W7500 System Architecture). 2. Add 5V VDDH case in 26.3.1 DC Specification. 3. Add 26.3.2 AC Specification.

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