7500P PHY Reference

Version 1.0.1

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1 Documentation conventions

1.1 Register Bit Conventions

Each register is shown with a key indicating the accessibility of the each individual bit, and the initial condition:

Key	Bit Accessibility
RW	Read/Write
SC	Self-Clearing
RO	Read Only
LL	Latching Low
LH	Latching High
(TP)	for twisted pair operation
(FX)	for fiber operation
(e-fuse)	only available for IP101G(dice)

2 Register Descriptions

2.1 Introduction

7500P PHY is an IEEE 802.3/802.3u compliant single-port Fast Ethernet Transceiver for both 100Mbps and 10Mbps operation. 7500P PHY, IP101G, has MII(Media Independent Interface) and it supports MII Register.

2.2 Register Access

7500P PHY MII Register can be accessed through MDC/MDIO. 7500x Library supports Software MDC/MDIO to access 7500P PHY MII Register.

Please refer W7500x_Library_Examples/ioLibrary/MDIO.

The more details of MDC/MDIO Format is here(3. MII Register Access).

2.3 Register Map

Table 1 Register Map is a port of IP101G Registers.

Table 1 Register Map

Register	Description	Default
0x20	Page Control Register	0x0010
0x00	Control Register	0x3100
0x01	Status Register	0x7849

2.3.1 Register Page mode Control Register

This is the description of MII register 0x20, page control register.

The other bits are reserved. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

Table 2 Page Mode Control Register

PHY	MII	ROM	R/W	Description	Default
	20[4:0]		R/W	REG16~31_Page_Sel[4:0] Register Page Select	0x10

2.3.2 Control Register

This is the description of MII register 0x00, control register.

Table 3 Control Register

Bit	Name	Description	Default value (h):3100
15	Reset	When set, this action will bring both status and control register of the PHY to default state. This bit is self-clearing. 1 = Software reset 0 = Normal operation	0, RW/SC
14	Loopback	This bit enables loopback of transmit data to the receive data path, i.e., TXD to RXD. 1 = enable loopback 0 = normal operation	0, RW
13	Speed Selection	This bit sets the speed of transmission. 1 = 100Mbps 0 = 10Mbps After completing auto-negotiation, this bit will reflect the speed status.(1: 100Mbps, 0: 10Mbps)	1, RW
12	Auto-Negotiation Enable	This bit determines the auto-negotiation function. 1 = enable auto-negotiation; bits 13 and 8 will be ignored. 0 = disable auto-negotiation; bit 13 and 8 will determine the link speed and the data transfer mode, under this condition.	1, RW(TP) 0, RO(FX)
11	Power Down	This bit will turn down the power of the PHY chip and the internal crystal oscillator circuit if this bit is enabled. The MDC and MDIO are still activated for accessing to the MAC. 1 = power down 0 = normal operation	0, RW
10	Isolate	1 = electrically Isolate PHY from MII but not isolate MDC and MDIO	0, RW
9	Restart Auto-Negotiation	This bit allows the auto-negotiation function to be reset. 1 = restart auto-negotiation 0 = normal operation	0, RW/SC
8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 12 = 0) 1 = full duplex 0 = half duplex	1, RW

		After completing auto-negotiation, this bit will reflect the duplex status.(1:Full duplex, 0:Half duplex)	
7	Collision Test	1 = enable COL signal test	0, RW
6:0	Reserved		0, RO

2.3.3 Status Register

This is the description of MII register 0x01, status register.

Table 4 Status Register

Bit	Name	Description/usage	Default value (h):3100
15	100Base-T4	1 = enable 100Base-T4 support 0 = suppress 100Base-T4	0, RO
14	100Base-TX Full Duplex	1 = enable 100Base-TX full duplex support 0 = suppress 100Base-TX full duplex support	1, RO
13	100Base-TX Half Duplex	1 = enable 100Base-TX half duplex support 0 = suppress 100Base-TX half duplex support	1, RO
12	10Base-T Full Duplex	1 = enable 10Base-T full duplex support 0 = suppress 10Base-T full duplex support	1, RO
11	10Base-T Half Duplex	1= enable 10Base-T half duplex support 0 = suppress 10Base-T half duplex support	1, RO
10:7	Reserved		
6	MF Preamble Suppression	The IP101G will accept management frames with preamble suppressed. The IP101G accepts management frames without preamble. A Minimum of 32 preamble bits is required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE802.3u specifications.	1, RO
5	Auto-Negotiation Complete	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	0, RO
4	Remote Fault	1 = remote fault condition detected(cleared on read)	0, RO/LH

		0 = no remote fault condition detected	
3	Auto-Negotiation	1 = able to perform auto-negotiation 0 = unable to perform auto-negotiation	1, RO
2	Link Status	1 = valid link established 0 = no valid link established	0, RO/LL
1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	0, RO/LH
0	Extended Capability	1 = extended register capability 0 = basic register capability only	1, RO

3 MII Register Access

W7500P PHY's MII register can be accessed by MDC and MDIO. Users can control MDC/MDIO through GPIOx. MDC/MDIO format is shown in the below table. To access MII register in W7500P PHY, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When this interface is idle, MDIO is in high impedance.

Table 5 Interface Format

Frame format	<Idle><start><op code><PHY address><Register address><turnaround><data><Idle>
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0><$b_{15}b_{14}b_{13}b_{12}b_{11}b_{10}b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10><$b_{15}b_{14}b_{13}b_{12}b_{11}b_{10}b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$><Idle>

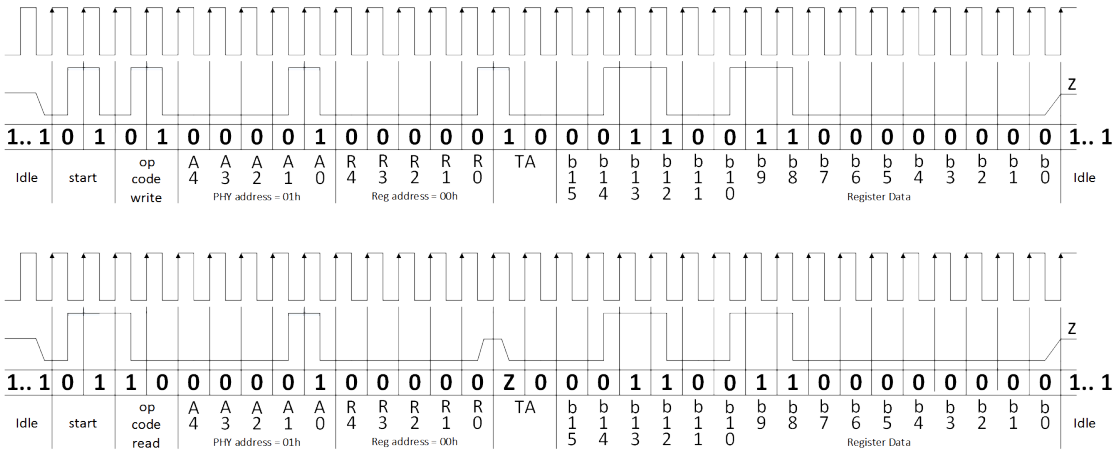

Figure 1 MDC/MDIO Format

3.1 How to Access PHY MII Register

- How to Write Access

```
{
START:
        // Set GPIO(Value, Length)
        Set GPIO(0x05, 4);   // Start bits 01, Write Access 01
        Set GPIO(PHY address, 5);   // PHY address
        Set GPIO(REG address, 5);   // MII register
        Set GPIO(0x02, 2);   // turnaround bits 10
        Set GPIO(DATA, 16);
}
```

- How to Read Access

```
{
START:
        // Set GPIO(Value, Length)
        Set GPIO(0x06, 4);   // Start bits 01, Read Access 10
        Set GPIO(PHY address, 5);   // PHY register
        Set GPIO(REG address, 5);   // MII register
        Set GPIO(CLR, 2);   // turnaround bits high impedance
        Val = Get GPIO(DATA, 16);
}
```

- How to get PHY address

```
{
START:
        // Loop to find PHY address
        for(i=0; i<8; i++)
        {
            Set GPIO(0x05, 4);   // Read Access
            Set GPIO(i, 5);   // PHY address
            Set GPIO(0x01, 5);   // PHY Status Register (0x01)
            Set GPIO(CLR, 2);    // turnaround bits high impedance
            Val = Get GPIO(DATA, 16);   // To check LINK bit in PHY Status Register.
            if(Val != 0) return i;   // i is PHY address
        }
}
```

Document History Information

Version	Date	Descriptions
Ver. 1.0.0	19APR2016	Initial Release
Ver. 1.0.1	31JAN2018	1. Add 2.2 Register Access 2. Add 3 MII Register Access