FPGA LAB-Challenge Problem 1

ANNU-EE21RESCH01010

Download all latex-tikz codes from

https://github.com/annu100/FPGA−LAB

1 Problem Statement

Obtain and implement an algorithm to convert any truth table to NAND logic.

2 Solution

2.1 Algorithm

1. Take the min terms for which the output in truth table will be 1.
2. Write SOP form of each minterms.
3. Take complement of each SOPs.
4. Multiply all the obtained complemented minterm SOPs.
5. Take the complement of above multiplication of SOP result.
6. THIS IS OUR OBTAINED NAND LOGIC.

2.2 Explanation using one example

For example the given truth table is as below

From truth table, the min terms for which $F = 1$ are 0,1,3,7.

STEP:1

Take complement of each SOPs.

Complemented SOPs are

A	B	C	F(A,B,C)	SOP(Minterm)
0	0	0	1	$\bar{A}\ \bar{B}\ \bar{C}$
0	0	1	1	$\bar{A}\ \bar{B}$ C
0	1	0	0	-
0	1	1	1	$\bar{A}$ BC
1	0	0	0	-
1	0	1	0	-
1	1	0	0	-
1	1	1	1	ABC

Table 1: Given Truth table

$$(\bar{A}\bar{B}\bar{C})', \tag{2.2.1}$$
$$(\bar{A}\bar{B}C)', \tag{2.2.2}$$
$$(\bar{A}BC)', \tag{2.2.3}$$
$$(ABC)' \tag{2.2.4}$$

STEP 2:Multiply all the obtained COMPLEMENTED minterm SOPs

$$K = (\bar{A}\bar{B}\bar{C})' \times (\bar{A}\bar{B}C)' \times (\bar{A}BC)' \times (ABC)' \tag{2.2.5}$$

STEP 3:Take the complement of above multiplication of SOP result.

$$Result = K' \qquad = ((\bar{A}\bar{B}\bar{C})' \times (\bar{A}\bar{B}C)' \times (\bar{A}BC)' \times (ABC)')' \tag{2.2.6}$$

Now we can draw the logic circuit using NAND gates as below.

3 Conclusion

Following the above given steps, we can get nand logic very easily for any given truth table problems.

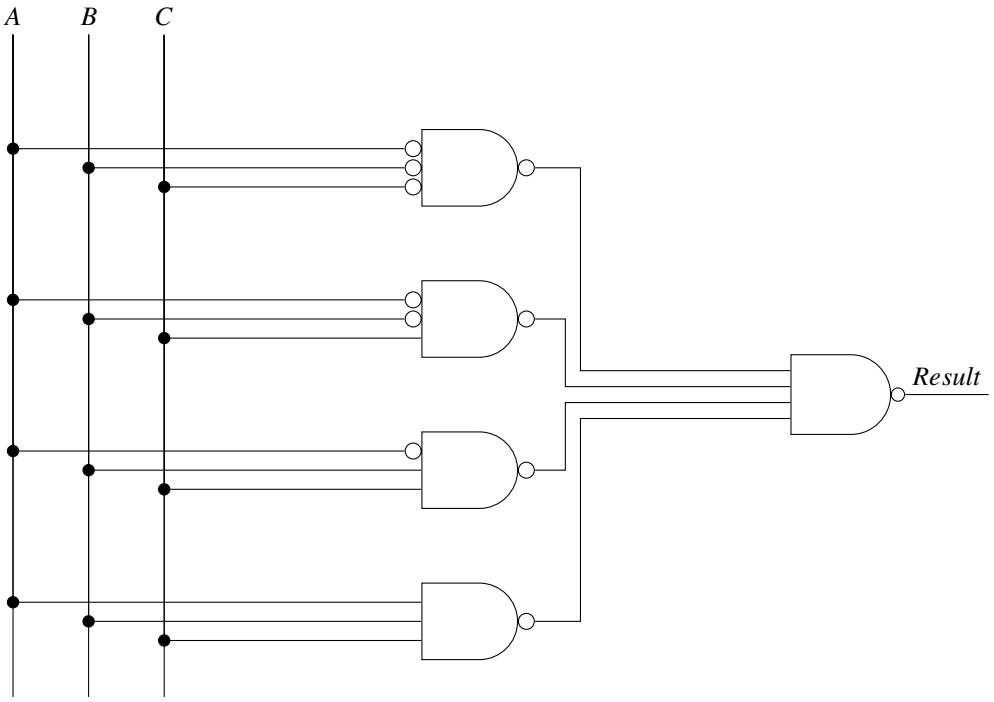

Figure 1: Logic Circuit using NAND gates