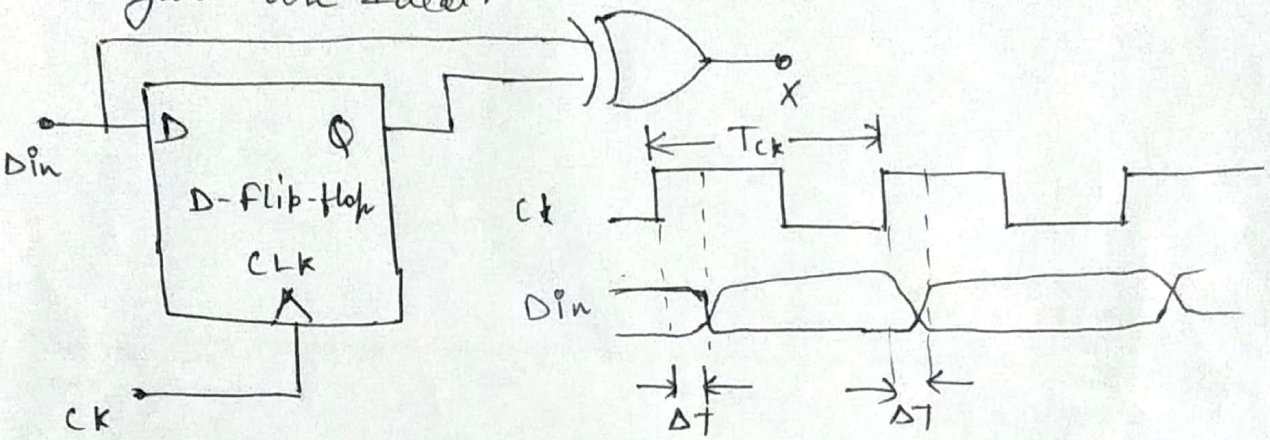
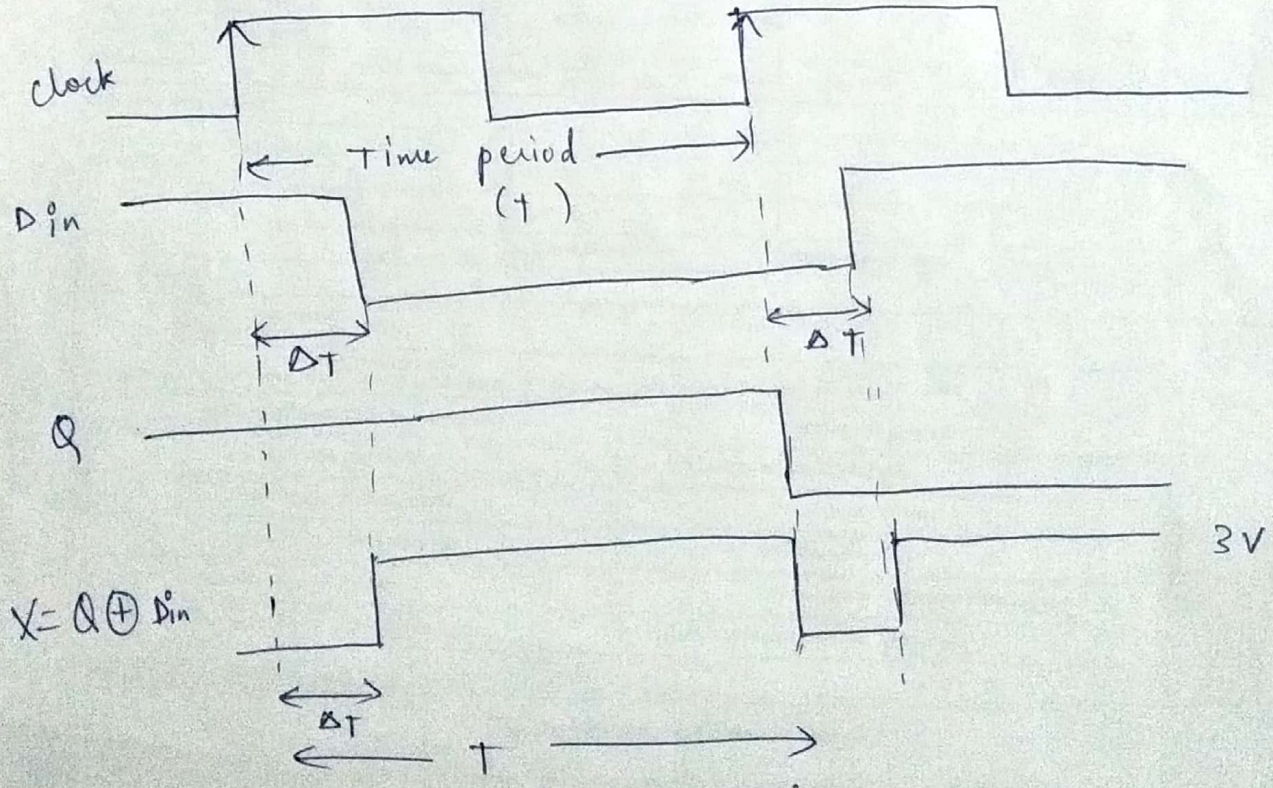
Q. In the circuit shown below, a (+)ve edge triggered D flip-flop is used for sampling input data D_{in} using clock CK. The X-OR gate outputs 3.3 Volts for logic HIGH & 0 volts for logic LOW levels. The data bit & clock periods are equal and the value of $\Delta T / T_{CK} = 0.15$, where the parameters ΔT & T_{CK} are shown in the figure. Assume that the flip-flop & X-OR gate are Ideal.



If probability of input data bit (D_{in}) transition in each clock period is 0.3, the average value (in volts, accurate to 2 decimal places) of the voltage at node X, is 0.8415 V.

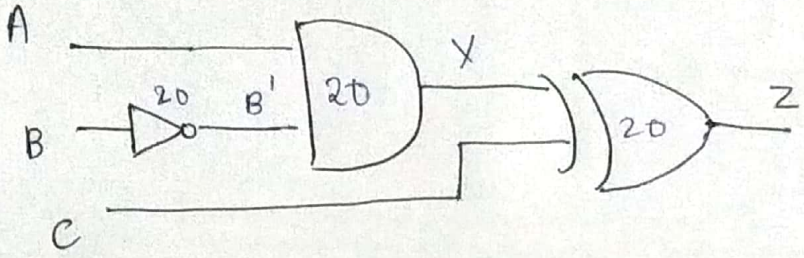


Voltage @ X = $\left(\frac{T-\Delta T}{T}\right)$ X Probability X voltage value

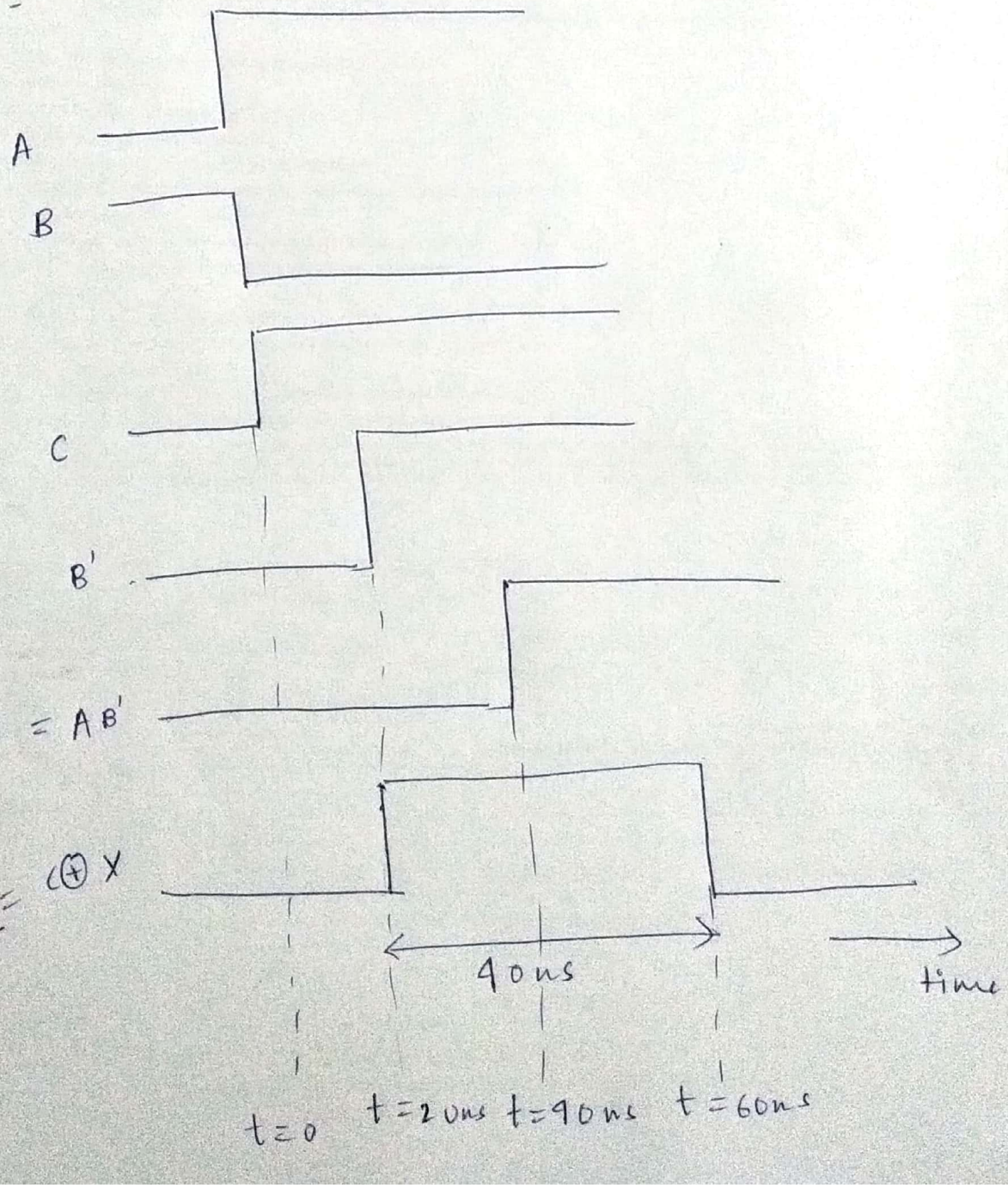
$= \left(1-\frac{\Delta T}{T}\right) \times 0.3 \times 3.3 = (1-0.15) \times 0.3 \times 3.3$

$= 0.8415$ V //

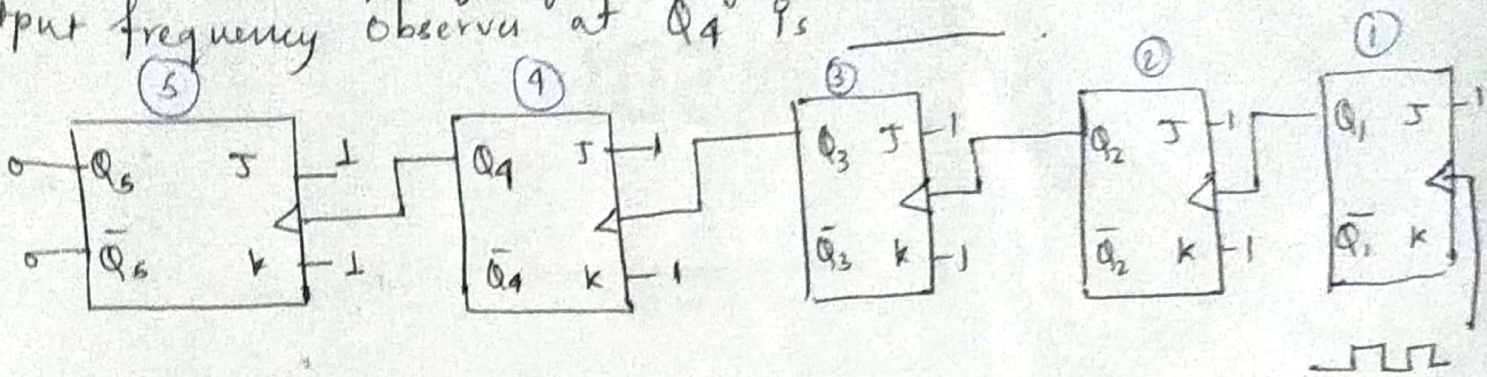
Q. All the logic gates shown in the figure have a propagation delay of 20ns. let A = C = 0 & B = 1 until time t = 0. At t = 0, all the inputs flip (i.e A = C = 1 & B = 0) & remain in that state. For t > 6, output Z = 1 for a duration (in ms) of 40ns →∞



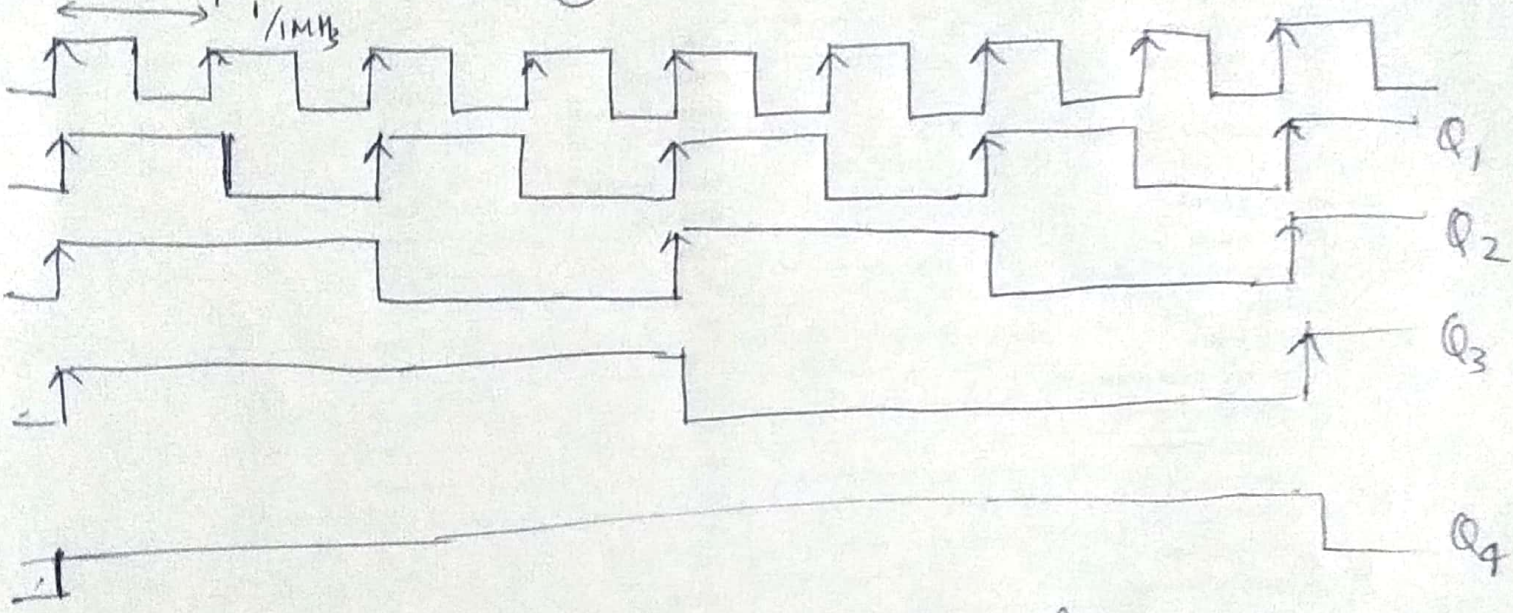
Sol^n -



Q. The input frequency for the given counter is 1 MHz, the output frequency observed at Q_4 is _____.



let i/p clock at (1) -



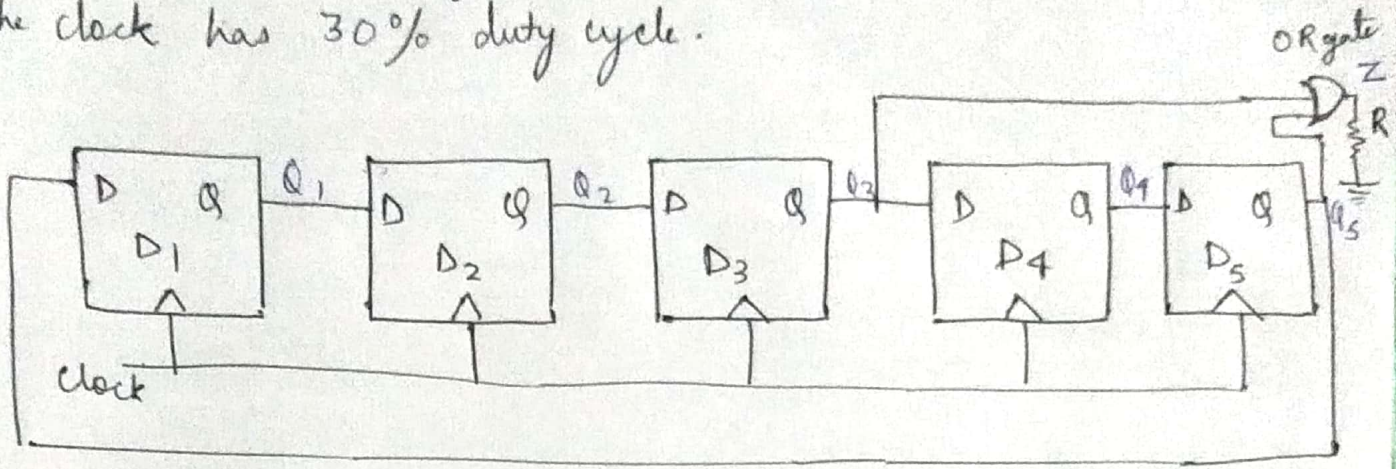
time period doubles for each successive flip-flop pass. It is being depicted in above graphs.

So, frequency gets divided by 2 for each successive f/f pass.

∴ freq. @ o/p of 4th f/f or Q_4

$$= \frac{1\ MHz}{2^4} = 62.5\ kHz$$

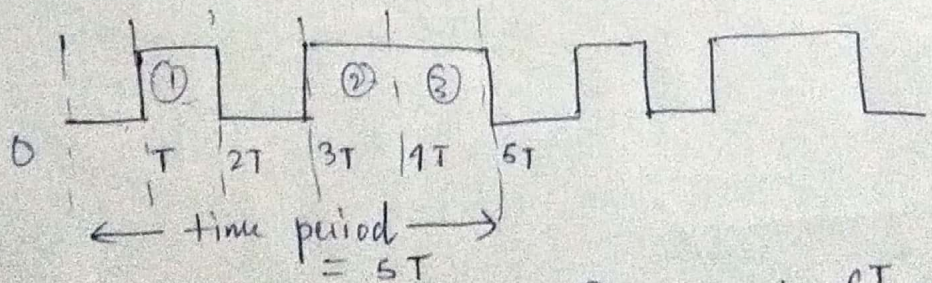
Q. Assume that all the digital gates in the circuit shown in the figure are ideal, the resistor $R = 10\,k\Omega$ and the supply voltage is 5 V. The D flip-flops D_1, D_2, D_3, D_4 & D_5 are initialized with logic values 0, 1, 0, 1 and 0 respectively. The clock has 30% duty cycle.



The average power dissipated (in mW) in the resistor R is _____.

$$Z = Q_3 + Q_5$$

Clk	Q_1	Q_2	Q_3	Q_4	Q_5	O/P = Z
0	0	1	0	1	0	0
1	0	0	1	0	1	1
2	1	0	0	1	0	0
3	0	1	0	0	1	1
4	1	0	1	0	0	1
5	0	1	0	1	0	0



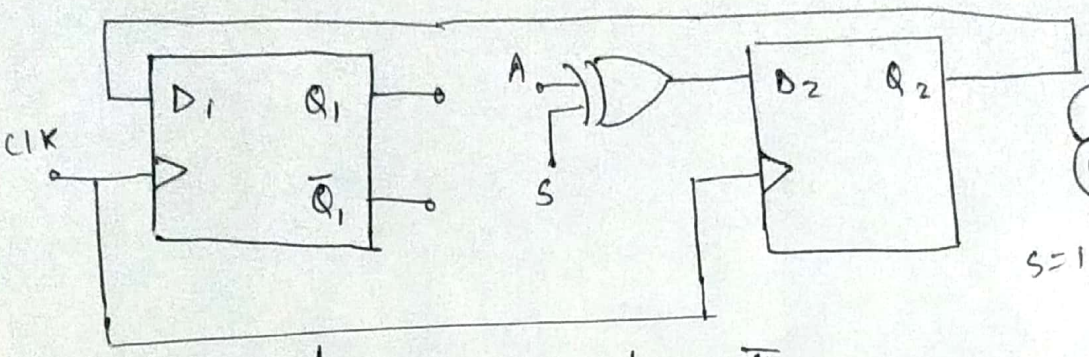
Average power dissipated –

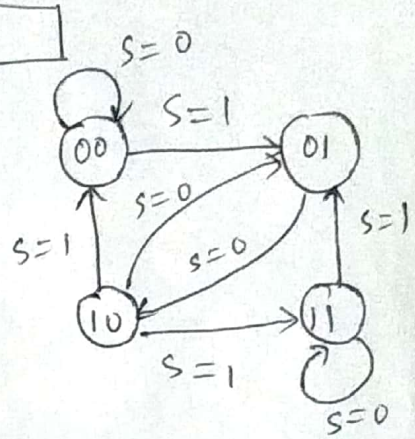
$$P_{avg} = \frac{1}{T}\int_0^T VI\,dt$$

$$= \frac{1}{5T}\int_0^{5T} \frac{V^2}{R}\,dt$$

$$= \frac{1}{5T} \times 3T \times \frac{1}{10k} \times 5^2 = 1.5\,mW$$

Q. In the given circuit, if A is connected to Q_1, the operation of the circuit is according to the state diagram. If XOR is replaced with XNOR, then to get the same operation of the circuit which of the following changes has to to be done -





(a) A should be connected to $\bar{Q}_1$.

(b) A should be connected to $\bar{Q}_2$.

(c) A should be connected to $\bar{Q}_1$ & S is replaced $\bar{S}$

(d) A should be connected to Q_2.

Initially, $A = Q_1$

$D_2 = A \oplus S = Q_1 \oplus S = \bar{Q}_1 S + \bar{S} Q_1$

Now - X-OR gate is replaced by X-NOR. let X is unknown

So, $D_2 = S \odot X$

$= \bar{S}\bar{X} + SX$

Since circuits required to be same before & after.

$\therefore D_2 = S \odot X = Q_1 \oplus S$

$\bar{S}\bar{X} + SX = \bar{Q}_1 S + \bar{S} Q_1$

By comparing above, unknown X must be equal to $\bar{Q}_1$.

i.e A must be connected to $\bar{Q}_1$.