ANN (YUAN CHIH) WU

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EDUCATION

University of Illinois at Urbana-Champaign

B.S. Electrical Engineering with Minor in Computer Science
Aug 2013 – May 2017 | GPA: 3.7

- IEEE Tech Events Director 2016
- SWE Professional Chair 2015
- SWE External Social Chair 2014

HONORS & AWARDS

- Timothy N. Trick Leadership Award 2017
- Lauren Kelley Scholarship 2016
- I4I Merit Scholarship 2015

SKILLS

Programming Languages & HDLs

C++ • C • Python • x86 • MATLAB • SystemVerilog • HTML

Software Tools

Cadence JasperGold • Altera Quartus II • Advanced Design System • JMP • Vim • SVN • Git

Lab Instruments

Network Analyzer • Optical Spectrum Analyzer • Digital Communications Analyzer • Modular DC Source • Multi-Channel Error Analyzer • Synthesized Clock Generator • Bit Pattern Generator

COURSES

Electrical & Computer Engineering

- Computer Architecture
- Computer Systems Lab
- Digital Systems Lab
- Active Microwave Circuits
- Wireless Communications Systems
- Electronic Circuits
- Fields & Waves II
- Probability & Statistics
- Digital Signal Processing
- Analog Signal Processing
- Photonic Devices

Computer Science

- Data Structures
- Artificial Intelligence
- Machine Learning

EXPERIENCE

Apple Inc. | SoC Pixel IP Design Intern

Jun 2017 – Dec 2017 | Sunnyvale, CA
Verilog, C-Modeling

- Realizing computer vision algorithms into silicon architecture

Intel Corporation | Platform Engineering Intern

Jun 2016 – Aug 2016 | Hillsboro, OR
Python, SystemVerilog, Cadence JasperGold

- Wrote and verified RTL for the state transitions and multi-processor arbitration in a cache-coherency protocol
- Developed a SystemVerilog macro that checks clock domain crossing
- Created a Python script in Unix that extracts archiving information of the project's design files into HTML, used internally within the business group

Intel Corporation | Signal Integrity Intern

Jun 2015 – Aug 2015 | Hillsboro, OR
C++, JMP, Sigrity PowerSI, Allegro PCB Editor, ODB++ format

- Created a C++ tool that performs file conversion from design to CAD format
- Created a design of experiment to simulate S-parameters of the filter, and extracted a mathematical expression to optimize for best performance

RESEARCH

PASSAT Group | Prof. Rakesh Kumar

Jan 2017 – Present | Champaign, IL
Python

- Developed in-depth understanding of the hardware requirements and suitable designs of off-chip accelerators for Convolutional Neural Networks
- Researching machine learning accelerators for Recurrent Neural Networks

High Speed Integrated Circuits Group | Prof. Milton Feng

May 2014 – Jun 2016 | Champaign, IL
Keysight/HP instruments, Origin

- Measured and analyzed μ-cavity lasing optoelectronic device (cavity size < 10 micron) for both free-space and fiber-coupled measurements
- Validated vertical cavity surface emitting lasers (VCSELs) with cutting-edge bit error ratio test system of data rates up to 56 Gb/s

PROJECTS

Tetris on FPGA | *SystemVerilog, Altera Quartus II FPGA*

Mar 2016 – May 2016

- Created a multi-level Tetris game with functionality implemented with a hierarchy of hardware modules and keyboard inputs handled by a C compiler

Unix-Like Operating System | *x86, C*

Oct 2016 – Dec 2016

- Developed a single-threaded kernel OS inspired by Linux
- Features included scheduling, paging, filesystem, and several drivers

Handwriting-Based Math Symbol Classifier | *Python, Tensorflow*

Nov 2016 – Dec 2016

- Used Recurrent Neural Networks and the Tensorflow library to build classifier
- Training and testing on CHORME 2012-2014 dataset yielded 87%+ accuracy