SOM-AM57XX
Hardware Design Spec

Revision: X02

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Revision History

X00	2017-06-26	Peng Wang	Initial Creation
X01	2017-07-04	Tony	Document translation and format modification
X02	2017-07-08	Tony	Update follow the review meeting

1. About This Document

This document describes the hardware design spec of the project **SOM-AM57XX.**
.Reference documents are listed below:

- AM572x Sitara Processors Silicon Revision 2.0 (Rev. B)
- AM572x AM571x-Compatibility Guide
- AM572x Technical Reference Manual
- AM572x Power Consumption Summary
- AM57XX ,Transformer SoM Family - AM57x MRD 201704
- SOM-AM57XX--PRD_REV00

2. Introduction

2.1. Target Components :

For the SOM board can work at -40°C ~+85°C,all the components used should meet the requirement.

CPU:	AM5728	New
PMIC:	TPS6590377ZWSR	New
DDR:	MT41K256M16TW-107 IT	Library
QSPI FLASH:	S25FL256SRS232	Library
EMMC:	EMMC08G-M325	New
Clock Generator:	CDCM9102RHBR	New
DC/DC	TPS51200	New
DC/DC	TPS22965	New
Logic	SN74LVC1G08	New
Crystal	5YAA22579182TF60Q3	New
Crystal	5YAA20000181TF70Q3	New
Crystal	5YAA16384102TF60Q3	New

2.2. List of Abbreviations:

XIP	- Execute in place
MCASP	- Multichannel audio serial port
SOM	- System On Module
GPMC	- General Purpose Memory Controller
MTBF	- Mean Time Between Failure
BTB	- Board To Board
IC	- Integrated Circuit
PD	- Pull Down
PU	- Pull Up
EMIF	- External Memory Interface

2.3. Principle of Hareware design

2.3.1. Hardware stability

- The logic level of a logic circuit must guarantee a level of magnitude (high or low), and the float pins of the chip must be setted to a low or high level.

- Power ripple: the power ripple of the core voltage should within the requirement .
- For the PCB design of high-speed signals,the special repedance,time delay and other requirements of PCB wiring should be guaranteed .
- The clocks devices should choose the devices with good stability and temperature characteristics.
- The circuit design needs to consider EMI suppression, EMI/EMC experiments need to do, and the relevant requirements need to meet.

2.3.2. Reliability requirements

- Structural reliability: PCB layout should be reasonable, the proper connectors should be selected, and ensure that is easy to production and maintenance .
- Reliability of the circuit: The material quality, capacitor quality, clock quality and so on should be considered to ensure that the system can work steadily for a long time.
- MTBF:20000 hours.

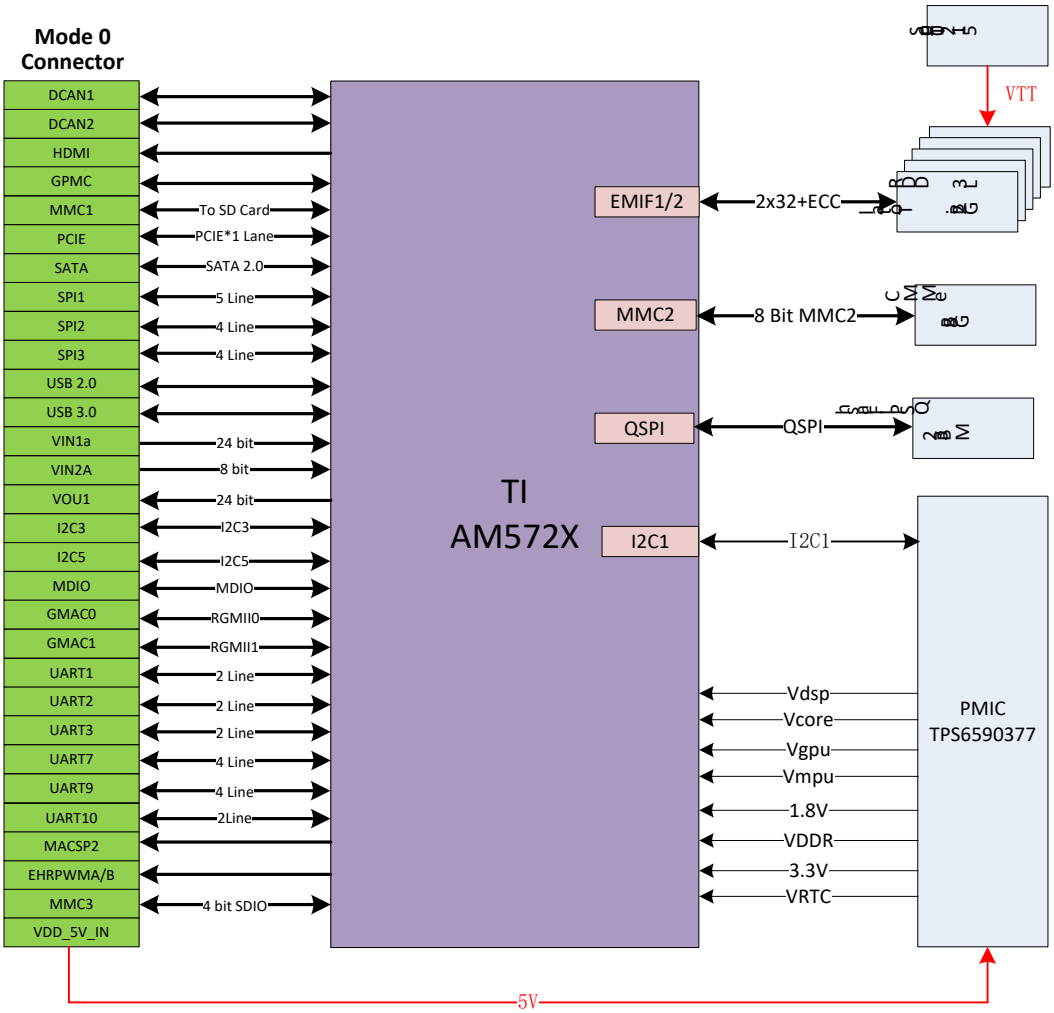
2.3.3. Hardware fault testability

- According to the function module distribution, each module should set the appropriate test points.

3. Platform Architecture

3.1. Block Diagram

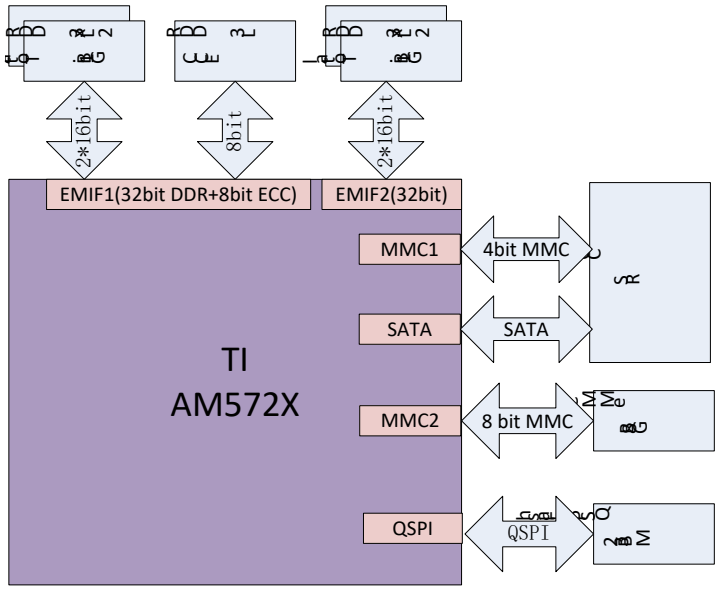
SOM-AM57xx-TM BLOCK Diagram



3.2. Hardware signal design

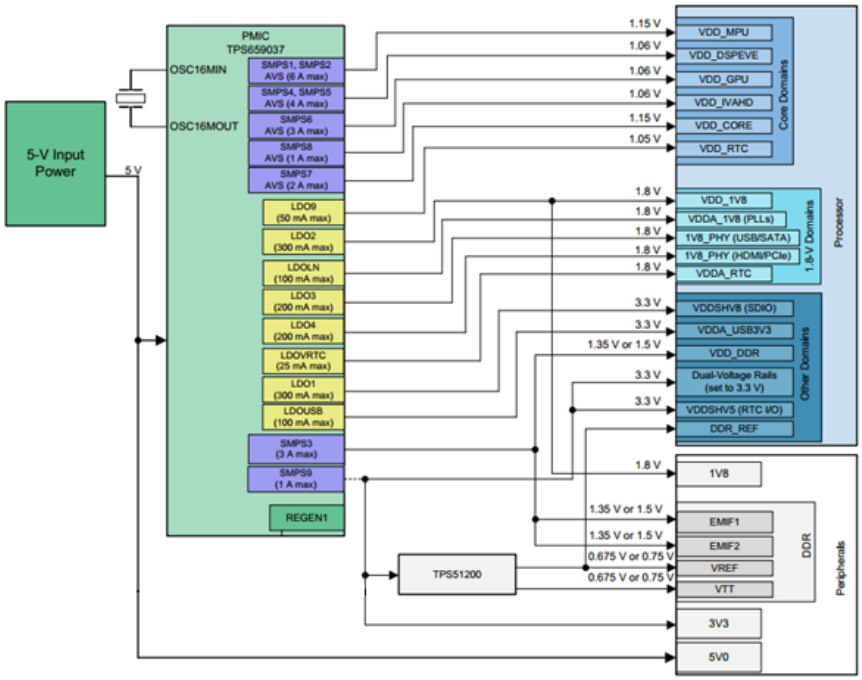
3.2.1. Storage Design

The SOM board takes RAM+ROM mode.
For the ROM, 8GB eMMC and 32MB QSPI flash are used.
SATA, MMC interfaces are connected to the connectors.
For the RAM, 4pcs 16x32MB DD3Ls are used because of the high price of 1GB DD3L.
A 16x32MB DDR3L used for ECC is connected to EMIF1.
The storage architecture as below:



3.2.2. Power Design

+5V/2A power supply is provided by the base board to supply the PMIC.
The PMIC provides all the power of AM5728.
The PMIC can control the power sequence of the AM5728 to meet the spec.
The AM5728 can communicate with PMIC with I2C1 interface and control the PMIC power output.
The PMIC can work when power on, and then the PMIC can be power off by the signal
The power architecture as below:



Power Consumption

Power Supply Group	Voltage [V]	Current [mA] [max]
VDD_CORE	1.00	747.7
VDD_MPU	1.20	3307.8
VDD_DSP	1.06	342.5
VDD_IVA	1.12	54.8

VDD_GPU	1.09	795.8
VDDS_DDR	1.35	366.9
Analog PHY	1.78	103.1
Analog DPLL	1.79	37.1
Analog USB PHY	3.30	3.5
1.8V IO	1.81	138.3
3.3V IO	3.27	80.3
VDD_DDR	1.34	528.5

The power on sequence as below:

Figure 5-1 and Figure 5-2 describe the device Power Sequencing when RTC-mode is NOT used.

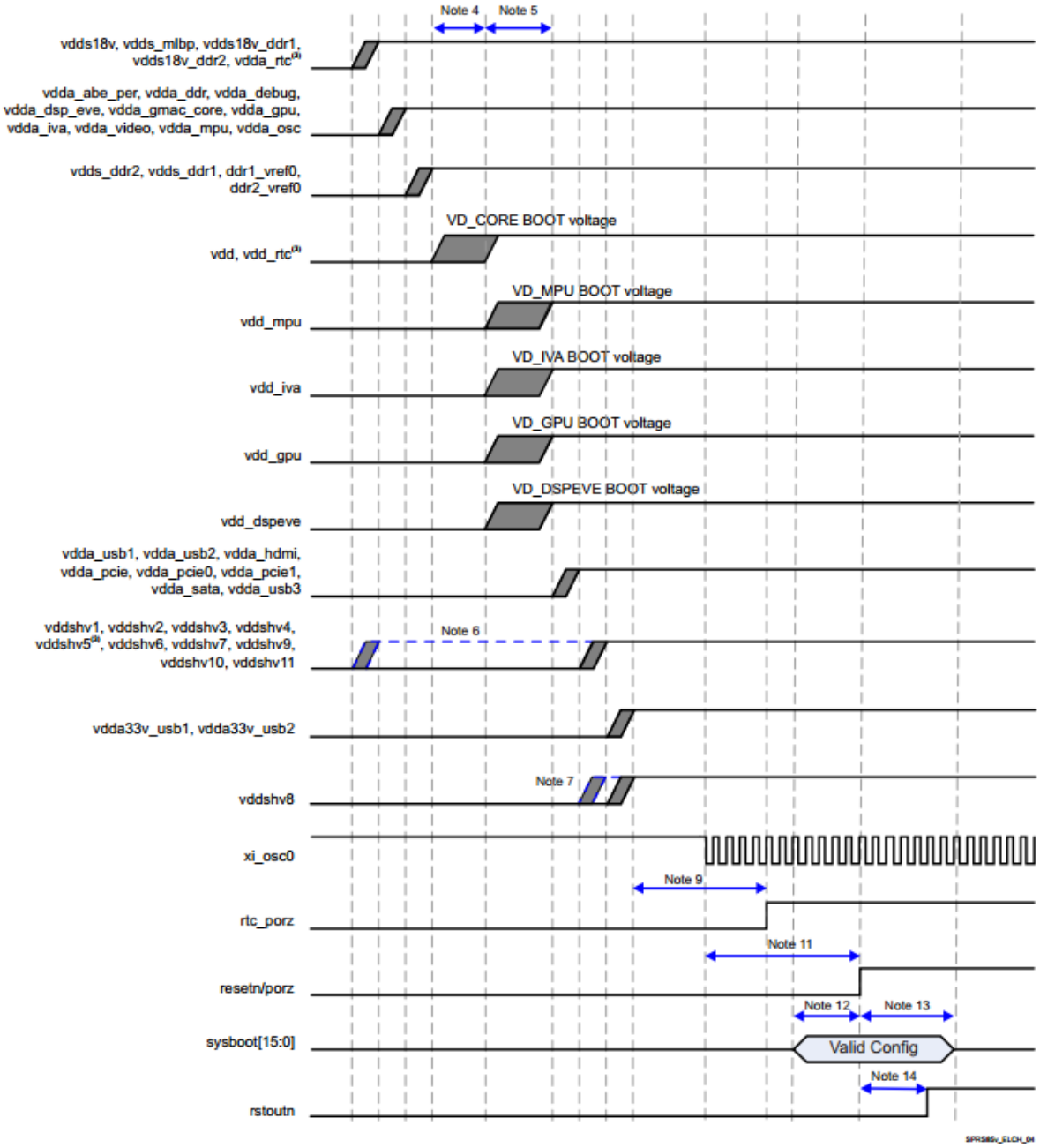


Figure 5-1. Power-Up Sequencing

3.2.3. Boot Design

There are 16 pins need to configured to select the work mode of the AM5728,sysboot[5:0] are used to select the boot device.

sysboot[5:4] sysboot[3:0]	First Device Second Device Third Device

Peripheral Preferred Booting

0b00 0b0000	USB **eMMC**
0b00 0b0001	USB **NAND**
0b00 0b0010	USB **SD eMMC**
0b00 0b0011	USB **SATA SD**
0b00 0b0100	USB UART **XIP**
0b00 0b0101	SD **XIP**
0b00 0b0110	SD **QSPI_1**
0b00 0b0111	SD **QSPI_4**
0b00 0b1010	SD **Fast XIP**

Recovery/Upgrade or Development Booting

0b01 0b0000	**USB**
0b01 0b0011	**UART**
0b01 0b0100	**SD** USB
0b01 0b0101	**SD** USB
0b01 0b0110	**SD** USB
0b01 0b0111	**SD** USB
0b01 0b1000	**SD** USB
0b01 0b1001	**SD** USB
0b01 0b1010	**SD** USB
0b01 0b1011	**SD** USB

Memory Preferred Booting

0b10 0b0000	**eMMC** USB
0b10 0b0001	**NAND** USB
0b10 0b0010	**SD eMMC** USB
0b10 0b0011	**SATA SD** USB
0b10 0b0100	**XIP** USB UART
0b10 0b0101	**XIP** SD USB
0b10 0b0110	**QSPI_1** SD USB
0b10 0b0111	**QSPI_4** SD USB

Production Booting(1)

0b11 0b0000	**SD**
0b11 0b0100	**SATA**
0b11 0b0101	**XIP**
0b11 0b0110	**QSPI_1**

0b11 0b0111	**QSPI_4**
0b11 0b1000	**eMMC**
0b11 0b1001	**NAND**
0b11 0b1010	**Fast XIP**
0b11 0b1011	**eMMC (boot part.)**(2)

Boot[15:6] need to be setted on the SOM board ,no need to reconfigurated on the base board.
Boot[5:0] need to pull high on the SOM board ,the base board can reconfigurate to set the work mode of AM5728.
Boot[15:0] default configuration is 1000000100111111 .

Boot Peripheral Pin Multiplexing

According to selected boot peripheral, the pin multiplexing configuration is coded by ROM code These settings are not restored to default values at ROM code exit.

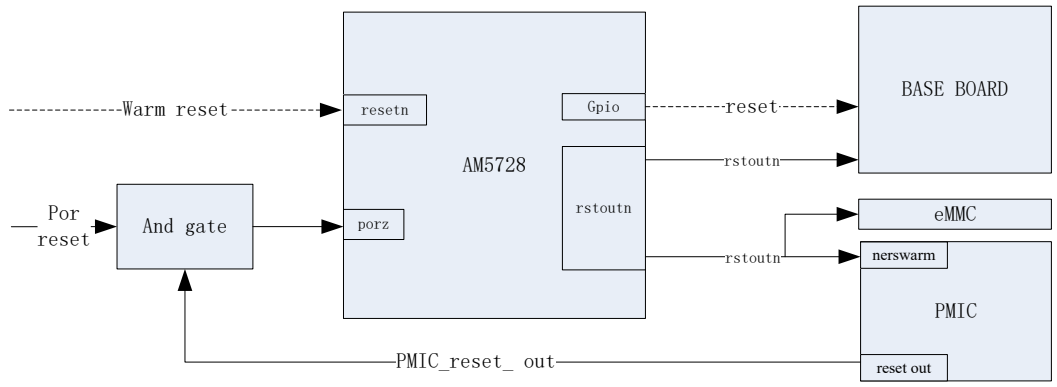
Table 33-10. Pin Multiplexing According to Boot Peripheral

Boot Device	Boot Interface	Pads	MuxMode	Signals
eMMC	MMC2	gpmc_a[19:27], gpmc_cs[1]	MuxMode=0x1	mmc2_dat[4:7], mmc2_clk, mmc2_dat[0:3], mmc2_cmd
SD	MMC1	mmc1_clk, mmc1_cmd, mmc1_dat[0:3]	MuxMode=0x0	mmc1_clk, mmc1_cmd, mmc1_dat[0:3]
NAND	GPMC	GPMC on CS0	MuxMode=0x0	GPMC on CS0
XIP	GPMC	GPMC on CS0	MuxMode=0x0	GPMC on CS0, wait signal monitoring according to the SYSBOOT[10] setting
SATA	SATA	sata1_txp0, sata1_txn0, sata1_rxp0, sata1_rxn0	-	sata1_txp0, sata1_txn0, sata1_rxp0, sata1_rxn0
QSPI_1/QSPI_4	QSPI1	gpmc_a[13:18], gpmc_cs[2]	MuxMode=0x1	qspi1_rtclk, qspi1_d[3:0], qspi1_sclk, qspi1_cs[0]
USB	USB1	usb1_dp and usb1_dm	-	usb1_dp and usb1_dm
UART	UART3	uart2_rtsn uart2_ctsn	MuxMode=0x1 MuxMode=0x2	uart3_txd uart3_rxd

3.2.4. Reset design

The SOM board can be reset by the base board with a reset input signal.
The SOM board can reset the base board with a reset output signal.
The peripheral devices can reset with cpu at the same time or controlled by cpu gpio.

There is a device erratum in all of the AM572x devices that prevents use of RESETn independent from PORz. The workaround is to generate PORz whenever a device reset occurs even if it is from an internal initiator. This is accomplished through cooperation with the PMIC paired with the AM572x device. The RSTOUTn output from the AM572x device is connected to the NRESWARM input of the PMIC. This initiates a re-start that drives RESET_OUT low and resets all voltages to their initial values. Since RESET_OUT from the PMIC is connected to PORz in the AM572x device, a hard reset is forced on the SOC that meets the needs of the erratum workaround.
Please reference the document “AM572x Errata” to get more information.
The reset architecture is as below:



The power sequence of reset as below:

Figure 13 shows the warm reset sequence of TPS6590377ZWSR in the case that all resources are turned off. If any resource is on when NRESWARM is asserted, the resource remains on.

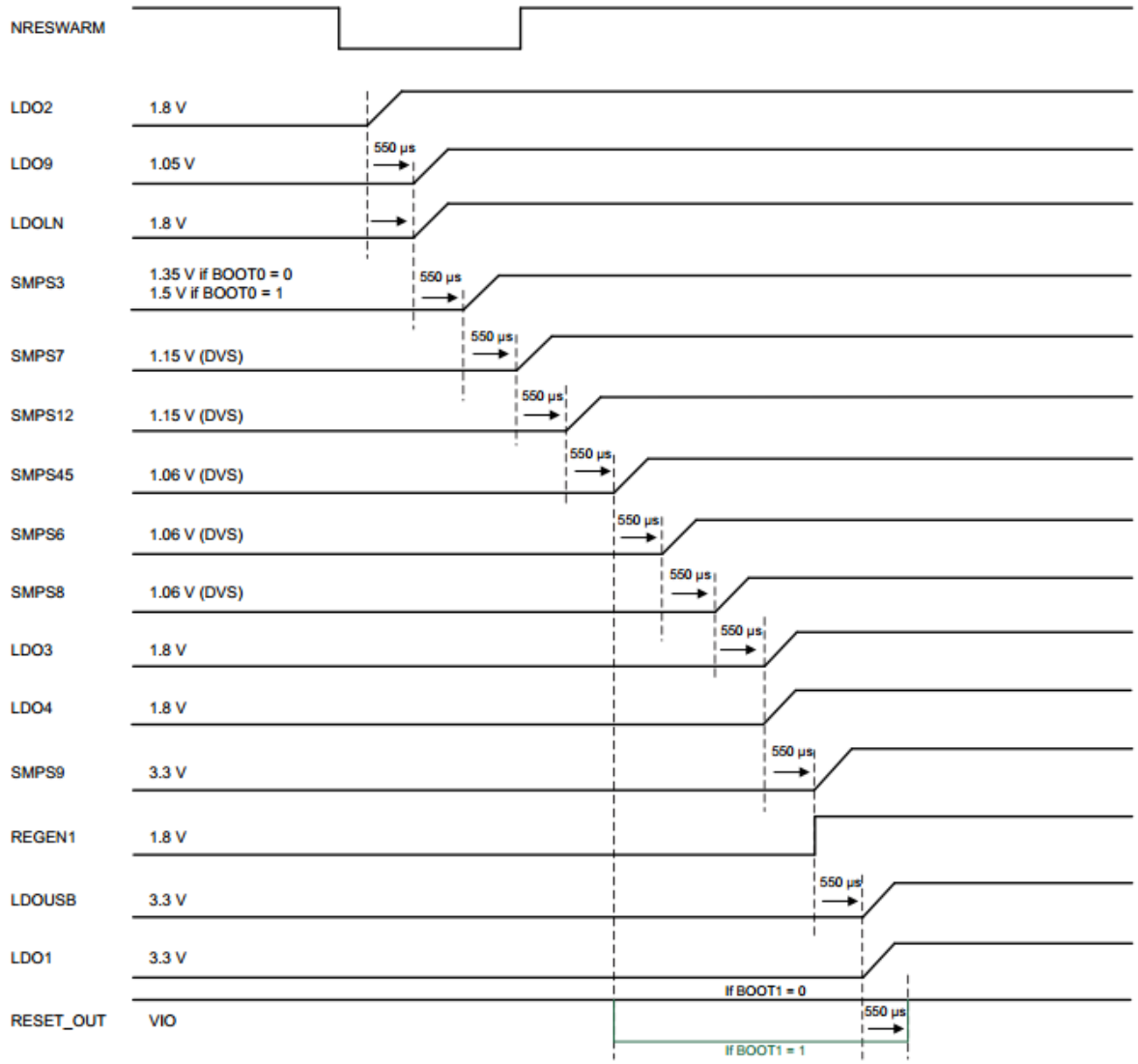


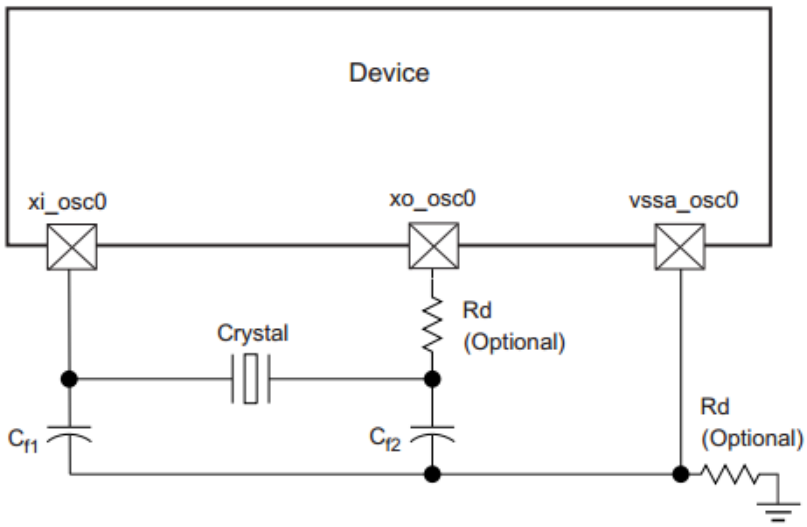
Figure 13. Warm Reset Sequence of TPS6590377ZWSR

3.2.5. Clock Design

AM5728 operation requires the follow clock:

The 32KHZ ferquency for low frequency operation can be supplied by on chip divider +mux(FUNC_32K_CLK),external input clock(32KHZ) is not used.

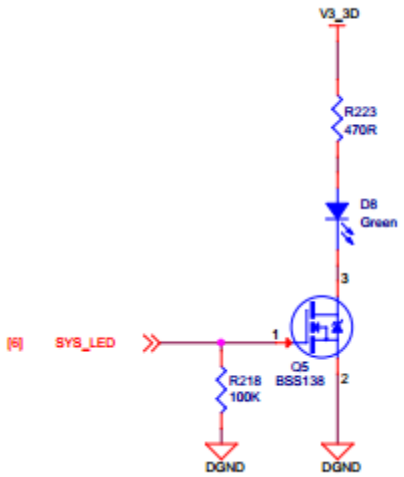
A crystal clock is connected to OSC0 as the source of the internal system clock(SYS_CLK1). The frequency is 20M as TI recommend.



A crystal clock is connected to OSC1 as the source of the internal system clock(SYS_CLK2) The frequency is 22.5792M as TI recommend.

3.2.6. LED Design

A LED is controlled by the powergood signal of PMIC to indicate the power status of the AM5728.
A LED is controled by a gpio (low level default),the function is defined by SW.
The reference circuit as below :



3.2.7. RTC Design

RTC mode is not supported in the family of devices,a external RTC need to add on the base board.

3.2.8. JTAG Design

To minimize the size of the SOM board,test points are used for the JATG.
We need to connect test points to a cable if the JTAG interface is used during the development.

3.2.9. UART/CAN/I2C Design

All the I2C interfaces have been pulled up on the SOM board,UART and CAN interfaces need to pull up on the base board.

3.2.10. Interface Design

All the interfaces need to connect to the connectors directly,ESD conponents are not needed,
Pull up /pull down resistances are not needed expect for the special use.
All the output clocks need to add the RC circuits to avoid the signal reflect and EMI.

4. Impedance Control

The impedance requirement as below.

Interface	Single Ended Impedance	Differential Impedance	Margin
DDR	50	100	+-10%
USB	45	90	+-10%
SATA	50	100	+-10%
MMC	50		+-10%
PCIe	50	100	+-10%
RGMII	50		+-10%
LCD	50		+-10%
GPMC	50		+-10%

5. Interface Assignment

5.1. eMMC

eMMC	mmc2_clk	J7	3.3V	OUT	MMC2 clock
	mmc2_cmd	H6	3.3V	OUT	MMC2 command
	mmc2_dat0	J4	3.3V	IO	MMC2 data bit 0
	mmc2_dat1	J6	3.3V	IO	MMC2 data bit 1
	mmc2_dat2	H4	3.3V	IO	MMC2 data bit 2
	mmc2_dat3	H5	3.3V	IO	MMC2 data bit 3
	mmc2_dat4	K7	3.3V	IO	MMC2 data bit 4
	mmc2_dat5	M7	3.3V	IO	MMC2 data bit 5
	mmc2_dat6	J5	3.3V	IO	MMC2 data bit 6
	mmc2_dat7	K6	3.3V	IO	MMC2 data bit 7

5.2. QSPI flash

QSPI	gpmc_a13/ qspi_rtclk	R3	3.3V	IN	GPMC address 13 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Return Clock Input
	gpmc_a14/ qspi_d3	T2	3.3V	IN	GPMC address 14 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Data[3]
	gpmc_a15/ qspi_d2	U2	3.3V	IN	GPMC address 15 in A/D

					nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Data[2]
	gpmc_a16/ qspi_d0	U1	3.3V	IN	GPMC address 16 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Data[0]
	gpmc_a17/ qspi_d1	P3	3.3V	IN	GPMC address 17 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Data[1]
	gpmc_a18/ qspi_sclk	R2	3.3V	OUT	GPMC address 18 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Serial Clock Output
	qspi_cs0	P2	3.3V	OUT	QSPI1 Chip Select [0]. This pin is Used for QSPI1 boot modes.

5.3. JTAG

JTAG	emu0	G21	3.3V	IO	Emulator pin 0
	emu1	D24	3.3V	IO	Emulator pin 1
	rtck	E18	3.3V	OUT	JTAG return clock output
	tclk	E20	3.3V	IN	JTAG test clock input
	tdi	D23	3.3V	IN	JTAG test data input
	tdo	F19	3.3V	OUT	JTAG test port data output
	tms	F18	3.3V	IO	JTAG test port mode select input.
	trstn	D20	3.3V	IN	JTAG test reset

5.4. BOOT

BOOT	gpmc_ad0/sysboot0	M6	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad1/sysboot1	M2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad2/sysboot2	L5	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad3/sysboot3	M1	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad4/sysboot4	L6	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad5/sysboot5	L4	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad6/sysboot6	L3	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad7/sysboot7	L2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad8/sysboot8	L1	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad9/sysboot9	K2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad10/sysboot10	J1	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad11/sysboot11	J2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad12/sysboot12	H1	3.3V	IO	General Purpose Memory Controller

					interface Address/Data
	gpmc_ad13/sysboot13	J3	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad14/sysboot14	H2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad15/sysboot15	H3	3.3V	IO	General Purpose Memory Controller interface Address/Data

5.5. GPMC Interface

GPMC	gpmc_a0	R6	3.3V	OUT	GPMC Address 0. Only used to effectively address 8-bit data nonmultiplexed memories
	gpmc_a1	T9	3.3V	OUT	GPMC address 1 in A/D nonmultiplexed mode and Address 17 in A/D multiplexed mode
	gpmc_a2	T6	3.3V	OUT	GPMC address 2 in A/D nonmultiplexed mode and Address 18 in A/D multiplexed mode
	gpmc_a3	T7	3.3V	OUT	GPMC address 3 in A/D nonmultiplexed mode and Address 19 in A/D multiplexed mode
	gpmc_a4	P6	3.3V	OUT	GPMC address 4 in A/D nonmultiplexed mode and Address 20 in A/D multiplexed mode
	gpmc_a5	R9	3.3V	OUT	GPMC address 5 in A/D nonmultiplexed mode and Address 21 in A/D multiplexed mode
	gpmc_a6	R5	3.3V	OUT	GPMC address 6 in A/D nonmultiplexed mode and Address 22 in A/D multiplexed mode
	gpmc_a7	P5	3.3V	OUT	GPMC address 7 in A/D nonmultiplexed mode and Address 23 in A/D multiplexed mode
	gpmc_a8	N7	3.3V	OUT	GPMC address 8 in A/D nonmultiplexed mode and Address 24 in A/D multiplexed mode
	gpmc_a9	R4	3.3V	OUT	GPMC address 9 in A/D nonmultiplexed mode and Address 25 in A/D multiplexed mode
	gpmc_a10	N9	3.3V	OUT	GPMC address 10 in A/D nonmultiplexed mode and Address 26 in A/D multiplexed mode
	gpmc_a11	P9	3.3V	OUT	GPMC address 11 in A/D nonmultiplexed mode and unused in A/D multiplexed mode
	gpmc_a12	P4	3.3V	OUT	GPMC address 12 in A/D

					nonmultiplexed mode and unused in A/D multiplexed mode
	gpmc_a13/ qspi_rtclk	R3	3.3V	IN	GPMC address 13 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Return Clock Input
	gpmc_a14/ qspi_d3	T2	3.3V	IN	GPMC address 14 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Data[3]
	gpmc_a15/ qspi_d2	U2	3.3V	IN	GPMC address 15 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Data[2]
	gpmc_a16/ qspi_d0	U1	3.3V	IN	GPMC address 16 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Data[0]
	gpmc_a17/ qspi_d1	P3	3.3V	IN	GPMC address 17 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Data[1]
	gpmc_a18/ qspi_sclk	R2	3.3V	OUT	GPMC address 18 in A/D nonmultiplexed mode and unused in A/D multiplexed mode/ QSPI1 Serial Clock Output
	gpmc_ad0/sysboot0	M6	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad1/sysboot1	M2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad2/sysboot2	L5	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad3/sysboot3	M1	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad4/sysboot4	L6	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad5/sysboot5	L4	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad6/sysboot6	L3	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad7/sysboot7	L2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad8/sysboot8	L1	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad9/sysboot9	K2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad10/sysboot10	J1	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad11/sysboot11	J2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad12/sysboot12	H1	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad13/sysboot13	J3	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad14/sysboot14	H2	3.3V	IO	General Purpose Memory Controller interface Address/Data
	gpmc_ad15/sysboot15	H3	3.3V	IO	General Purpose Memory Controller interface Address/Data

	gpmc_clk	P7	3.3V	IO	GPMC Clock output
	gpmc_advn_ale	N1	3.3V	OUT	GPMC address valid active low or address latch enable
	gpmc_oen_ren	M5	3.3V	OUT	GPMC output enable active low or read enable
	gpmc_wen	M3	3.3V	OUT	GPMC write enable active low
	gpmc_ben0	N6	3.3V	OUT	GPMC lower-byte enable active low
	gpmc_ben1	M4	3.3V	OUT	GPMC upper-byte enable active low
	gpmc_wait0	N2	3.3V	IN	GPMC external indication of wait 0
	gpmc_cs0	T1	3.3V	OUT	GPMC Chip Select 0 (active low)
	gpmc_cs3	P1	3.3V	OUT	GPMC Chip Select 3 (active low)

5.6. PCIE Interface

PCIe	pcie_rxp0	AH13		IN	PCIe1_PHY_RX Receive Data Lane 0 (positive)
	pcie_rxn0	AG13		IN	PCIe1_PHY_RX Receive Data Lane 0 (negative)
	pcie_txp0	AH14		OUT	PCIe1_PHY_TX Transmit Data Lane 0 (positive)
	pcie_txn0	AG14		OUT	PCIe1_PHY_TX Transmit Data Lane 0 (negative)
	pcie _rxp1	AH11		IN	PCIe1_PHY_RX Receive Data Lane 1 (positive)
	pcie _rxn1	AG11		IN	PCIe1_PHY_RX Receive Data Lane1 (negative)
	pcie_txp1	AH12		OUT	PCIe1_PHY_TX Transmit Data Lane 1 (positive)
	pcie_txn1	AG12		OUT	PCIe1_PHY_TX Transmit Data Lane 1 (negative)

5.7. SATA Interface

SATA	sata1_rxn0	AH9		IN	SATA differential negative receiver lane 0
	sata1_rxp0	AG9		IN	SATA differential positive receiver lane 0
	sata1_txp0	AH10		OUT	SATA differential positive transmitter lane 0
	sata1_txn0	AG10		OUT	SATA differential negative transmitter lane 0

5.8. USB Interface

USB3.0	usb1_drvvbus	AB10	3.3V	OUT	USB1 Drive VBUS signal
	usb1_dp	AD12		IO	USB1 USB2.0 differential signal pair (positive)
	usb1_dm	AC12		IO	USB1 USB2.0 differential signal pair (negative)
	usb_rxp0	AE12		IN	USB1 USB3.0 receiver positive lane
	usb_rxn0	AF12		IN	USB1 USB3.0 receiver negative lane
	usb_txp0	AD11		OUT	USB1 USB3.0 transmitter positive lane
	usb_txn0	AC11		OUT	USB1 USB3.0 transmitter negative lane
USB2	usb2_drvvbus	AC10	3.3V	OUT	USB2 Drive VBUS signal

	usb2_dp	AE11		IO	USB2 USB2.0 differential signal pair (positive)
	usb2_dm	AF11		IO	USB2 USB2.0 differential signal pair (negative)

5.9. VIDEO input Interface

VIN1	vin1a_d0	AE8	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d1	AD8	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d2	AG7	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d3	AH6	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d4	AH3	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d5	AH5	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d6	AG6	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d7	AH4	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d8	AG4	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d9	AG2	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d10	AG3	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d11	AG5	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d12	AF2	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d13	AF6	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d14	AF3	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d15	AF4	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d16	AF1	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d17	AE3	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d18	AE5	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d19	AE1	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d20	AE2	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d21	AE6	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d22	AD2	3.3V	IN	Video Input 1 Port A Data input
	vin1a_d23	AD3	3.3V	IN	Video Input 1 Port A Data input
	vin1a_clk0	AG8	3.3V	IN	Video Input 1 Port A Clock input. Input clock for 8-bit 16-bit or 24-bit Port A video capture. Input data is sampled on the CLK0 edge.
	vin1a_de0	AD9	3.3V	IN	Video Input 1 Data Enable input
	vin1a_fld0	AF9	3.3V	IN	Video Input 1 Port A Field ID input
	vin1a_hsync0	AE9	3.3V	IN	Video Input 1 Port A Horizontal Sync input
	vin1a_vsync0	AF8	3.3V	IN	Video Input 1 Port A Vertical Sync input
VIN2	vin2a_clk0	E1	3.3V	IN	Video Input 2 Port A Clock input.
	vin2a_de0	G2	3.3V	IN	Video Input 2 Port A Data Enable input
	vin2a_fld0	H7	3.3V	IN	Video Input 2 Port A Field ID input
	vin2a_hsync0	G1	3.3V	IN	Video Input 2 Port A Horizontal Sync input
	vin2a_vsync0	G6	3.3V	IN	Video Input 2 Port A Vertical Sync input
	vin2a_d0	F2	3.3V	IN	Video Input 2 Port A Data input
	vin2a_d1	F3	3.3V	IN	Video Input 2 Port A Data input
	vin2a_d2	D1	3.3V	IN	Video Input 2 Port A Data input
	vin2a_d3	E2	3.3V	IN	Video Input 2 Port A Data input
	vin2a_d4	D2	3.3V	IN	Video Input 2 Port A Data input
	vin2a_d5	F4	3.3V	IN	Video Input 2 Port A Data input
	vin2a_d6	C1	3.3V	IN	Video Input 2 Port A Data input

	vin2a_d7	E4	3.3V	IN	Video Input 2 Port A Data input

5.10. VIDEO output Interface

LCD	vout1_d0	F11	3.3V	OUT	Video Output 1 Data output
	vout1_d1	G10	3.3V	OUT	Video Output 1 Data output
	vout1_d2	F10	3.3V	OUT	Video Output 1 Data output
	vout1_d3	G11	3.3V	OUT	Video Output 1 Data output
	vout1_d4	E9	3.3V	OUT	Video Output 1 Data output
	vout1_d5	F9	3.3V	OUT	Video Output 1 Data output
	vout1_d6	F8	3.3V	OUT	Video Output 1 Data output
	vout1_d7	E7	3.3V	OUT	Video Output 1 Data output
	vout1_d8	E8	3.3V	OUT	Video Output 1 Data output
	vout1_d9	D9	3.3V	OUT	Video Output 1 Data output
	vout1_d10	D7	3.3V	OUT	Video Output 1 Data output
	vout1_d11	D8	3.3V	OUT	Video Output 1 Data output
	vout1_d12	A5	3.3V	OUT	Video Output 1 Data output
	vout1_d13	C6	3.3V	OUT	Video Output 1 Data output
	vout1_d14	C8	3.3V	OUT	Video Output 1 Data output
	vout1_d15	C7	3.3V	OUT	Video Output 1 Data output
	vout1_d16	B7	3.3V	OUT	Video Output 1 Data output
	vout1_d17	B8	3.3V	OUT	Video Output 1 Data output
	vout1_d18	A7	3.3V	OUT	Video Output 1 Data output
	vout1_d19	A8	3.3V	OUT	Video Output 1 Data output
	vout1_d20	C9	3.3V	OUT	Video Output 1 Data output
	vout1_d21	A9	3.3V	OUT	Video Output 1 Data output
	vout1_d22	B9	3.3V	OUT	Video Output 1 Data output
	vout1_d23	A10	3.3V	OUT	Video Output 1 Data output
	vout1_clk	D11	3.3V	OUT	Video Output 1 Clock output
	vout1_de	B10	3.3V	OUT	Video Output 1 Data Enable output
	vout1_fld	B11	3.3V	OUT	Video Output 1 Field ID output. This signal is not used for embedded sync modes.
	vout1_hsync	C11	3.3V	OUT	Video Output 1 Horizontal Sync output. This signal is not used for embedded sync modes.
	vout1_vsync	E11	3.3V	OUT	Video Output 1 Vertical Sync output. This signal is not used for embedded sync modes.

HDMI	hdmi1_clocky	AH16		OUT	HDMI clock differential positive or negative
	hdmi1_clockx	AG16		OUT	HDMI clock differential positive or negative
	hdmi1_data2y	AH19		OUT	HDMI data 2 differential positive or negative
	hdmi1_data2x	AG19		OUT	HDMI data 2 differential positive or negative
	hdmi1_data1y	AH18		OUT	HDMI data 1 differential positive or negative
	hdmi1_data1x	AG18		OUT	HDMI data 1 differential positive or negative
	hdmi1_data0y	AH17		OUT	HDMI data0 differential positive or negative

	hdmi1_data0x	AG17		OUT	HDMI data 0 differential positive or negative
	hdmi1_ddc_scl	C25	3.3V	OUT	HDMI display data channel clock
	hdmi1_ddc_sda	F17	3.3V	IO	HDMI display data channel data
	hdmi1_ddc_cec	B20	3.3V	IO	HDMI consumer electronic control
	hdmi1_ddc_hpd	B21	3.3V	IN	HDMI display hot plug detect

5.11. RGMII Interface

RGMII1	rgmii1_txc	D5	3.3V	OUT	RGMII1 Transmit Clock
	rgmii1_txctl	C2	3.3V	OUT	RGMII1 Transmit Enable
	rgmii1_txd3	C3	3.3V	OUT	RGMII1 Transmit Data
	rgmii1_txd2	C4	3.3V	OUT	RGMII1 Transmit Data
	rgmii1_txd1	B2	3.3V	OUT	RGMII1 Transmit Data
	rgmii1_txd0	D6	3.3V	OUT	RGMII1 Transmit Data
	rgmii1_rxc	C5	3.3V	IN	RGMII1 Receive Clock
	rgmii1_rxctl	A3	3.3V	IN	RGMII1 Receive Control
	rgmii1_rxd3	B3	3.3V	IN	RGMII1Receive Data
	rgmii1_rxd2	B4	3.3V	IN	RGMII1Receive Data
	rgmii1_rxd1	B5	3.3V	IN	RGMII1Receive Data
	rgmii1_rxd0	A4	3.3V	IN	RGMII1Receive Data
RGMII0	rgmii0_txc	W9	3.3V	OUT	RGMII0 Transmit Clock
	rgmii0_txctl	V9	3.3V	OUT	RGMII0 Transmit Enable
	rgmii0_txd3	V7	3.3V	OUT	RGMII0 Transmit Data
	rgmii0_txd2	U7	3.3V	OUT	RGMII0 Transmit Data
	rgmii0_txd1	V6	3.3V	OUT	RGMII0 Transmit Data
	rgmii0_txd0	U6	3.3V	OUT	RGMII0 Transmit Data
	rgmii0_rxc	U5	3.3V	IN	RGMII0 Receive Clock
	rgmii0_rxctl	V5	3.3V	IN	RGMII0 Receive Control
	rgmii0_rxd3	V4	3.3V	IN	RGMII0 Receive Data
	rgmii0_rxd2	V3	3.3V	IN	RGMII0 Receive Data
	rgmii0_rxd1	Y2	3.3V	IN	RGMII0 Receive Data
	rgmii0_rxd0	W2	3.3V	IN	RGMII0 Receive Data
	mdio_d	U4	3.3V	IO	MDIO Data
	mdio_clk	V1	3.3V	OUT	MDIO Clock

5.12. MCASP Interface

MCASP2	mcasp2_aclkx	A19	3.3V	OUT	MCASP2 Transmit Bit Clock I/O
	mcasp2_fsx	A18	3.3V	OUT	MCASP2 Transmit Frame Sync I/O
	mcasp2_ahclkx/xref_clk1	E17	3.3V	OUT	MCASP2 Transmit High-Frequency Master Clock I/O
	mcasp2_axr0	B15	3.3V	IO	MCASP2 Transmit/Receive Data I/O
	mcasp2_axr1	A15	3.3V	IO	MCASP2 Transmit/Receive Data I/O
MCASP1	mcasp1_fsx/ gpio7_10	D14	3.3V	OUT	MCASP1 Transmit Frame Sync
	mcasp1_aclkx/ gpio7_31	C14	3.3V	OUT	MCASP1 Transmit Bit Clock
	mcasp1_axr0 /gpio5_2	G12	3.3V	IO	MCASP1 Transmit/Receive Data I/O
	mcasp1_axr1/ gpio5_3	F12	3.3V	IO	MCASP1 Transmit/Receive Data I/O
	mcasp1_ahclkx /gpio6_17	D18	3.3V	OUT	MCASP1 Transmit High-Frequency Master Clock

5.13. MMC Interface

MMC	mmc3_clk	AD4	3.3V	OUT	MMC3 clock

	mmc3_cmd	AC4	3.3V	OUT	MMC3 command
	mmc3_dat0	AC7	3.3V	IO	MMC3 data bit 0
	mmc3_dat1	AC6	3.3V	IO	MMC3 data bit 1
	mmc3_dat2	AC9	3.3V	IO	MMC3 data bit 2
	mmc3_dat3	AC3	3.3V	IO	MMC3 data bit 3
	mmc1_clk	W6	3.3V	OUT	MMC1 clock
	mmc1_cmd	Y6	3.3V	OUT	MMC1 command
	mmc1_dat0	AA6	3.3V	IO	MMC1 data bit 0
	mmc1_dat1	Y4	3.3V	IO	MMC1 data bit 1
	mmc1_dat2	AA5	3.3V	IO	MMC1 data bit 2
	mmc1_dat3	Y3	3.3V	IO	MMC1 data bit 3
	mmc1_sdcd	W7	3.3V	IN	MMC1 Card Detect
	mmc1_sdwp	Y9	3.3V	IN	MMC1 Write Protect

5.14. Can Interface

CAN	dcan1_tx	G20	3.3V	OUT	DCAN1 transmit data pin
	dcan1_rx	G19	3.3V	IN	DCAN1 receive data pin
	dcan2_tx	E21	3.3V	OUT	DCAN2 transmit data pin
	dcan2_rx	F20	3.3V	IN	DCAN2 receive data pin

5.15. UART Interface

UART	uart1_rxd	B27	3.3V	IN	UART1 Receive Data Input
	uart1_txd	C26	3.3V	OUT	UART1 Transmit Data Output.
	uart2_rxd	D28	3.3V	IN	UART2 Receive Data Input.
	uart2_txd	D26	3.3V	OUT	UART2 Transmit Data Output.
	uart3_rxd	D27	3.3V	IN	UART3 Receive Data Input.
	uart3_txd	C28	3.3V	OUT	UART3 Transmit Data Output.
	uart7_rxd	B18	3.3V	IN	UART7 Receive Data Input.
	uart7_txd	F15	3.3V	OUT	UART7 Transmit Data Output.
	uart7_rtsn	C17	3.3V	OUT	UART7 request to send active low
	uart7_ctsn	B19	3.3V	IN	UART7 clear to send active low
	uart9_rxd /uart1_ctsn	E25	3.3V	IN	UART9 Receive Data Input.
	uart9_txd /uart1_rtsn	C27	3.3V	OUT	UART9 Transmit Data Output.
	uart9_ctsn	AB3	3.3V	IN	UART9 clear to send active low
	uart9_rtsn	AA4	3.3V	OUT	UART9 request to send active low
	uart10_txd	AD6	3.3V	OUT	UART10 Transmit Data Output.
	uart10_rxd	AC8	3.3V	IN	UART10 Receive Data Input.

5.16. SPI Interface

SPI	spi1_sclk	A25	3.3V	IO	SPI1 Clock I/O
	spi1_d1	F16	3.3V	IO	SPI1 Data I/O. Can be configured as either MISO or MOSI.
	spi1_d0	B25	3.3V	IO	SPI1 Data I/O. Can be configured as either MISO or MOSI.
	spi1_cs0 /gpio7_10	A24	3.3V	IO	SPI1 Chip Select I/O
	spi1_cs1/ gpio7_11	A22	3.3V	IO	SPI1 Chip Select I/O
	spi3_sclk	C18	3.3V	IO	SPI3 Clock I/O
	spi3_d1	A21	3.3V	IO	SPI3 Data I/O. Can be configured as

					either MISO or MOSI.
	spi3_d0	G16	3.3V	IO	SPI3 Data I/O. Can be configured as either MISO or MOSI.
	spi3_cs0	D17	3.3V	IO	SPI3 Chip Select I/O

5.17. I2C Interface

I2C	i2c1_sda	C21	3.3V	IO	I2C1 Data I/O
	i2c1_scl	C20	3.3V	OUT	I2C1 Clock
	i2c3_sda	AC5	3.3V	IO	I2C3 Data I/O
	i2c3_scl	AB4	3.3V	OUT	I2C3 Clock
	i2c4_sda	B14	3.3V	IO	I2C4 Data I/O
	i2c4_scl	J14	3.3V	OUT	I2C4 Clock
	i2c5_sda	AA3	3.3V	IO	I2C5 Data I/O
	i2c5_scl	AB9	3.3V	OUT	I2C5 Clock

5.18. PWM

PWM	timer3/GPIO	F21	3.3V	IO	PWM output/event trigger input
	eCAP3_in_PWM3_out/gpio1_25	AB5	3.3V	IO	ECAP3 Capture Iniput / PWM Output
	ehrpwm2A	E6	3.3V	OUT	EHRPWM2 Output A
	ehrpwm2B	D3	3.3V	OUT	EHRPWM2 Output B

5.19. GPIOs

GPIO	gpio4_9	F5	3.3V	IO	gpio
	gpio4_12	F6	3.3V	IO	gpio
	gpio1_24	AB8	3.3V	IO	gpio
	gpio5_19	Y1	3.3V	IO	gpio
	gpio5_18	V2	3.3V	IO	gpio
	gpio7_14/ spi2_sclk	A26	3.3V	IO	gpio
	gpio7_15/ spi2_d1	B22	3.3V	IO	gpio
	gpio7_16/ spi2_d0	G17	3.3V	IO	gpio
	gpio7_17/ spi2_cs0	B24	3.3V	IO	gpio
	gpio2_29/mcasp2_axr6	B17	3.3V	IO	gpio
	gpio6_19/mcasp2_axr10	B26	3.3V	IO	gpio
	gpio5_10/mcasp1_axr8/timer5	B12	3.3V	IO	gpio
	gpio6_5/mcasp1_axr14/timer11	G14	3.3V	IO	gpio
	gpio4_18/mcasp1_axr12/timer11	E14	3.3V	IO	gpio
	gpio6_4/mcasp1_axr13/timer10	A13	3.3V	IO	gpio

5.1. MISC

DSP	nmin_dsp	D21	3.3V	IN	Non maskable interrupt input, active-low.
PRCM	clkout3	C23	3.3V	OUT	Device Clock output 3. Can be used externally for devices with noncritical timing requirements, or for debug
	resetn	E23	3.3V	IN	Device Reset Input
	rstoutn	F23	3.3V	OUT	Reset out (Active low). This pin asserts low in response to any global reset condition on the device.
	porz	F22	3.3V	IN	Power on Reset (active low). This pin must be asserted low until all device supplies are valid (see reset sequence/requirements)
RTCSS	rtc_iso	AF14	3.3V	IN	RTC Domain Isolation Signal
	on_off	Y11	3.3V	OUT	RTC Power Enable output pin
	rtc_porz	AB17	3.3V	IN	RTC Power Domain Power-On Reset Input
	wakeup0	AD17	3.3V	IN	RTC External Wakeup Input 0
	Wakeup1	AC17	3.3V	IN	RTC External Wakeup Input 1
	Wakeup2	AB16	3.3V	IN	RTC External Wakeup Input 2
	Wakeup3	AC16	3.3V	IN	RTC External Wakeup Input 3

6. Resource Allocation

The resource requirements of PRD have been meeted.

6.1.1. Memory Map

The system memory mapping is flexible, with two levels of granularity for target address space allocation:
• L1: The four quarters are labeled Q0, Q1, Q2, and Q3. Each quarter corresponds to a 1-GB address space (the total low-address space is 4 GB, 32-bit). The CPU extended address range is labeled as high memory (Q8 – Q15) and provides a total of 8 GB.
• L2: Each quarter is divided into eight blocks of 32 MB, with target spaces mapped in the blocks.

Item	Address space	Description
Boot	0x4000 0000–0x400F FFFF	When booting from the on-chip ROM with the appropriate external sys_boot pin configuration, the lowest 1-MiB memory space [0x0000 0000–0x000F FFFF] is redirected to the on-chip boot ROM address space [0x4000 0000–0x400F FFFF]
GPMC	Q0 0x00000000–0x1FFFFFFF	
EMIF1/EMIF2 CS0	Q2 0x80000000–0xBFFFFFFF	
EMIF1/EMIF2 CS0	Q3 0xC0000000–0xFFFFFFFF	
QSPI	Q1 0x5C000000–0x5FFFFFFF	

6.1.2. I2C Address Allocation

IC	I2C address (7bit)	I2C address(R/W)
TPS659037(I2C1)	0x58 0x59 0x5A 0x5B	Power registers 0XB1/0XB0 Interfaces and auxiliaries 0XB3/0XB2 Trimming and test 0XB5/0XB4 OTP 0XB7/0XB6

6.1.3. Pins Definition Of BTB Connectors

CON1

NUMBER	BALL NUMBER	SINGAL	RESET STATE	NUMBER	BALL NUMBER	SINGAL	RESET STATE
1		GND		2		GND	
3	AH19	hdmi1_data2y		4	AB10	usb1_drvvbus/timer16/gpio6_12	PD
5	AG19	hdmi1_data2x		6	AD12	usb1_dp	
7		GND		8	AC12	usb1_dm	
9	AH18	hdmi1_data1y		10		GND	
11	AG18	hdmi1_data1x		12	AE12	usb_rxp0	
13		GND		14	AF12	usb_rxn0	
15	AH17	hdmi1_data0y		16		GND	
17	AG17	hdmi1_data0x		18	AD11	usb_txp0	
19		GND		20	AC11	usb_txn0	
21	AH16	hdmi1_clocky		22		GND	
23	AG16	hdmi1_clockx		24	AC10	usb2_drvvbus/timer15/gpio6_13	PD
25		GND		26	AE11	usb2_dp	
27	C25	hdmi1_ddc_scl	OFF	28	AF11	usb2_dm	
29	F17	hdmi1_ddc_sda	OFF	30		GND	
31	B20	hdmi1_ddc_cec	PU	32	AH9	sata1_rxn0	
33	B21	hdmi1_ddc_hpd	PU	34	AG9	sata1_rxp0	
35		GND		36		GND	
37	PCIE_REFCLKP	CDCM9102_OUTP0		38	AH10	sata1_txp0	
39	PCIE_REFCLKN	CDCM9102_OUTN0		40	AG10	sata1_txn0	
41		GND		42		GND	
43	AH13	pcie_rxp0		44	B27	uart1_rxd	PU
45	AG13	pcie_rxn0		46	C26	uart1_txd	PU
47		GND		48	D28	uart2_rxd	PU
49	AH14	pcie_txp0		50	D26	uart2_txd	PU
51	AG14	pcie_txn0		52	D27	uart3_rxd	PU
53		GND		54	C28	uart3_txd	PU
55	AH11	pcie_rxp1		56	AB3	uart9_ctsn	PD

57	AG11	pcie_rxn1		58	AA4	uart9_rtsn	PD
59		GND		60	E25	uart9_rxd/uart1_ctsn	PU
61	AH12	pcie_txp1		62	C27	uart9_txd/uart1_rtsn	PU
63	AH14	pcie_txn1		64		GND	
65		GND		66	C18	spi3_sclk	PD
67	A25	spi1_sclk/ gpio7_7	PD	68	A21	spi3_d1	PD
69	F16	spi1_d1/ gpio7_8	PD	70	G16	spi3_d0	PD
71	B25	spi1_d0/ gpio7_9	PD	72	D17	spi3_cs0	PD
73	A24	spi1_cs0/ gpio7_10	PU	74	B12	gpio5_10/mcasp1_axr8/timer5	PD
75	A22	spi1_cs1/ gpio7_11	PU	76	G14	gpio6_5/mcasp1_axr14/timer11	PD
77	B26	gpio6_19/mcasp2_axr10/xref_clk2	PD	78	F21	timer3/GPIO	PU
79		GND		80		GND	

CON2

NUMBER	BALL NUMBER	SINGAL	RESET STATE	NUMBER	BALL NUMBER	SINGAL	RESET STATE
1		GND		2		GND	
3	W9	rgmii0_txc	PD	4	AE8	vin1a_d0	PD
5	V9	rgmii0_txctl	PD	6	AD8	vin1a_d1	PD
7	V7	rgmii0_txd3	PD	8	AG7	vin1a_d2	PD
9	U7	rgmii0_txd2	PD	10	AH6	vin1a_d3	PD
11	V6	rgmii0_txd1	PD	12	AH3	vin1a_d4	PD
13	U6	rgmii0_txd0	PD	14	AH5	vin1a_d5	PD
15		GND		16	AG6	vin1a_d6	PD
17	U5	rgmii0_rxc	PD	18	AH4	vin1a_d7	PD
19	V5	rgmii0_rxctl	PD	20	AG4	vin1a_d8	PD
21	V4	rgmii0_rxd3	PD	22	AG2	vin1a_d9	PD
23	V3	rgmii0_rxd2	PD	24	AG3	vin1a_d10	PD
25	Y2	rgmii0_rxd1	PD	26	AG5	vin1a_d11	PD
27	W2	rgmii0_rxd0	PD	28	AF2	vin1a_d12	PD
29		GND		30	AF6	vin1a_d13	PD
31	U4	MDIO_D	PU	32	AF3	vin1a_d14	PD
33	V1	MDIO_CLK	PU	34	AF4	vin1a_d1	PD

						5	
35	Y1	GPIO5_19	PD	36	AF1	vin1a_d16	PD
37	V2	GPIO5_18	PD	38	AE3	vin1a_d17	PD
39	F5	GPIO4_9	PD	40	AE5	vin1a_d18	PD
41	F6	GPIO4_12	PD	42	AE1	vin1a_d19	PD
43	E14	gpio4_18/mcasp1_axr12/timer11	PD	44	AE2	vin1a_d20	PD
45	A13	gpio6_4/mcasp1_axr13/timer10	PD	46	AE6	vin1a_d21	PD
47	AA3	i2c5_sda/uart9_rxd	PD	48	AD2	vin1a_d22	PD
49	AB9	i2c5_scl/uart9_txd	PD	50	AD3	vin1a_d23	PD
51		GND		52		GND	
53	C23	CLKOUT3	PD	54	AG8	vin1a_clk0	PD
55		GND		56	AD9	vin1a_de0	PD
57		PWRON		58	AF9	vin1a_fld0	PD
59		PMIC_RESET_IN		60	AE9	vin1a_hsync0	PD
61		PMIC_VBUS		62	AF8	vin1a_vsync0	PD
63		GND		64		GND	
65		GND		66	W6	mmc1_clk	PU
67		GND		68	Y6	mmc1_cmd	PU
69		VDD_5V		70	AA6	mmc1_dat0	PU
71		VDD_5V		72	Y4	mmc1_dat1	PU
73		VDD_5V		74	AA5	mmc1_dat2	PU
75		VDD_5V		76	Y3	mmc1_dat3	PU
77		VDD_5V		78	W7	mmc1_sdcd	PU
79		VDD_5V		80		GND	

CON3

NUMBER	BALL NUMBER	SINGAL	RESET STATE	NUMBER	BALL NUMBER	SINGAL	RESET STATE
1		GND		2		GND	

3	A26	gpio7_14/spi2_sclk	PD	4	F11	vout1_d0	PD
5	B22	gpio7_15/spi2_d1	PD	6	G10	vout1_d1	PD
7	G17	gpio7_16/spi2_d0	PD	8	F10	vout1_d2	PD
9	B24	gpio7_17/spi2_cs0	PU	10	G11	vout1_d3	PD
11	AB8	gpio1_24	PU	12	E9	vout1_d4	PD
13	AB5	ecap3	PU	14	F9	vout1_d5	PD
15	B18	uart7_rxd	PD	16	F8	vout1_d6	PD
17	F15	uart7_txd	PD	18	E7	vout1_d7	PD
19	C17	uart7_rtsn	PD	20	E8	vout1_d8	PD
21	B19	uart7_ctsn	PD	22	D9	vout1_d9	PD
23	AC5	i2c3_sda	PU	24	D7	vout1_d10	PD
25	AB4	i2c3_scl	PU	26	D8	vout1_d11	PD
27		GND		28	A5	vout1_d12	PD
29	AD4	mmc3_clk	PU	30	C6	vout1_d13	PD
31	AC4	mmc3_cmd	PU	32	C8	vout1_d14	PD
33	AC7	mmc3_dat0	PU	34	C7	vout1_d15	PD
35	AC6	mmc3_dat1	PU	36	B7	vout1_d16	PD
37	AC9	mmc3_dat2	PU	38	B8	vout1_d17	PD
39	AC3	mmc3_dat3	PU	40	A7	vout1_d18	PD
41		GND		42	A8	vout1_d19	PD
43	AD6	uart10_txd	PU	44	C9	vout1_d20	PD
45	AC8	uart10_rxd	PU	46	A9	vout1_d21	PD
47	G20	dcan1_tx	PU	48	B9	vout1_d22	PD
49	G19	dcan1_rx	PU	50	A10	vout1_d23	PD
51	E21	dcan2_tx	PU	52		GND	
53	F20	dcan2_rx	PU	54	D11	vout1_clk	PD
55		GND		56	B10	vout1_de	PD
57	D18	mcasp1_ahclkx/xref_clk0/gpio6_17	PD	58	B11	vout1_fld	PD
59	D14	mcasp1_fsx/gpio7_10	PD	60	C11	vout1_hsync	PD
61	C14	mcasp1_aclkx/gpio7_31	PD	62	E11	vout1_vsync	PD
63	F12	mcasp1_axr1/gpio5_3	PD	64		GND	
65	G12	mcasp1_axr0/gpio5_2	PD	66	B17	gpio2_29/mcasp2_axr6	PD
67		GND		68	J14	i2c4_scl	PD
69	E17	mcasp2_ahclkx/gpio6_18	PD	70	B14	i2c4_sda	PD
71	A19	mcasp2_aclkx	PD	72	D21	nmin_dsp	PD
73	A18	mcasp2_fsx	PD	74	E23	resetn	PU
75	B15	mcasp2_axr0	PD	76	F23	rstoutn	PD
77	A15	mcasp2_axr1	PD	78	F22	porz	
79		GND		80		GND	

CON4

NUMBER	BALL NUMBER	SINGAL	RESET STATE	NUMBER	BALL NUMBER	SINGAL	RESET STATE

1		GND		2		GND	
3	R6	gpmc_a0	PD	4	M6	gpmc_ad0/sysboot0	OFF
5	T9	gpmc_a1	PD	6	M2	gpmc_ad1/sysboot1	OFF
7	T6	gpmc_a2	PD	8	L5	gpmc_ad2/sysboot2	OFF
9	T7	gpmc_a3	PD	10	M1	gpmc_ad3/sysboot3	OFF
11	P6	gpmc_a4	PD	12	L6	gpmc_ad4/sysboot4	OFF
13	R9	gpmc_a5	PD	14	L4	gpmc_ad5/sysboot5	OFF
15	R5	gpmc_a6	PD	16	L3	gpmc_ad6/sysboot6	OFF
17	P5	gpmc_a7	PD	18	L2	gpmc_ad7/sysboot7	OFF
19	N7	gpmc_a8	PD	20	L1	gpmc_ad8/sysboot8	OFF
21	R4	gpmc_a9	PD	22	K2	gpmc_ad9/sysboot9	OFF
23	N9	gpmc_a10	PD	24	J1	gpmc_ad10/sysboot10	OFF
25	P9	gpmc_a11	PD		J2	gpmc_ad11/sysboot11	OFF
27	P4	gpmc_a12	PD	28	H1	gpmc_ad12/sysboot12	OFF
29	R3	gpmc_a13	PD	30	J3	gpmc_ad13/sysboot13	OFF
31	T2	gpmc_a14	PD	32	H2	gpmc_ad14/sysboot14	OFF
33	U2	gpmc_a15	PD	34	H3	gpmc_ad15/sysboot15	OFF
35	U1	gpmc_a16	PD	36		GND	
37	P3	gpmc_a17	PD	38	P7	gpmc_clk	PU
39	R2	gpmc_a18	PD	40	N1	gpmc_advn_ale	PU
41	T1	gpmc_cs0	PU	42	M5	gpmc_oen_ren	PU
43	P1	gpmc_cs3	PU	44	M3	gpmc_wen	PU
45		GND		46	N6	gpmc_ben0	PU
47	E6	EHRPWM2A	PD	48	M4	gpmc_ben1	PU
49	D3	EHRPWM2B	PD	50	N2	gpmc_wait0	PU
51		GND		52		GND	
53	C5	rgmii1_txc	PD	54	E1	vin2a_clk0	PD
55	A3	rgmii1_txctl	PD	56	G2	vin2a_de0	PD
57	B3	rgmii1_txd3	PD	58	H7	vin2a_fld0	PD

59	B4	rgmii1_txd2	PD	60	G1	vin2a_hsync0	PD
61	B5	rgmii1_txd1	PD	62	G6	vin2a_vsync0	PD
63	A4	rgmii1_txd0	PD	64	F2	vin2a_d0	PD
65		GND		66	F3	vin2a_d1	PD
67	D5	rgmii1_rxc	PD	68	D1	vin2a_d2	PD
69	C2	rgmii1_rxctl	PD	70	E2	vin2a_d3	PD
71	C3	rgmii1_rxd3	PD	72	D2	vin2a_d4	PD
73	C4	rgmii1_rxd2	PD	74	F4	vin2a_d5	PD
75	B2	rgmii1_rxd1	PD	76	C1	vin2a_d6	PD
77	D6	rgmii1_rxd0	PD	78	E4	vin2a_d7	PD
79		GND		80		GND	