ASSIGNMENT NO: 05

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EXAMINED BY: Prof. G. B. Aochar	**EXPERIMENT NO: 5**

TITLE: Parity Generator Checker

PROBLEM STATEMENT: Design & Implement Parity Generator using EX-OR.

APPARATUS REQUIRED:

Digital trainer kit, ICs- 7486, 74LS08, 7404 Probs

THEORY:

Parity: A term used to specify the number of one's in a digital word as odd or even. There are two types of Parity - even and odd. An even parity generator will produce a logic 1 at its output ifthe data word contains an odd number of ones. If the data word contains an even number of ones then the output of the parity generator will be low. By concatenating the Parity bit to the data word, a word will be formed which always has an even number of ones i.e. has even parity.

Parity bit: An extra bit attached to a binary word to make the parity of resultant word even or odd. Parity bits are extra signals which are added to a data word to enable error checking.

7 bits of data	(count of 1-bits)	8 bits including parity	
		even	odd
0000000	0	**0**0000000	**1**0000000
1010001	3	**1**1010001	**0**1010001
1101001	4	**0**1101001	**1**1101001
1111111	7	**1**1111111	**0**1111111

Parity generator: A logic circuit that generates an additional bit which when appended to a digital word makes its parity as desired (odd or even).Parity generators calculate the parity ofdata packets and add a parity amount to them. Parity is used on communication links (e.g. Modem lines) and is often included in memory systems. If a data word is sent out with even parity, but has odd parity when it is received then the data has been corrupted and must be resent.As its name implies the operation of an Odd Parity generator is similar but it provides odd parity.The table shows the parity generator outputs for various 8-bit data words.

Parity checker: A logic circuit that checks the parity of binary word. Parity checkers are integrated circuits (ICs) used in digital systems to detect errors when streams of bits are sent from a transmitter to a receiver. The minimum distance between any two code words with parity bit attached is two. The parity bit 1 or 0 is attached to the code to be transmitted at the transmitter end and the parity of the received (n+1)-bit word is checked at the receiving end. If there is only one error, the erroneously code is detected at the receiving end by parity check.

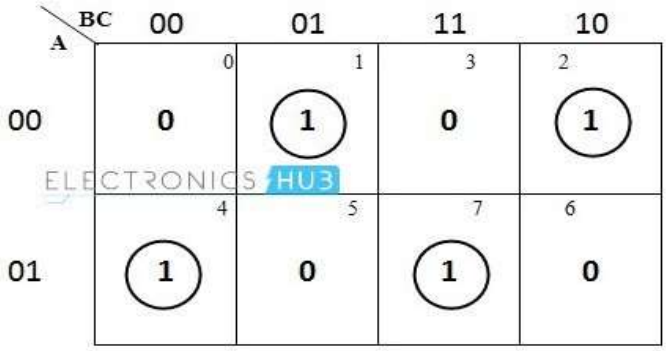
Design:

3 Bit Even Parity Generator

the truth table of even parity generator in which 1 is placed as parity bit in order to make all 1s as even when the number of 1s in the truth table is odd.

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The K-map simplification for 3-bit message even parity generator is



From the above truth table, the simplified expression of the parity bit can be written as

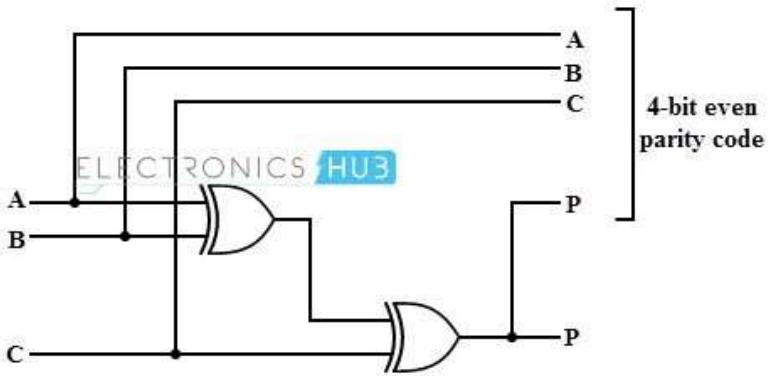
$$P = \bar{A}\,\bar{B}\,C + \bar{A}\,B\,\bar{C} + A\,\bar{B}\,\bar{C} + A\,B\,C$$

$$= \bar{A}\,(\bar{B}\,C + B\,\bar{C}) + A\,(\bar{B}\,\bar{C} + B\,C)$$

$$= \bar{A}\,(B \oplus C) + A\,(\overline{B \oplus C})$$

$$P = A \oplus B \oplus C$$

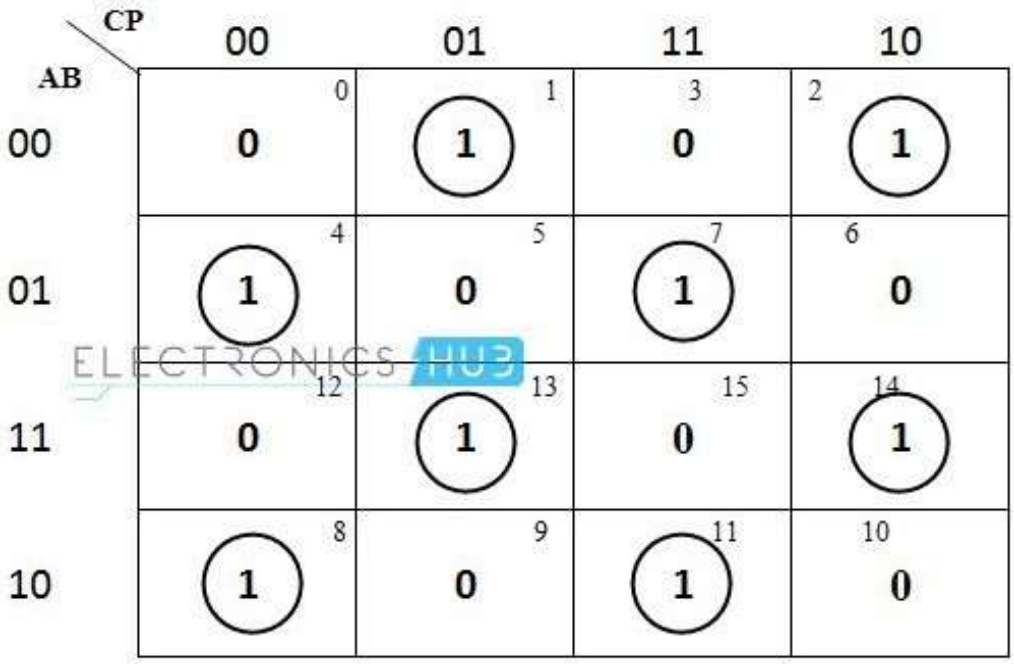
Digital Circuit:



Even Parity Checker

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

The above truth table can be simplified using K-map as shown below.



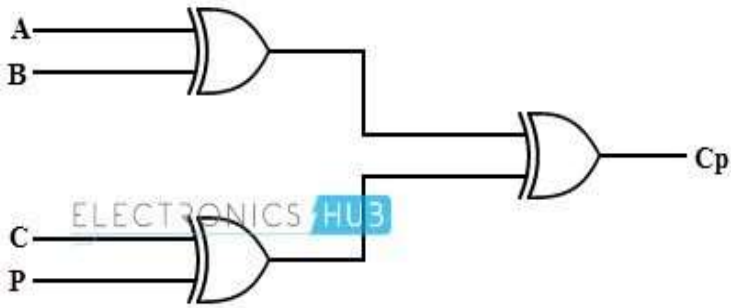
$$PEC = \bar{A}\ \bar{B}\ (\bar{C}\ D + C\ \bar{D}) + \bar{A}\ B\ (\bar{C}\ \bar{D} + C\ D) + A\ B\ (\bar{C}\ D + C\ \bar{D}) + A\ \bar{B}\ (\bar{C}\ \bar{D} + C\ D)$$

$$= \bar{A}\ \bar{B}\ (C \oplus D) + \bar{A}\ B\ (\overline{C \oplus D}) + A\ B\ (C \oplus D) + A\ \bar{B}\ (\overline{C \oplus D})$$

$$= (\bar{A}\ \bar{B} + A\ B)\ (C \oplus D) + (\bar{A}\ B + A\ \bar{B})\ (\overline{C \oplus D})$$

$$= (A \oplus B) \oplus (C \oplus D)$$

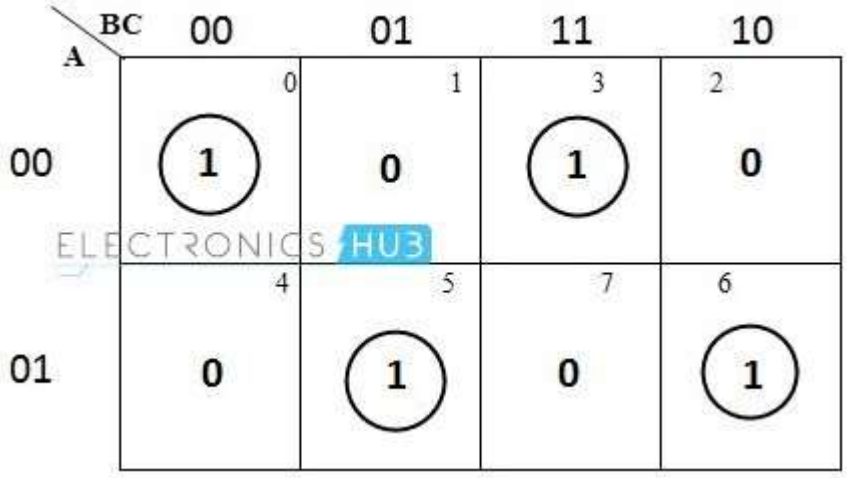
The above logic expression for the even parity checker can be implemented by using three Ex-OR gates as shown in figure. If the received message consists of five bits, then one more Ex-OR gate is required for the even parity checking.



Odd Parity Generator

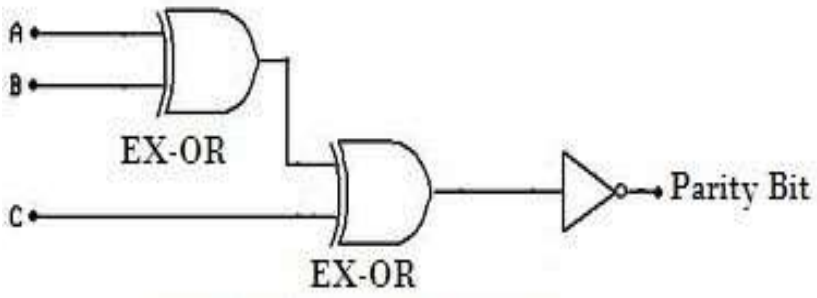
3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

The truth table of the odd parity generator can be simplified by using K-map as



The output parity bit expression for this generator circuit is obtained as

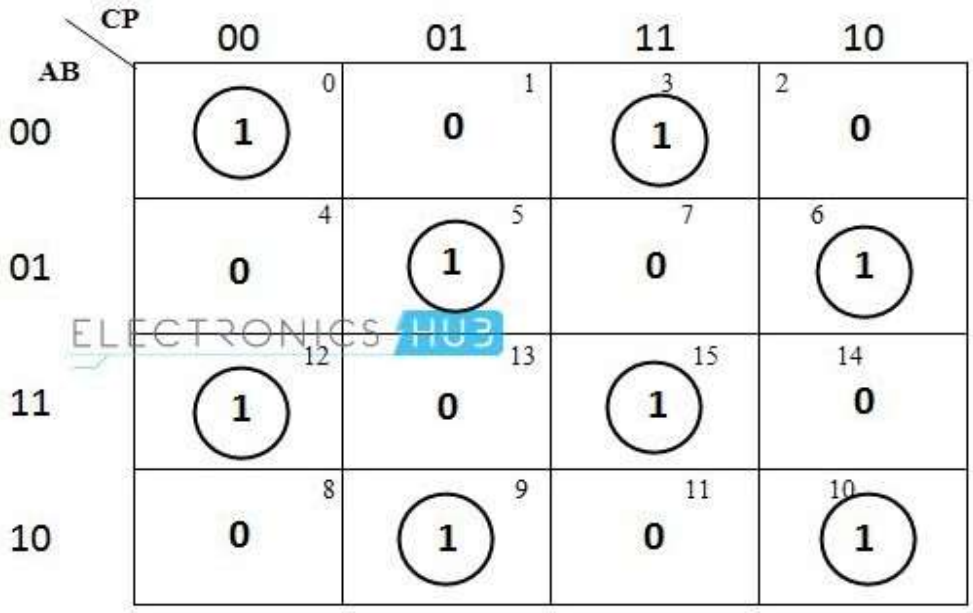
$$P = A \oplus B \text{ Ex-NOR } C$$



Odd Parity Checker

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

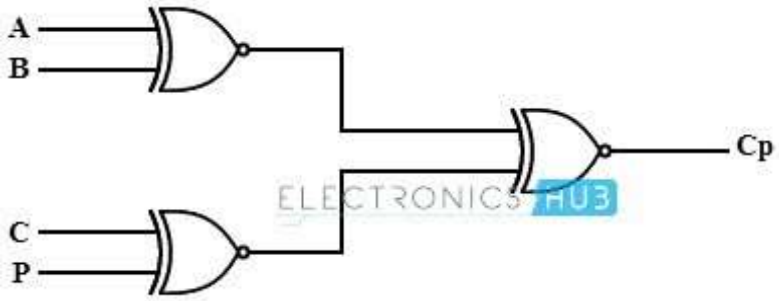
The expression for the PEC in the above truth table can be simplified by K-map as shown below.



After simplification, the final expression for the PEC is obtained as

PEC = (A Ex-NOR B) Ex-NOR (C Ex-NOR D)

The expression for the odd parity checker can be designed by using three Ex-NOR gates as shown below.

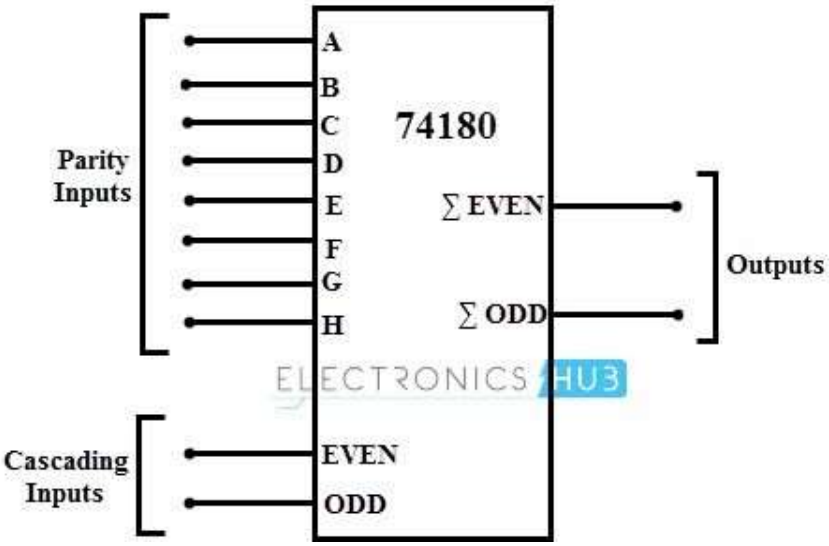


Parity Generator/Checker ICs

There are different types of parity generator /checker ICs are available with different input configurations such as 5-bit, 4-bit, 9-bit, 12-bit, etc. A most commonly used and standard type of parity generator/checker IC is 74180.

It is a 9-bit parity generator or checker used to detect errors in high speed data transmission or data retrieval systems. The figure below shows the pin diagram of 74180 IC.

This IC can be used to generate a 9-bit odd or even parity code or it can be used to check for odd or even parity in a 9-bit code (8 data bits and one parity bit).



This IC consists of eight parity inputs from A through H and two cascading inputs. There are two outputs even sum and odd sum. In implementing generator or checker circuits, unused parity bits must be tied to logic zero and the cascading inputs must not be equal.

Questions:

1. What is parity bit?
2. What is even parity and odd parity?
3. What is the use of parity bit?
4. What are the other error detecting codes and correcting?
5. What is IC 74180?
6. What is the disadvantage of parity bit used for error detection?