ASSIGNMENT NO. 01

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SEMESTER/YEAR: Sem-3 / 2022-23	**ROLL NO:** 015
DATE OF PERFORMANCE: / /2022	**DATE OF SUBMISSION:** / /2022
EXAMINED BY: Prof. G. B. Aochar	**EXPERIMENT NO: 1**

TTILE: To study the Realization of Full Adder and Subtractor using
a) Basic Gates and b) Universal Gates

PROBLEM STATEMENT: To Realize Full Adder and Subtractor using

a) Basic Gates and b) Universal Gates

PRE-REQUISITE:

Digital trainer kit, ICs- 74LS08, 74LS86, 74LS00, 74LS02, Probs

THEORY:

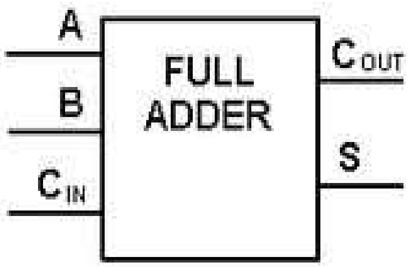
1) Implementation of Full Adder:

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of these variables denoted by A and B represent the two significant bits to be added. The third input represents the carry from previous lower significant position. From the truth-table, the full adder logic can be implemented. We can see that the output S is an EXOR between the input A and the half-adder SUM output with B and CIN inputs. We must also note that the COUT will only be true if any of the two inputs out of the three are HIGH.

Thus, we can implement a full adder circuit with the help of two half adder circuits. The first will half adder will be used to add A and B to produce a partial Sum. The second half adder logic can be used to add CIN to the Sum produced by the first half adder to get the final S output. If any of the half adder logic produces a carry, there will be an output carry. Thus, COUT will be an OR function of the half-adder Carry outputs. Take a look at the Logic Diagram & implementation of the full adder circuit shown below.

Implementation of Full Adder using Basic Gates:

Logic Diagram:

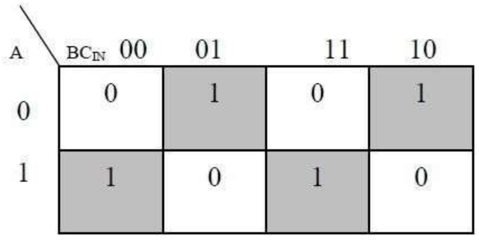


Truth Table for Design of full adder:

Input			*Output*	
A	**B**	**C**	**Sum**	**Carry**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

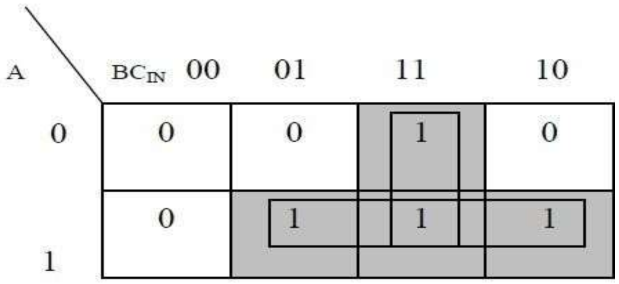
Based on the truth table, the Boolean functions for Sum (S) and Carry – out (COUT) can be derived using

K – Map For Sum S



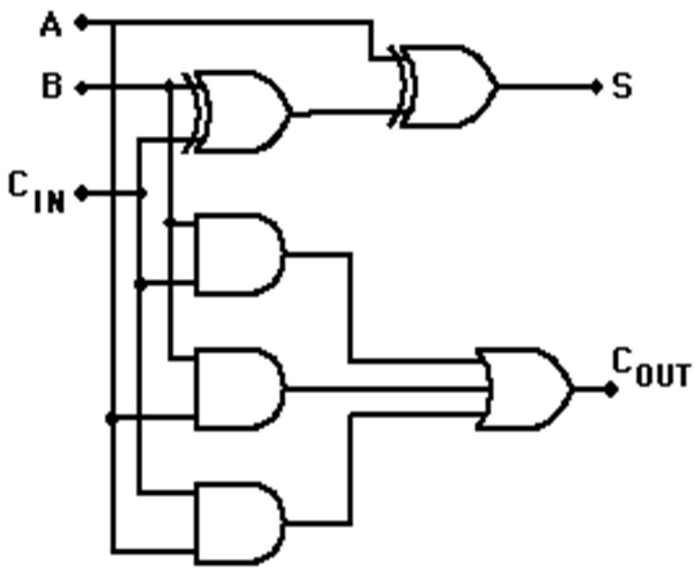
SUM = A EXOR B EXOR Cin

K – Map For Carry C



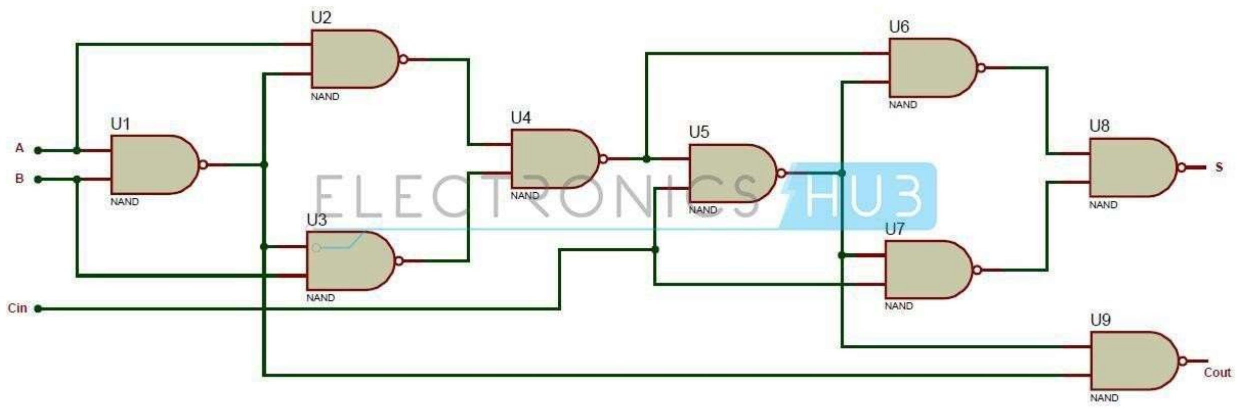
1. **Carry = (A AND B) OR (A AND C) OR (B AND C)**

Logic Circuit for Full Adder



Implementation of Full Adder using Universal Gates:

As mentioned earlier, a NAND gate is one of the universal gates and can be used to implement any logic design. The circuit of full adder using only NAND gates is shown below.



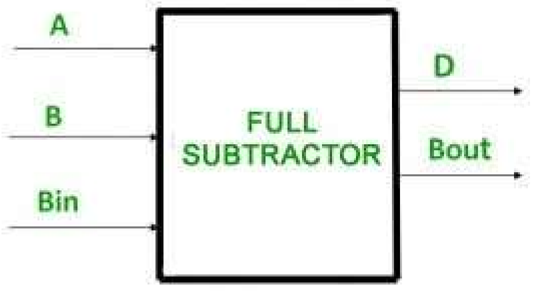
2) Implementation of Full Subtractor:

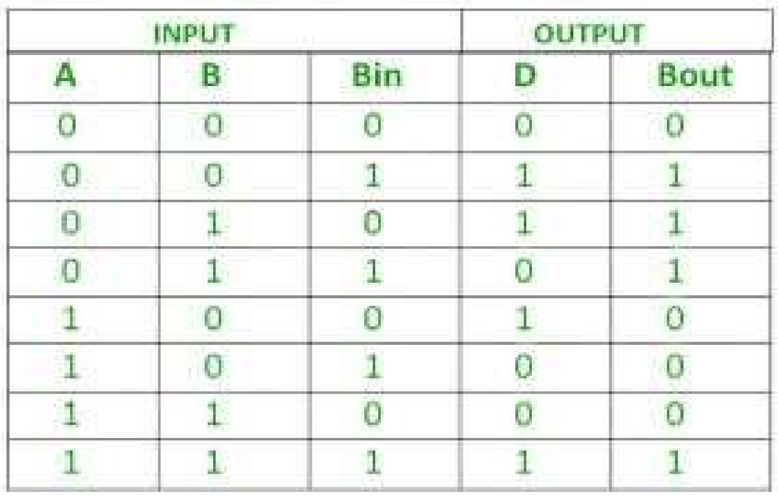
The full subtractor is a Combinational Circuit which is used to perform subtraction of three input bits : the minuend , subtrahend , and borrow in . The full subtractor generates two output bits: the difference and borrow out . is set when the previous digit borrowed from . Thus, is also subtracted from as well as the subtrahend. Like the half subtractor, the full subtractor generates a borrow out when it needs to borrow from the next digit. Since we are subtracting by and , a borrow out needs to be generated when .

When a borrow out is generated, 2 is added in the current digit. (This is similar to the subtraction algorithm in decimal. Instead of adding 2, we add 10 when borrow.)

Implementation of Full Subtravtor using Basic Gates:

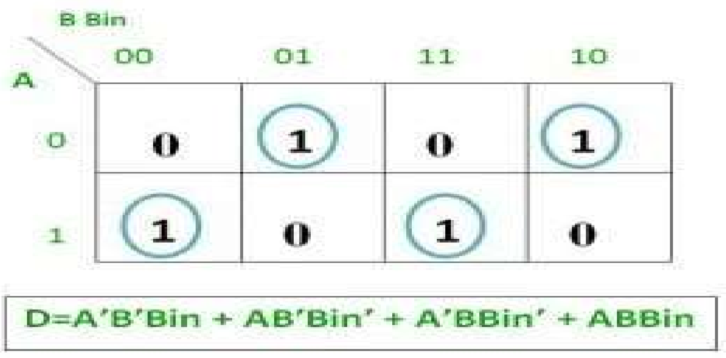
Logic Diagram:





INPUT			OUTPUT	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

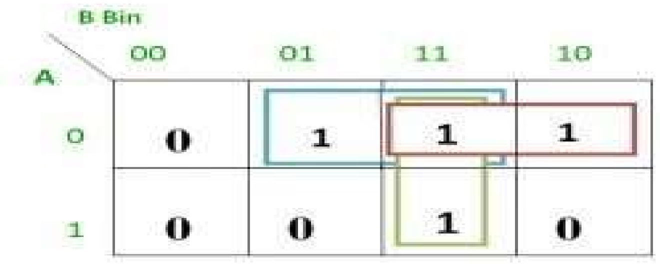
From above table we can draw the K-Map as shown for “difference” and “borrow”.



A \ B Bin	00	01	11	10
0	0	1	0	1
1	1	0	1	0

D=A’B’Bin + AB’Bin’ + A’BBin’ + ABBin

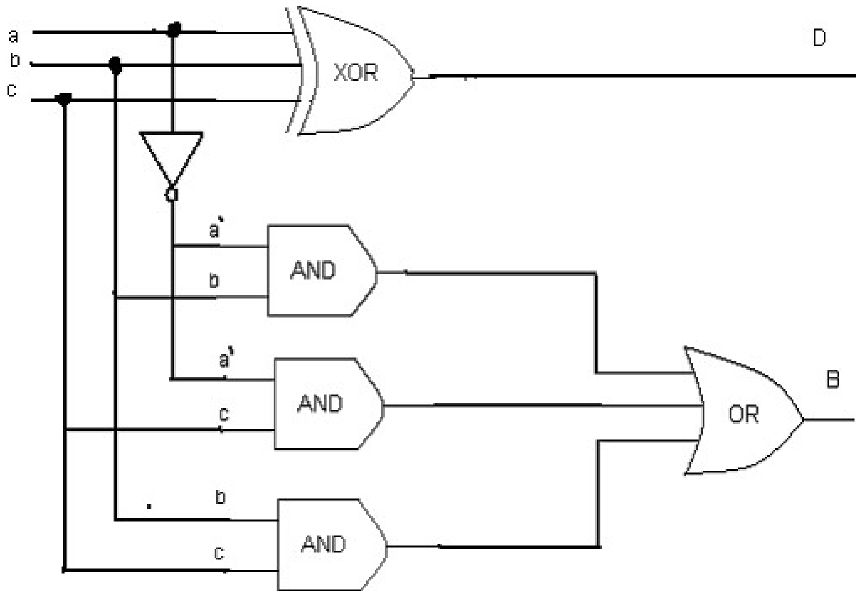
Difference= A EXOR B EXOR Bin



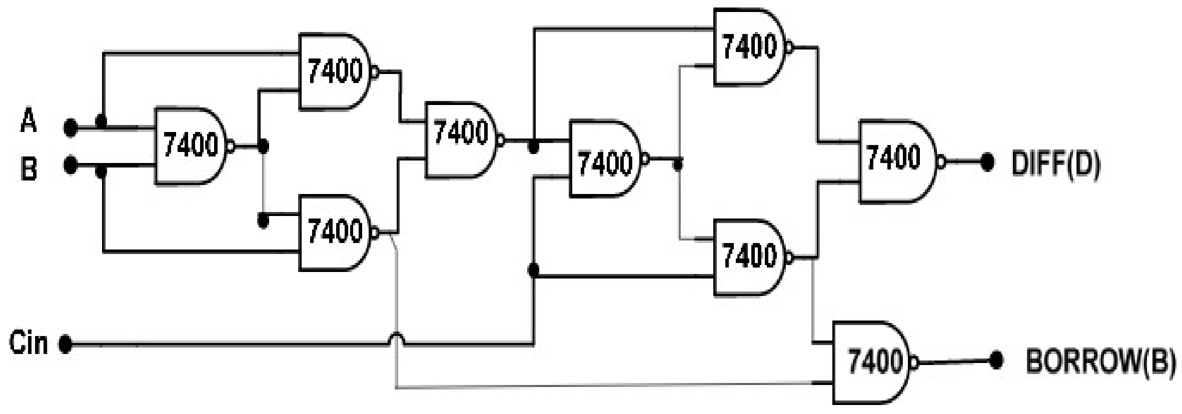
A \ B Bin	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$$B_{out} = A'B_{in} + A'B + BB_{in}$$

Logic Circuit for Full Subtractor



2. Implementation of Full Subtractor using Universal Gates:



QUESTIONS:

1. Which are universal gates?
2. What NAND gate and NOR gate called Universal gates?
3. Explain types of Ic's.
4. What is Full Adder?
5. Disadvantage of Half Adder.
6. What is Full subtractor?
7. Disadvantage of Half subtractor?
8. How Full adder is implemented using half adder?