ASSIGNMENT SET – II

Assignment-II is only for those who have completed the evaluation of the Assignment-I successfully.

A universal gate can be use to implement any Boolean function without the need of any other primitive logic gates. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and more comfortable to fabricate and are used in most of the integrated circuits (IC) of digital logic families.

The objective of Assignment-II is to implement all the logic function shown below. The only building blocks that you can use are NAND gates and the composite gates that you have created on top of them in Assignment-I.

The only tool that you required for this assignment is the ModelSim-Intel FPGA Starter Edition. All the logic functions should be implemented using Verilog HDL in the given order. Students are expected to design only Gate-Level Modeling (Structural Modeling) for the implementation.

As the assignment progress, students have to call/use the essential logical functions that are already implemented by him/her for building other logical functions.

1. Half Adder
2. Full Adder
3. 4-bit Incrementer
4. 4-bit Adder
5. 4-bit Negator (Hint: input: x output:!x)
6. 16-bit Adder
7. 16-bit Incrementer
8. 16-bit Negator (Hint: input: x output:!x)
9. Arithmetic-Logic Unit with following functions on two 16-bit inputs (x, y):

a. x+y	g. x	m. x+1
b. x-y	h. y	n. y+1
c. y–x	i. –x	o. x-1
d. 0	j. –y	p. y-1
e. 1	k. !x	q. x&y
f. -1	l. !y	r. x|y