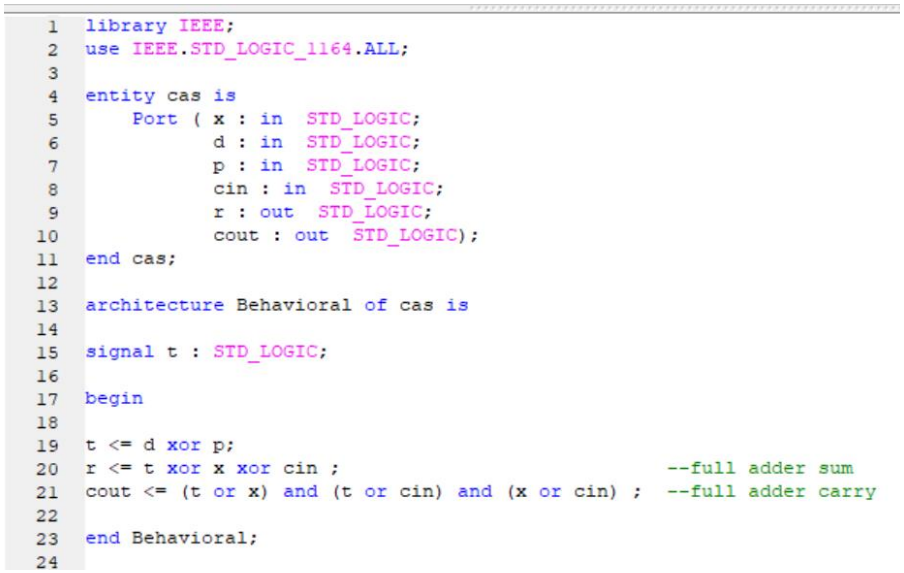
گزارش تمرین vhdl سری 2 معماری کامپیوتر

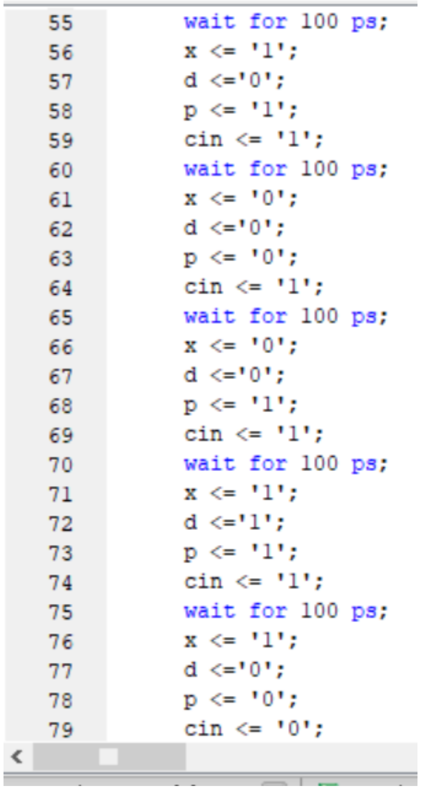
آنوشا شریعتی 9923041

ماژول cas و تست بنچ :

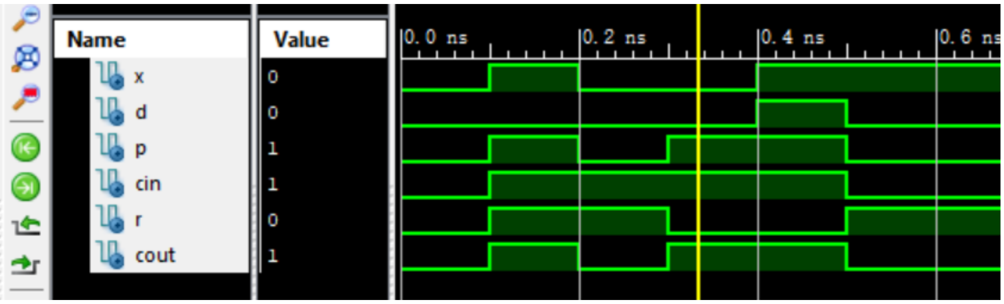
طبق مدار داده شده در صورت سوال ماژول به شکل روبه رو طراحی شد. برای طراحی به یک بلوک فول ادر نیز نیاز داشتیم ولی برای راحتی کار به صورت ماژول جدا تعریف نشد و با توجه به مدار آن و با تعریف سیگنال t کد آن نوشته شد.

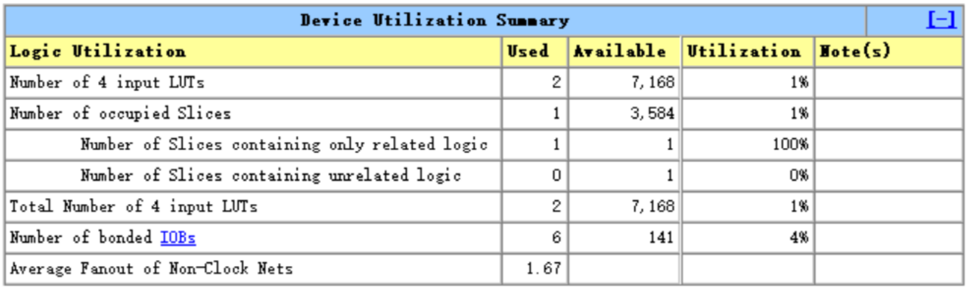


```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity cas is
    Port ( x : in  STD_LOGIC;
           d : in  STD_LOGIC;
           p : in  STD_LOGIC;
           cin : in  STD_LOGIC;
           r : out  STD_LOGIC;
           cout : out  STD_LOGIC);
end cas;

architecture Behavioral of cas is

signal t : STD_LOGIC;

begin

t <= d xor p;
r <= t xor x xor cin ;                          --full adder sum
cout <= (t or x) and (t or cin) and (x or cin) ;  --full adder carry

end Behavioral;

```



```
        wait for 100 ps;
        x <= '1';
        d <='0';
        p <= '1';
        cin <= '1';
        wait for 100 ps;
        x <= '0';
        d <='0';
        p <= '0';
        cin <= '1';
        wait for 100 ps;
        x <= '0';
        d <='0';
        p <= '1';
        cin <= '1';
        wait for 100 ps;
        x <= '1';
        d <='1';
        p <= '1';
        cin <= '1';
        wait for 100 ps;
        x <= '1';
        d <='0';
        p <= '0';
        cin <= '0';
```

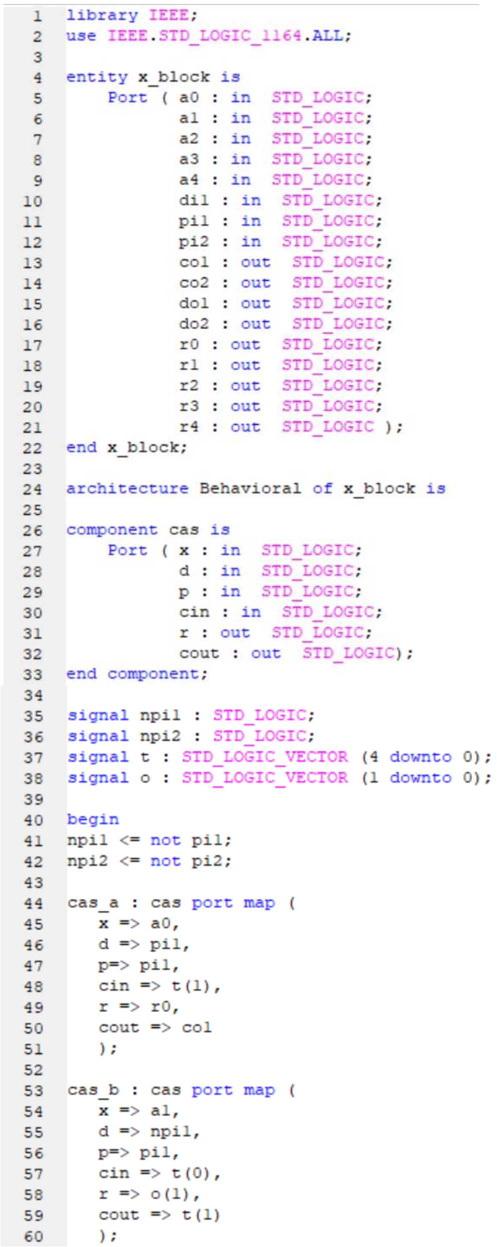




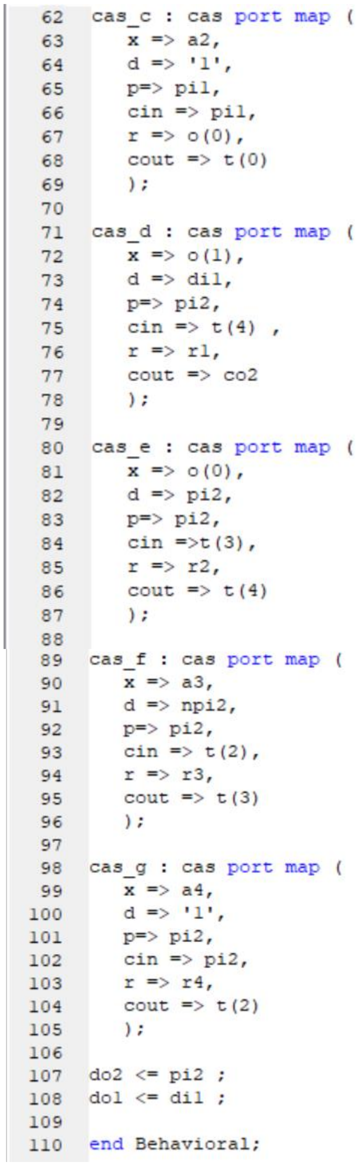
Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	2	7,168	1%	
Number of occupied Slices	1	3,584	1%	
Number of Slices containing only related logic	1	1	100%	
Number of Slices containing unrelated logic	0	1	0%	
Total Number of 4 input LUTs	2	7,168	1%	
Number of bonded IOBs	6	141	4%	
Average Fanout of Non-Clock Nets	1.67			

ماژول x :

برای طراحی این ماژول از ماژول cas که در قسمت قبل توضیح داده شد به صورت component استفاده کردیم. سپس با استفاده از شکل مدار داده شده در صورت سوال با دستورport map ورودی و خروجی های ماژول cas را مشخص میکنیم.

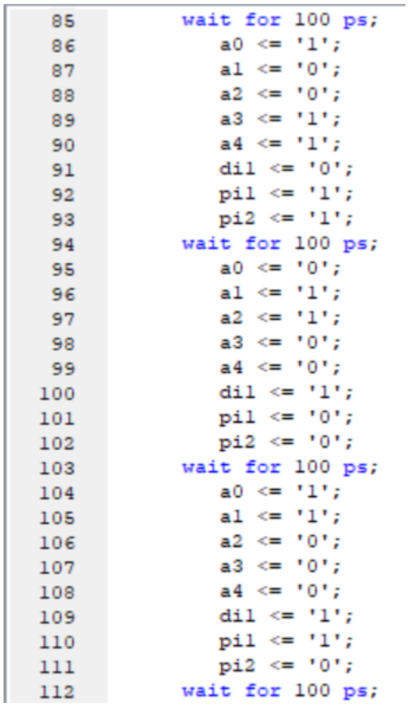


```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity x_block is
    Port ( a0 : in  STD_LOGIC;
           a1 : in  STD_LOGIC;
           a2 : in  STD_LOGIC;
           a3 : in  STD_LOGIC;
           a4 : in  STD_LOGIC;
           di1 : in  STD_LOGIC;
           pi1 : in  STD_LOGIC;
           pi2 : in  STD_LOGIC;
           co1 : out  STD_LOGIC;
           co2 : out  STD_LOGIC;
           do1 : out  STD_LOGIC;
           do2 : out  STD_LOGIC;
           r0 : out  STD_LOGIC;
           r1 : out  STD_LOGIC;
           r2 : out  STD_LOGIC;
           r3 : out  STD_LOGIC;
           r4 : out  STD_LOGIC );
end x_block;

architecture Behavioral of x_block is

component cas is
    Port ( x : in  STD_LOGIC;
           d : in  STD_LOGIC;
           p : in  STD_LOGIC;
           cin : in  STD_LOGIC;
           r : out  STD_LOGIC;
           cout : out  STD_LOGIC);
end component;

signal npi1 : STD_LOGIC;
signal npi2 : STD_LOGIC;
signal t : STD_LOGIC_VECTOR (4 downto 0);
signal o : STD_LOGIC_VECTOR (1 downto 0);

begin
npi1 <= not pi1;
npi2 <= not pi2;

cas_a : cas port map (
   x => a0,
   d => pi1,
   p=> pi1,
   cin => t(1),
   r => r0,
   cout => co1
   );

cas_b : cas port map (
   x => a1,
   d => npi1,
   p=> pi1,
   cin => t(0),
   r => o(1),
   cout => t(1)
   );
```

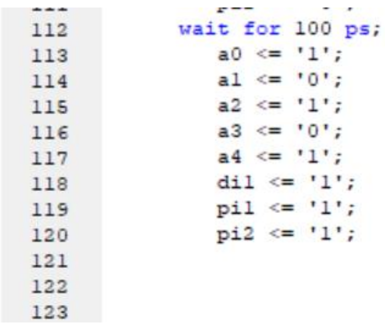


```vhdl
cas_c : cas port map (
   x => a2,
   d => '1',
   p=> pi1,
   cin => pi1,
   r => o(0),
   cout => t(0)
   );

cas_d : cas port map (
   x => o(1),
   d => di1,
   p=> pi2,
   cin => t(4)  ,
   r => r1,
   cout => co2
   );

cas_e : cas port map (
   x => o(0),
   d => pi2,
   p=> pi2,
   cin =>t(3),
   r => r2,
   cout => t(4)
   );

cas_f : cas port map (
   x => a3,
   d => npi2,
   p=> pi2,
   cin => t(2),
   r => r3,
   cout => t(3)
   );

cas_g : cas port map (
   x => a4,
   d => '1',
   p=> pi2,
   cin => pi2,
   r => r4,
   cout => t(2)
   );

do2 <= pi2 ;
do1 <= di1 ;

end Behavioral;
```

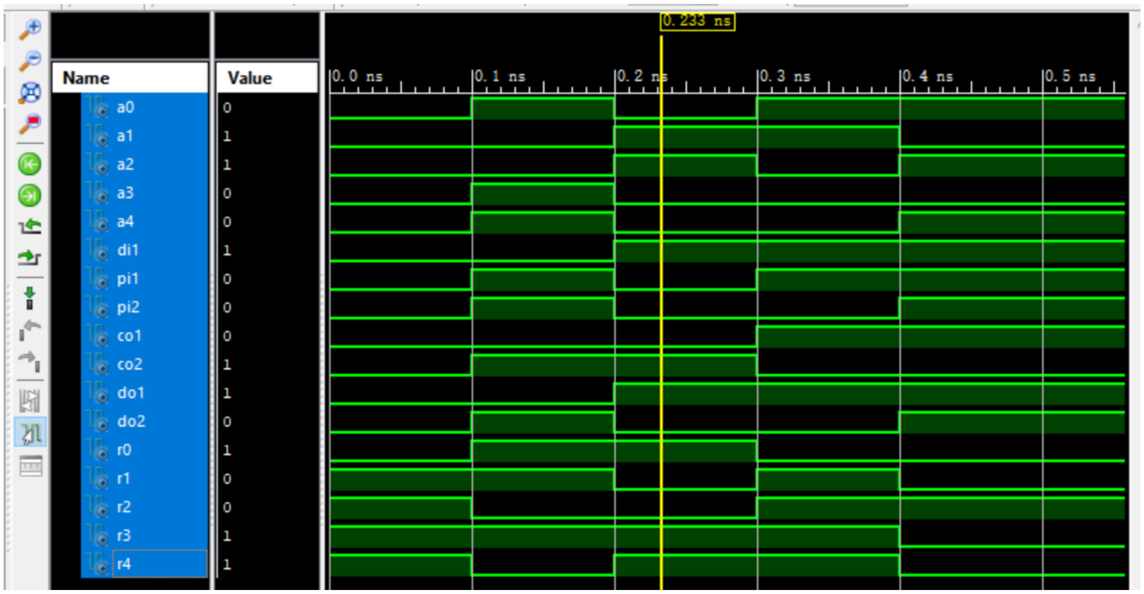
تست بنچ ماژول x :



```
    wait for 100 ps;
        a0 <= '1';
        a1 <= '0';
        a2 <= '0';
        a3 <= '1';
        a4 <= '1';
        di1 <= '0';
        pi1 <= '1';
        pi2 <= '1';
    wait for 100 ps;
        a0 <= '0';
        a1 <= '1';
        a2 <= '1';
        a3 <= '0';
        a4 <= '0';
        di1 <= '1';
        pi1 <= '0';
        pi2 <= '0';
    wait for 100 ps;
        a0 <= '1';
        a1 <= '1';
        a2 <= '0';
        a3 <= '0';
        a4 <= '0';
        di1 <= '1';
        pi1 <= '1';
        pi2 <= '0';
    wait for 100 ps;
```

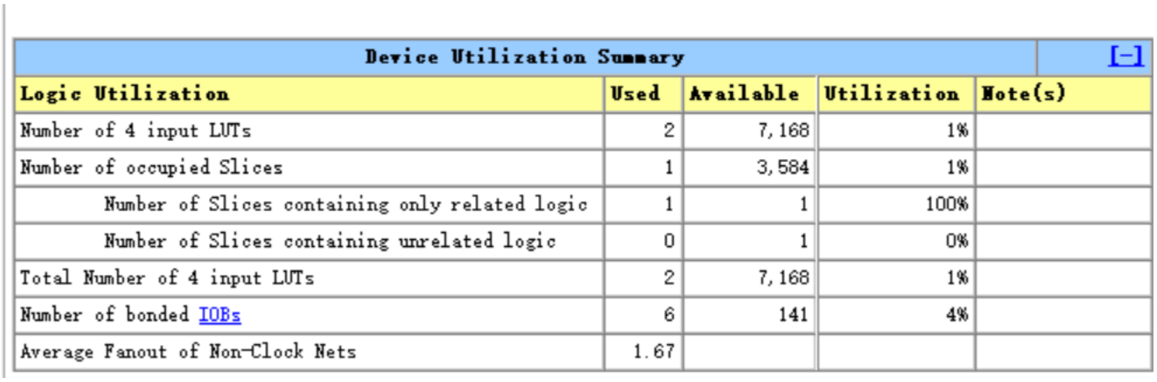


```
    wait for 100 ps;
        a0 <= '1';
        a1 <= '0';
        a2 <= '1';
        a3 <= '0';
        a4 <= '1';
        di1 <= '1';
        pi1 <= '1';
        pi2 <= '1';
```



Name	Value
a0	0
a1	1
a2	1
a3	0
a4	0
di1	1
pi1	0
pi2	0
co1	0
co2	1
do1	1
do2	0
r0	1
r1	0
r2	0
r3	1
r4	1

سطوح مصرف:

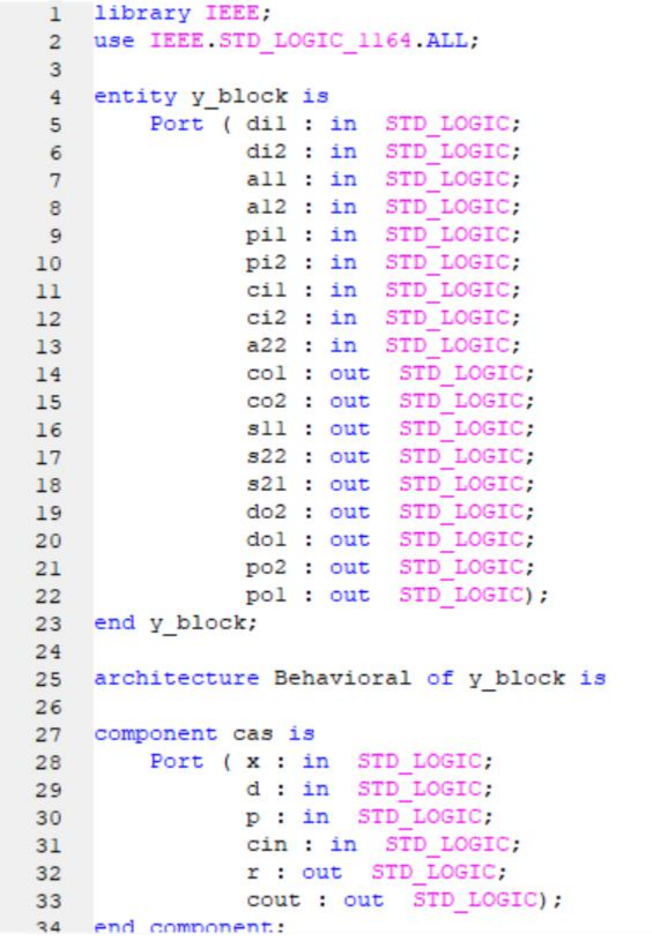


Device Utilization Summary [-]

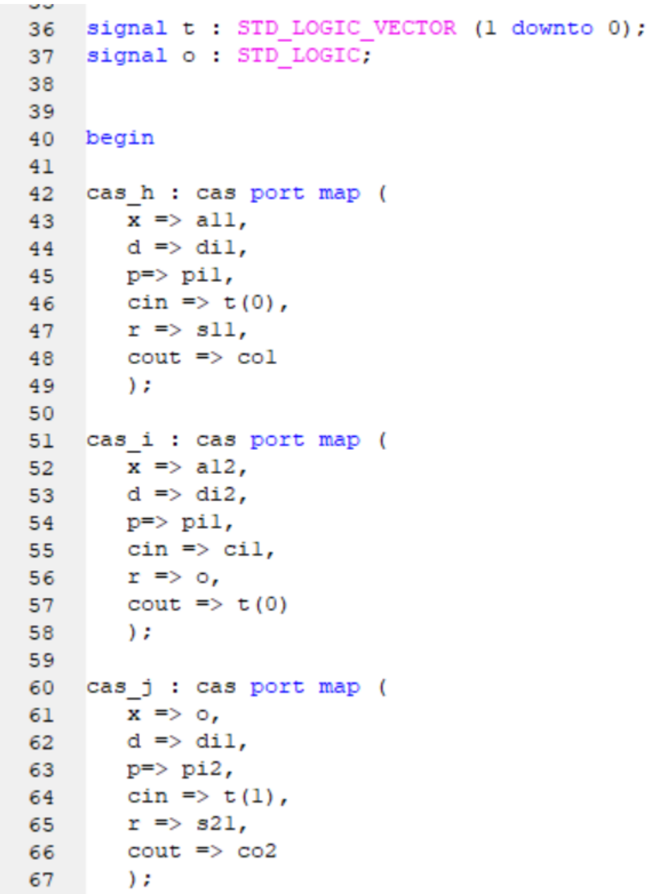
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	2	7,168	1%	
Number of occupied Slices	1	3,584	1%	
Number of Slices containing only related logic	1	1	100%	
Number of Slices containing unrelated logic	0	1	0%	
Total Number of 4 input LUTs	2	7,168	1%	
Number of bonded IOBs	6	141	4%	
Average Fanout of Non-Clock Nets	1.67			

ماژول y :

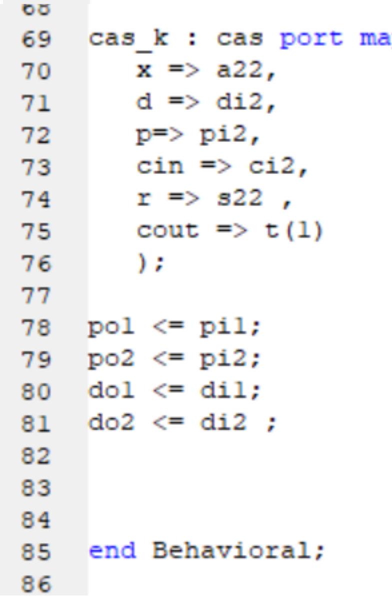
برای طراحی این ماژول مانند ماژول x از بلوک cas استفاده کردیم و با استفاده از شکل مدار خروجی و ورودی های آن را تعیین کردیم.



```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity y_block is
    Port ( di1 : in  STD_LOGIC;
           di2 : in  STD_LOGIC;
           a11 : in  STD_LOGIC;
           a12 : in  STD_LOGIC;
           pi1 : in  STD_LOGIC;
           pi2 : in  STD_LOGIC;
           ci1 : in  STD_LOGIC;
           ci2 : in  STD_LOGIC;
           a22 : in  STD_LOGIC;
           co1 : out  STD_LOGIC;
           co2 : out  STD_LOGIC;
           s11 : out  STD_LOGIC;
           s22 : out  STD_LOGIC;
           s21 : out  STD_LOGIC;
           do2 : out  STD_LOGIC;
           do1 : out  STD_LOGIC;
           po2 : out  STD_LOGIC;
           po1 : out  STD_LOGIC);
end y_block;

architecture Behavioral of y_block is

component cas is
    Port ( x : in  STD_LOGIC;
           d : in  STD_LOGIC;
           p : in  STD_LOGIC;
           cin : in  STD_LOGIC;
           r : out  STD_LOGIC;
           cout : out  STD_LOGIC);
end component;
```

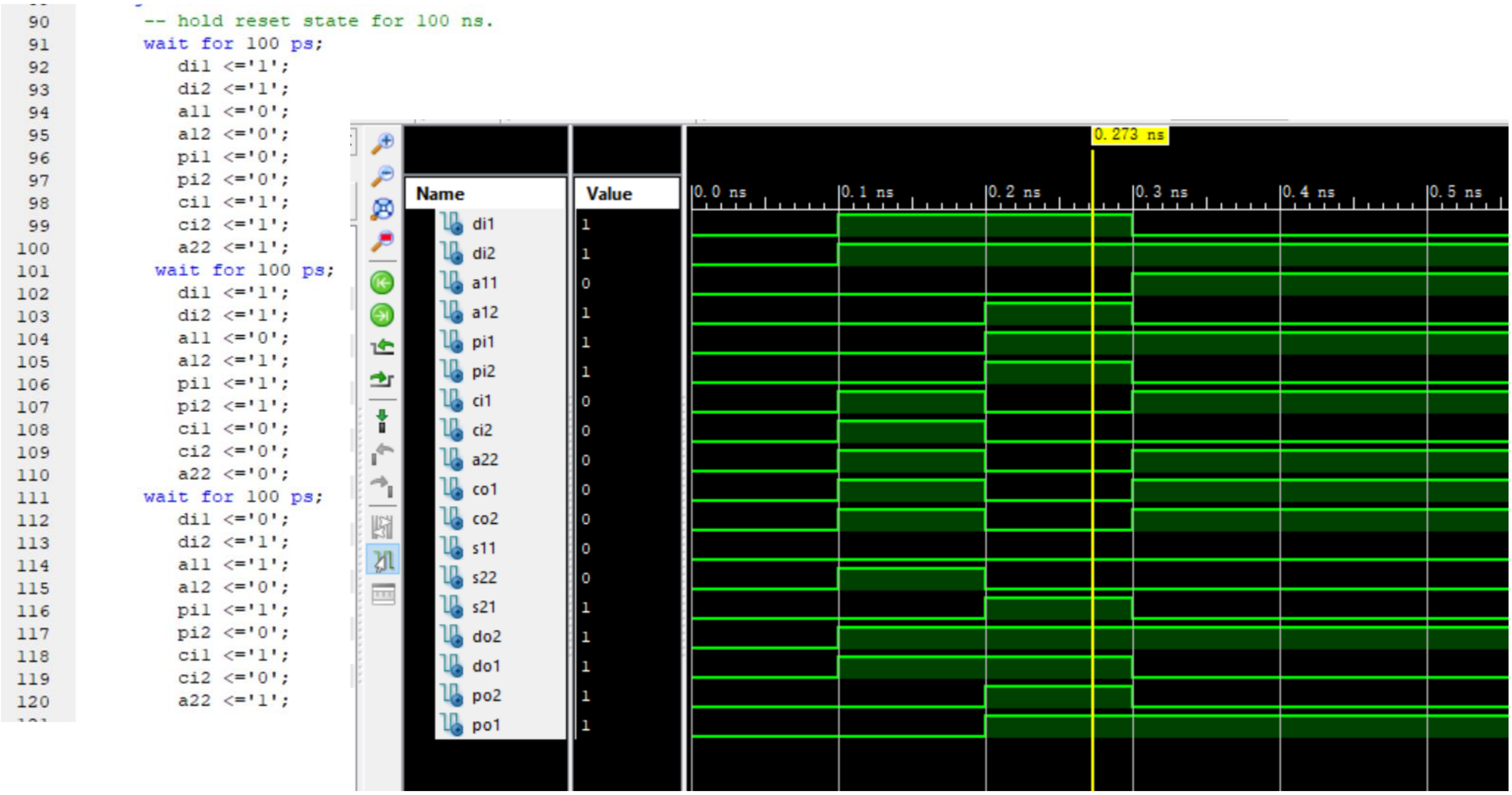


```
signal t : STD_LOGIC_VECTOR (1 downto 0);
signal o : STD_LOGIC;


begin

cas_h : cas port map (
   x => a11,
   d => di1,
   p=> pi1,
   cin => t(0),
   r => s11,
   cout => co1
   );

cas_i : cas port map (
   x => a12,
   d => di2,
   p=> pi1,
   cin => ci1,
   r => o,
   cout => t(0)
   );

cas_j : cas port map (
   x => o,
   d => di1,
   p=> pi2,
   cin => t(1),
   r => s21,
   cout => co2
   );
```



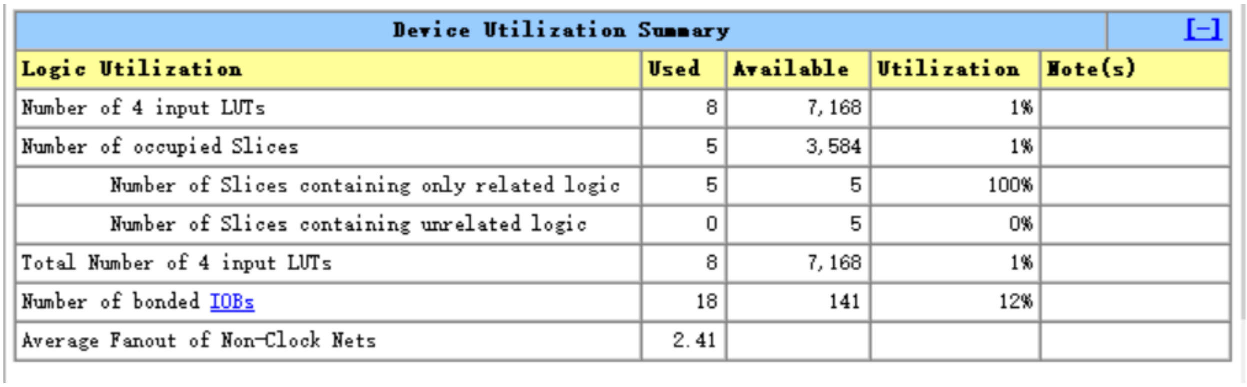
```
cas_k : cas port map (
   x => a22,
   d => di2,
   p=> pi2,
   cin => ci2,
   r => s22 ,
   cout => t(1)
   );

po1 <= pi1;
po2 <= pi2;
do1 <= di1;
do2 <= di2 ;



end Behavioral;

```

تست بنچ ماژول y :



```
 -- hold reset state for 100 ns.
 wait for 100 ps;
    di1 <='1';
    di2 <='1';
    a11 <='0';
    a12 <='0';
    pi1 <='0';
    pi2 <='0';
    ci1 <='1';
    ci2 <='1';
    a22 <='1';
  wait for 100 ps;
    di1 <='1';
    di2 <='1';
    a11 <='0';
    a12 <='1';
    pi1 <='1';
    pi2 <='1';
    ci1 <='0';
    ci2 <='0';
    a22 <='0';
 wait for 100 ps;
    di1 <='0';
    di2 <='1';
    a11 <='1';
    a12 <='0';
    pi1 <='1';
    pi2 <='0';
    ci1 <='1';
    ci2 <='0';
    a22 <='1';
```

سطوح مصرف:

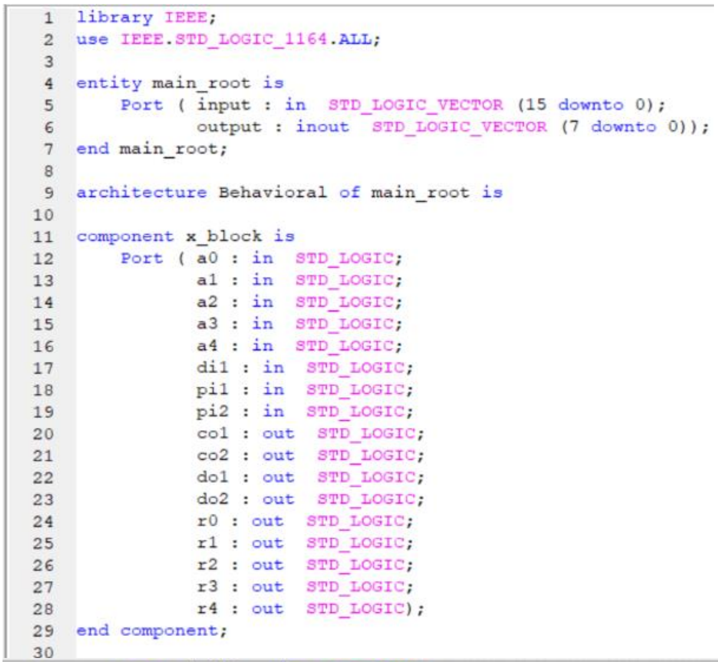


Device Utilization Summary [-]

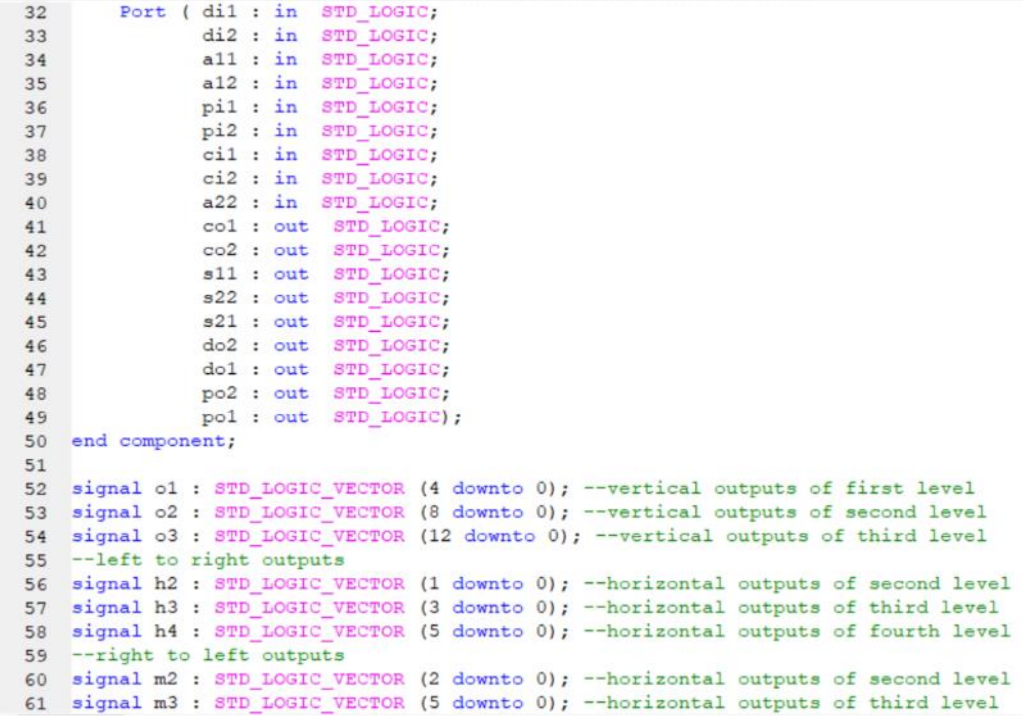
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	8	7,168	1%	
Number of occupied Slices	5	3,584	1%	
Number of Slices containing only related logic	5	5	100%	
Number of Slices containing unrelated logic	0	5	0%	
Total Number of 4 input LUTs	8	7,168	1%	
Number of bonded IOBs	18	141	12%	
Average Fanout of Non-Clock Nets	2.41			

کد اصلی:

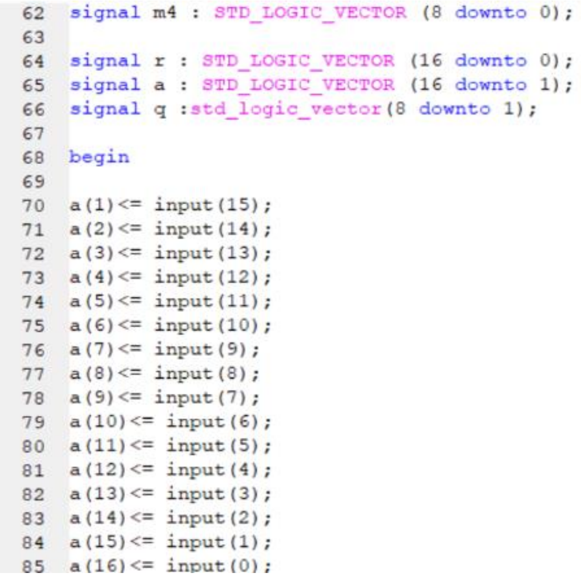
برای نوشتن کد اصلی از دو بلاک x,y که در قسمت قبل تعریف شد به صورت component استفاده میکنیم.
سپس سیگنال های زیر را برای ارتباط بین ماژول ها تعریف میکنیم. سپس با دستور پورت مپ برای هر
ماژول استفاده شده ورودی و خروجی ها را طبق شکل تعیین میکنیم. (کد خلاصه شده طبقه آخر)



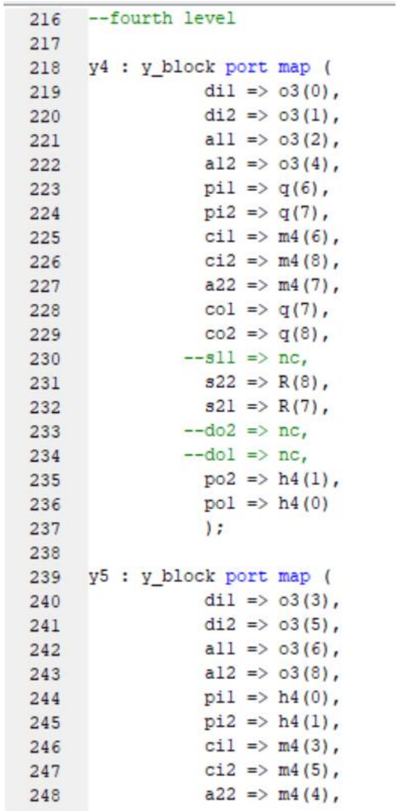
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity main_root is
    Port ( input : in  STD_LOGIC_VECTOR (15 downto 0);
           output : inout  STD_LOGIC_VECTOR (7 downto 0));
end main_root;

architecture Behavioral of main_root is

component x_block is
    Port ( a0 : in  STD_LOGIC;
           a1 : in  STD_LOGIC;
           a2 : in  STD_LOGIC;
           a3 : in  STD_LOGIC;
           a4 : in  STD_LOGIC;
           di1 : in  STD_LOGIC;
           pi1 : in  STD_LOGIC;
           pi2 : in  STD_LOGIC;
           co1 : out  STD_LOGIC;
           co2 : out  STD_LOGIC;
           do1 : out  STD_LOGIC;
           do2 : out  STD_LOGIC;
           r0 : out  STD_LOGIC;
           r1 : out  STD_LOGIC;
           r2 : out  STD_LOGIC;
           r3 : out  STD_LOGIC;
           r4 : out  STD_LOGIC);
end component;

```



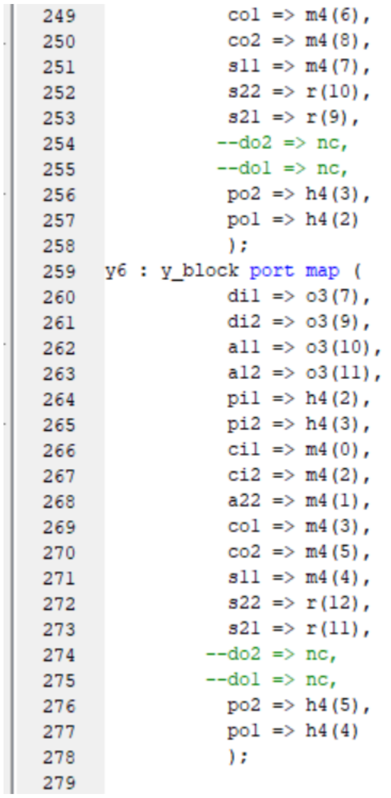
```vhdl
    Port ( di1 : in  STD_LOGIC;
           di2 : in  STD_LOGIC;
           a11 : in  STD_LOGIC;
           a12 : in  STD_LOGIC;
           pi1 : in  STD_LOGIC;
           pi2 : in  STD_LOGIC;
           ci1 : in  STD_LOGIC;
           ci2 : in  STD_LOGIC;
           a22 : in  STD_LOGIC;
           co1 : out  STD_LOGIC;
           co2 : out  STD_LOGIC;
           s11 : out  STD_LOGIC;
           s22 : out  STD_LOGIC;
           s21 : out  STD_LOGIC;
           do2 : out  STD_LOGIC;
           do1 : out  STD_LOGIC;
           po2 : out  STD_LOGIC;
           po1 : out  STD_LOGIC);
end component;

signal o1 : STD_LOGIC_VECTOR (4 downto 0); --vertical outputs of first level
signal o2 : STD_LOGIC_VECTOR (8 downto 0); --vertical outputs of second level
signal o3 : STD_LOGIC_VECTOR (12 downto 0); --vertical outputs of third level
--left to right outputs
signal h2 : STD_LOGIC_VECTOR (1 downto 0); --horizontal outputs of second level
signal h3 : STD_LOGIC_VECTOR (3 downto 0); --horizontal outputs of third level
signal h4 : STD_LOGIC_VECTOR (5 downto 0); --horizontal outputs of fourth level
--right to left outputs
signal m2 : STD_LOGIC_VECTOR (2 downto 0); --horizontal outputs of second level
signal m3 : STD_LOGIC_VECTOR (5 downto 0); --horizontal outputs of third level
```



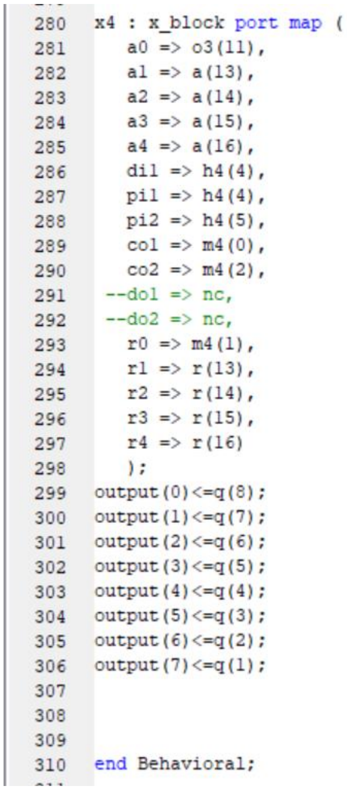
```vhdl
signal m4 : STD_LOGIC_VECTOR (8 downto 0);

signal r : STD_LOGIC_VECTOR (16 downto 0);
signal a : STD_LOGIC_VECTOR (16 downto 1);
signal q :std_logic_vector(8 downto 1);

begin

a(1)<= input(15);
a(2)<= input(14);
a(3)<= input(13);
a(4)<= input(12);
a(5)<= input(11);
a(6)<= input(10);
a(7)<= input(9);
a(8)<= input(8);
a(9)<= input(7);
a(10)<= input(6);
a(11)<= input(5);
a(12)<= input(4);
a(13)<= input(3);
a(14)<= input(2);
a(15)<= input(1);
a(16)<= input(0);
```



```
--fourth level

y4 : y_block port map (
             di1 => o3(0),
             di2 => o3(1),
             a11 => o3(2),
             a12 => o3(4),
             pi1 => q(6),
             pi2 => q(7),
             ci1 => m4(6),
             ci2 => m4(8),
             a22 => m4(7),
             co1 => q(7),
             co2 => q(8),
           --s11 => nc,
             s22 => R(8),
             s21 => R(7),
           --do2 => nc,
           --do1 => nc,
             po2 => h4(1),
             po1 => h4(0)
             );

y5 : y_block port map (
             di1 => o3(3),
             di2 => o3(5),
             a11 => o3(6),
             a12 => o3(8),
             pi1 => h4(0),
             pi2 => h4(1),
             ci1 => m4(3),
             ci2 => m4(5),
             a22 => m4(4),
```



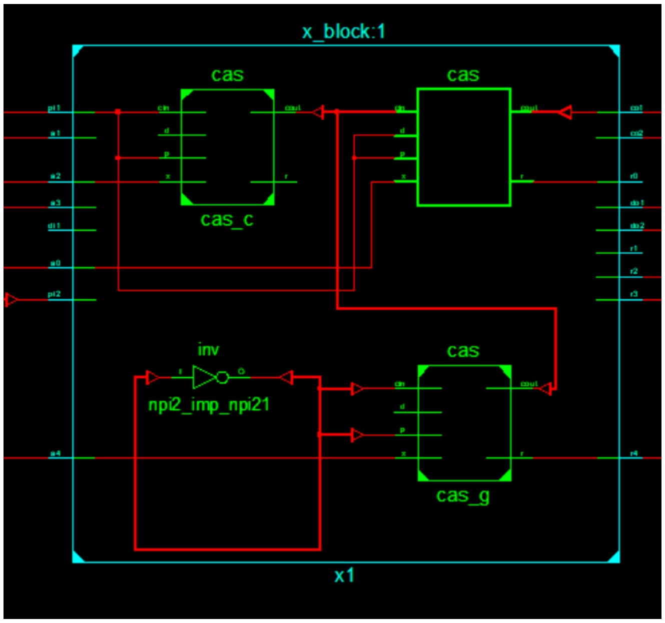
```
             co1 => m4(6),
             co2 => m4(8),
             s11 => m4(7),
             s22 => r(10),
             s21 => r(9),
            --do2 => nc,
            --do1 => nc,
             po2 => h4(3),
             po1 => h4(2)
             );
y6 : y_block port map (
             di1 => o3(7),
             di2 => o3(9),
             a11 => o3(10),
             a12 => o3(11),
             pi1 => h4(2),
             pi2 => h4(3),
             ci1 => m4(0),
             ci2 => m4(2),
             a22 => m4(1),
             co1 => m4(3),
             co2 => m4(5),
             s11 => m4(4),
             s22 => r(12),
             s21 => r(11),
           --do2 => nc,
           --do1 => nc,
             po2 => h4(5),
             po1 => h4(4)
             );

```

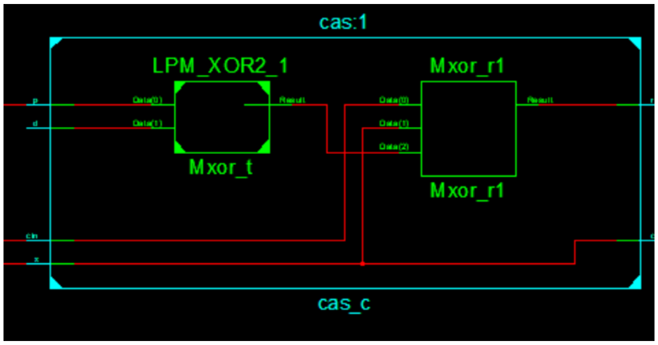


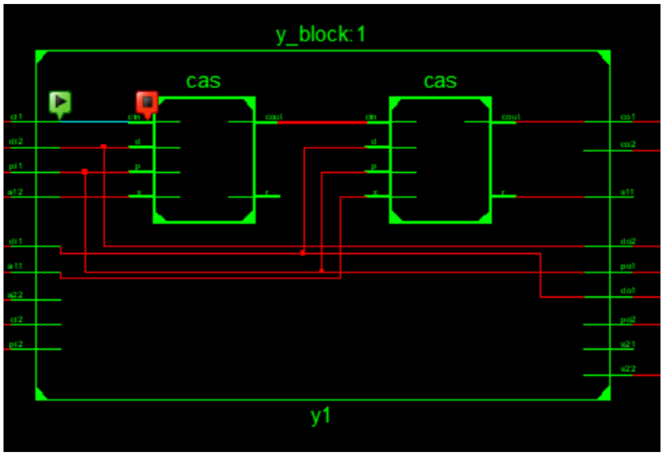
```
x4 : x_block port map (
    a0 => o3(11),
    a1 => a(13),
    a2 => a(14),
    a3 => a(15),
    a4 => a(16),
    di1 => h4(4),
    pi1 => h4(4),
    pi2 => h4(5),
    co1 => m4(0),
    co2 => m4(2),
  --do1 => nc,
  --do2 => nc,
    r0 => m4(1),
    r1 => r(13),
    r2 => r(14),
    r3 => r(15),
    r4 => r(16)
    );
output(0)<=q(8);
output(1)<=q(7);
output(2)<=q(6);
output(3)<=q(5);
output(4)<=q(4);
output(5)<=q(3);
output(6)<=q(2);
output(7)<=q(1);



end Behavioral;
```

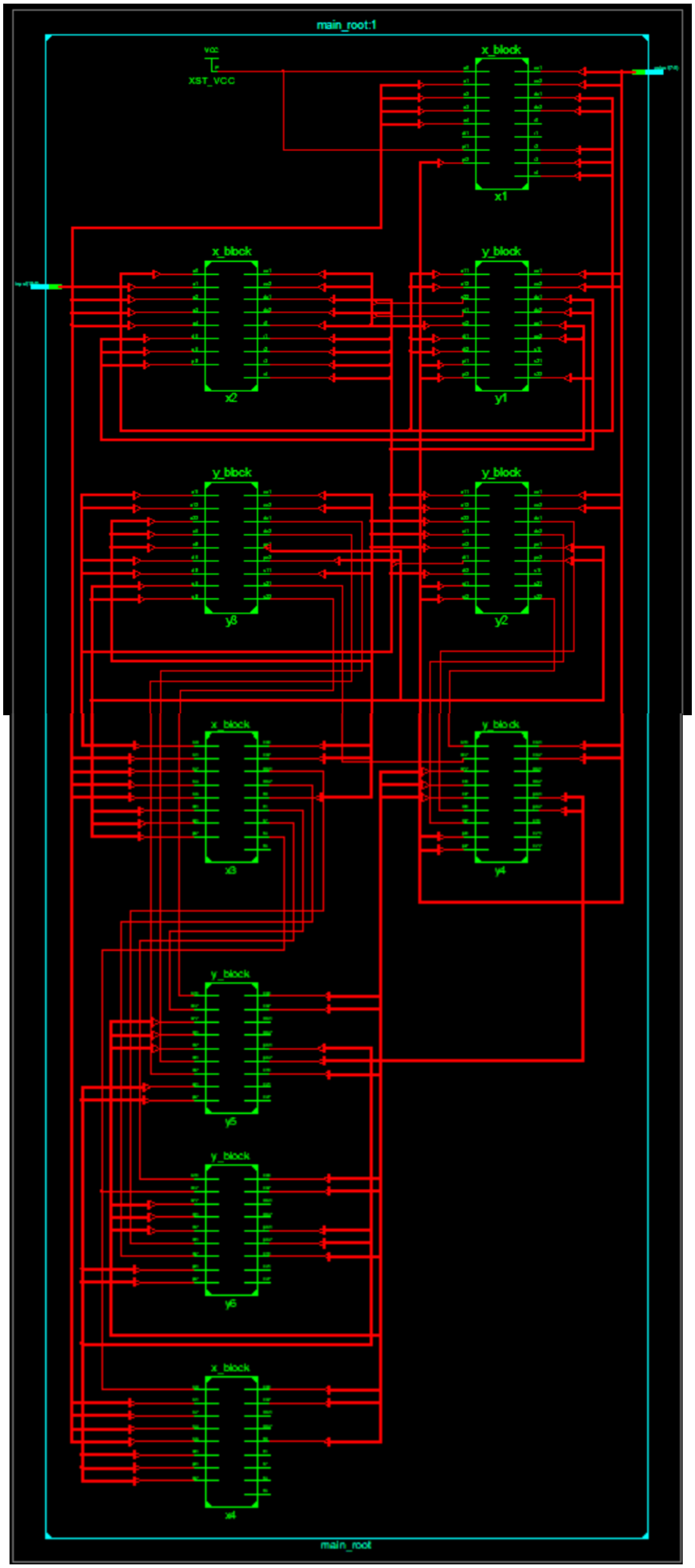
آر تی ال شماتیک:

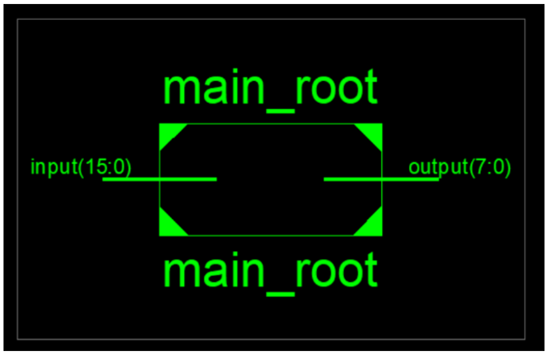
شماتیک بلو ک cas و x و y داخل مدار کلی:



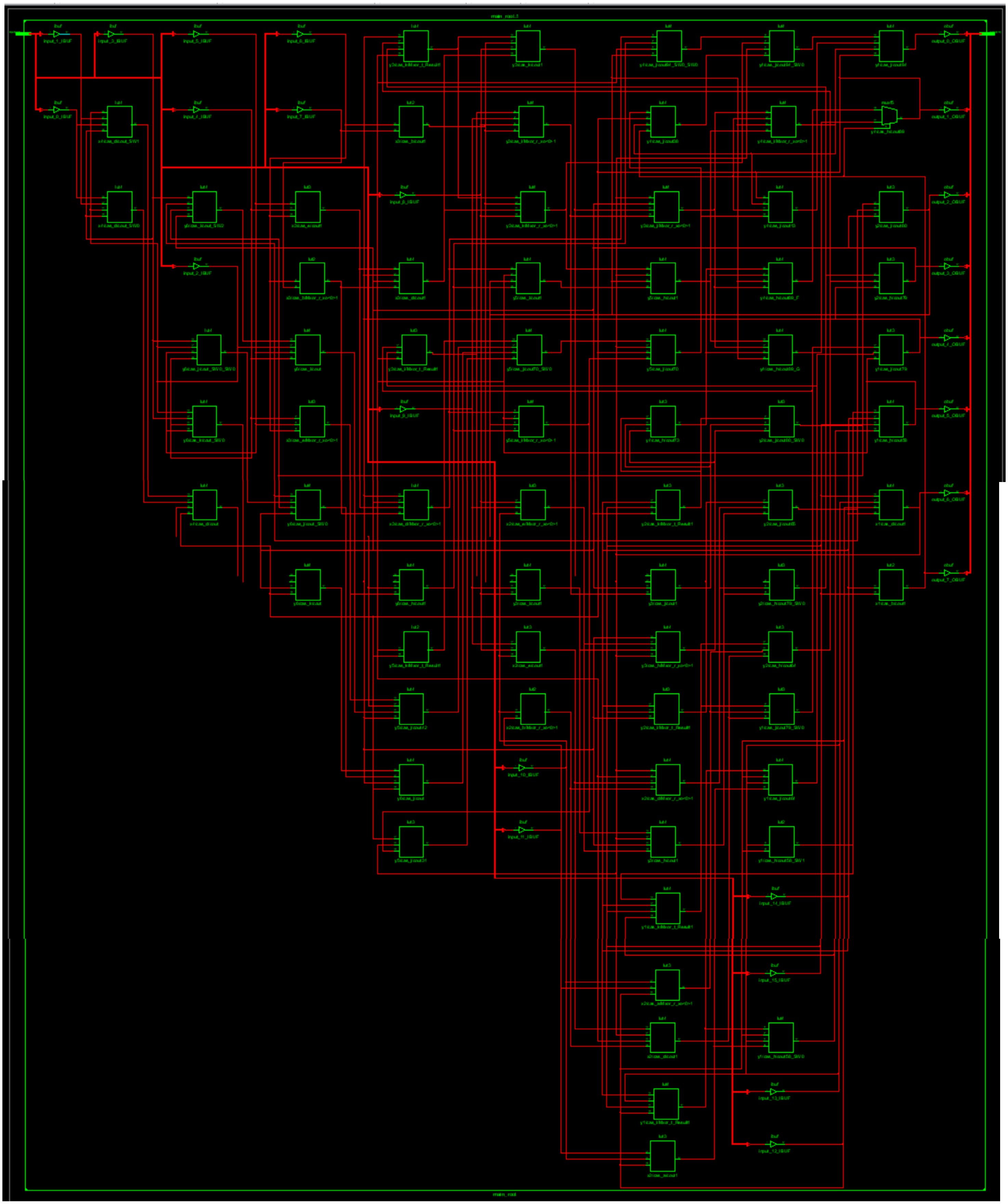




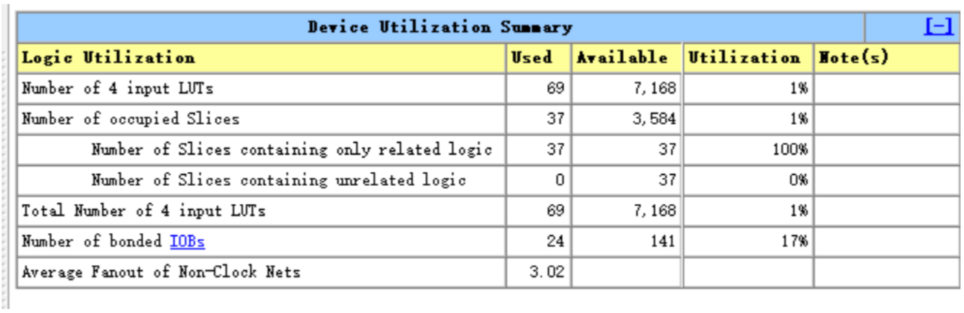

main_root:1
VCC
XST_VCC
x_block
x1
x_block
x2
y_block
y1
y_block
y3
y_block
y2
x_block
x3
y_block
y4
y_block
y5
y_block
y6
x_block
x4
main_root


main_root
input(15:0)
output(7:0)
main_root

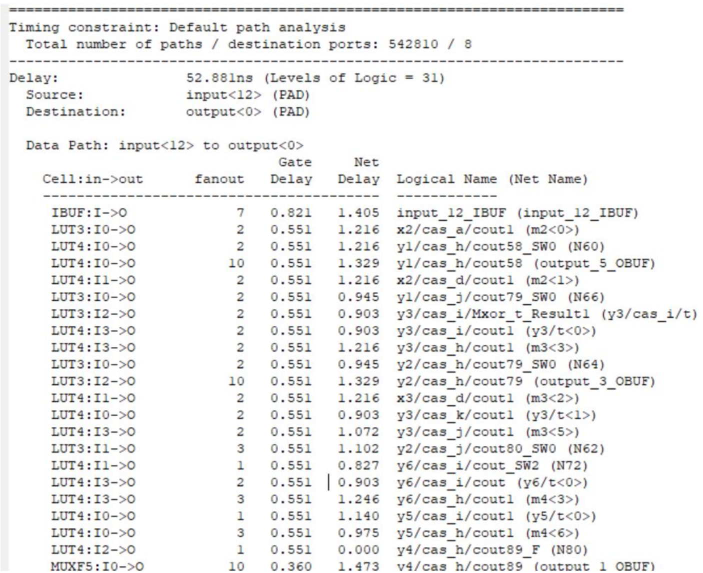
تکنولوژی شماتیک:



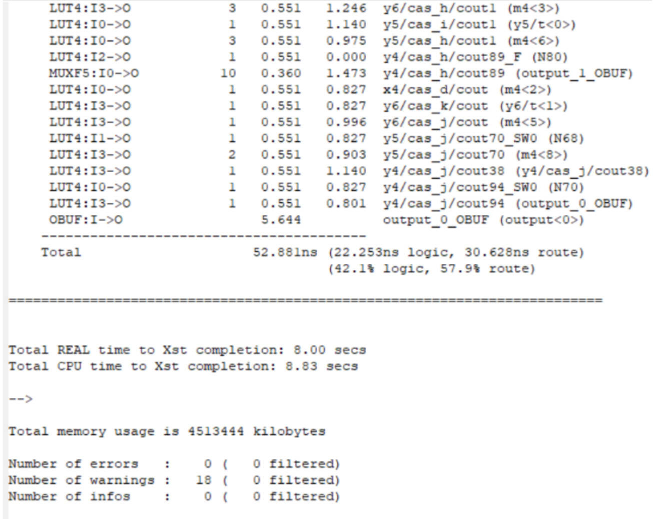
سطوح مصرف:



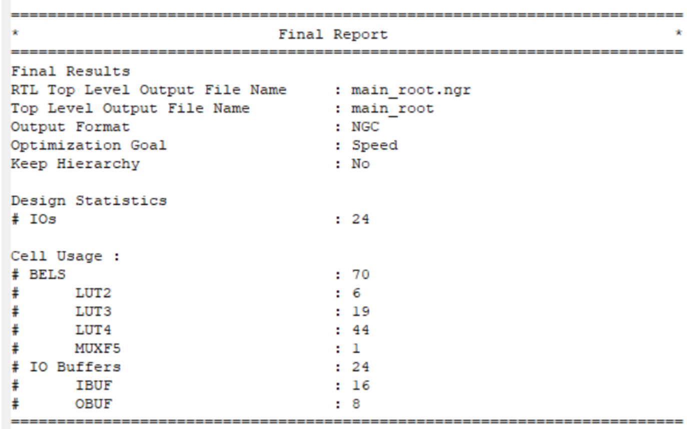
Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	69	7,168	1%	
Number of occupied Slices	37	3,584	1%	
Number of Slices containing only related logic	37	37	100%	
Number of Slices containing unrelated logic	0	37	0%	
Total Number of 4 input LUTs	69	7,168	1%	
Number of bonded IOBs	24	141	17%	
Average Fanout of Non-Clock Nets	3.02			



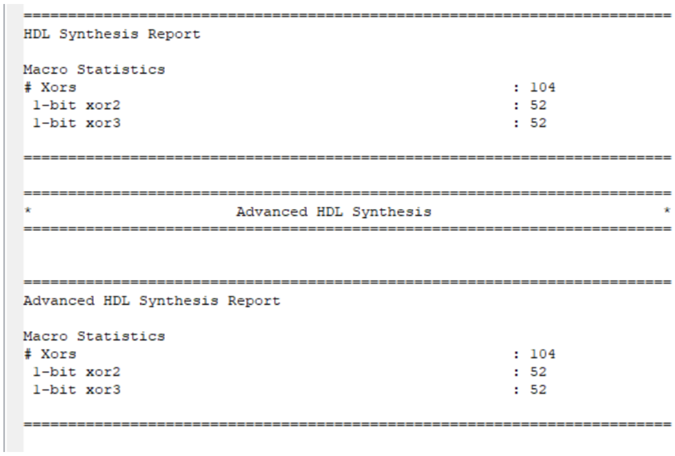
```
=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 542810 / 8
-------------------------------------------------------------------------
Delay:               52.881ns (Levels of Logic = 31)
  Source:            input<12> (PAD)
  Destination:       output<0> (PAD)

  Data Path: input<12> to output<0>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             7   0.821   1.405  input_12_IBUF (input_12_IBUF)
     LUT3:I0->O            2   0.551   1.216  x2/cas_a/cout1 (m2<0>)
     LUT4:I0->O            2   0.551   1.216  y1/cas_h/cout58_SW0 (N60)
     LUT4:I0->O           10   0.551   1.329  y1/cas_h/cout58 (output_5_OBUF)
     LUT4:I1->O            2   0.551   1.216  x2/cas_d/cout1 (m2<1>)
     LUT3:I0->O            2   0.551   0.945  y1/cas_j/cout79_SW0 (N66)
     LUT3:I2->O            2   0.551   0.903  y3/cas_i/Mxor_t_Result1 (y3/cas_i/t)
     LUT4:I3->O            2   0.551   0.903  y3/cas_i/cout1 (y3/t<0>)
     LUT4:I3->O            2   0.551   1.216  y3/cas_h/cout1 (m3<3>)
     LUT3:I0->O            2   0.551   0.945  y2/cas_h/cout79_SW0 (N64)
     LUT3:I2->O           10   0.551   1.329  y2/cas_h/cout79 (output_3_OBUF)
     LUT4:I1->O            2   0.551   1.216  x3/cas_d/cout1 (m3<2>)
     LUT4:I0->O            2   0.551   0.903  y3/cas_k/cout1 (y3/t<1>)
     LUT4:I3->O            2   0.551   1.072  y3/cas_j/cout1 (m3<5>)
     LUT3:I1->O            3   0.551   1.102  y2/cas_j/cout80_SW0 (N62)
     LUT4:I1->O            1   0.551   0.827  y6/cas_i/cout_SW2 (N72)
     LUT4:I3->O            2   0.551 | 0.903  y6/cas_i/cout (y6/t<0>)
     LUT4:I3->O            3   0.551   1.246  y6/cas_h/cout1 (m4<3>)
     LUT4:I0->O            1   0.551   1.140  y5/cas_i/cout1 (y5/t<0>)
     LUT4:I0->O            3   0.551   0.975  y5/cas_h/cout1 (m4<6>)
     LUT4:I2->O            1   0.551   0.000  y4/cas_h/cout89_F (N80)
     MUXF5:I0->O          10   0.360   1.473  y4/cas_h/cout89 (output_1_OBUF)
```



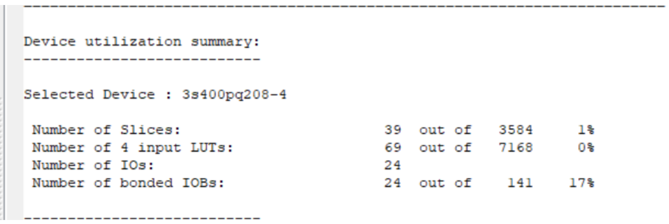
```
     LUT4:I3->O            3   0.551   1.246  y6/cas_h/cout1 (m4<3>)
     LUT4:I0->O            1   0.551   1.140  y5/cas_i/cout1 (y5/t<0>)
     LUT4:I0->O            3   0.551   0.975  y5/cas_h/cout1 (m4<6>)
     LUT4:I2->O            1   0.551   0.000  y4/cas_h/cout89_F (N80)
     MUXF5:I0->O          10   0.360   1.473  y4/cas_h/cout89 (output_1_OBUF)
     LUT4:I0->O            1   0.551   0.827  x4/cas_d/cout (m4<2>)
     LUT4:I3->O            1   0.551   0.827  y6/cas_k/cout (y6/t<1>)
     LUT4:I3->O            1   0.551   0.996  y6/cas_j/cout (m4<5>)
     LUT4:I1->O            1   0.551   0.827  y5/cas_j/cout70_SW0 (N68)
     LUT4:I3->O            2   0.551   0.903  y5/cas_j/cout70 (m4<8>)
     LUT4:I3->O            1   0.551   1.140  y4/cas_j/cout38 (y4/cas_j/cout38)
     LUT4:I0->O            1   0.551   0.827  y4/cas_j/cout94_SW0 (N70)
     LUT4:I3->O            1   0.551   0.801  y4/cas_j/cout94 (output_0_OBUF)
     OBUF:I->O                     5.644          output_0_OBUF (output<0>)
    ----------------------------------------
    Total                     52.881ns (22.253ns logic, 30.628ns route)
                                       (42.1% logic, 57.9% route)

=========================================================================


Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 8.83 secs

-->

Total memory usage is 4513444 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   18 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : main_root.ngr
Top Level Output File Name         : main_root
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 24

Cell Usage :
# BELS                             : 70
#      LUT2                        : 6
#      LUT3                        : 19
#      LUT4                        : 44
#      MUXF5                       : 1
# IO Buffers                       : 24
#      IBUF                        : 16
#      OBUF                        : 8
=========================================================================
```

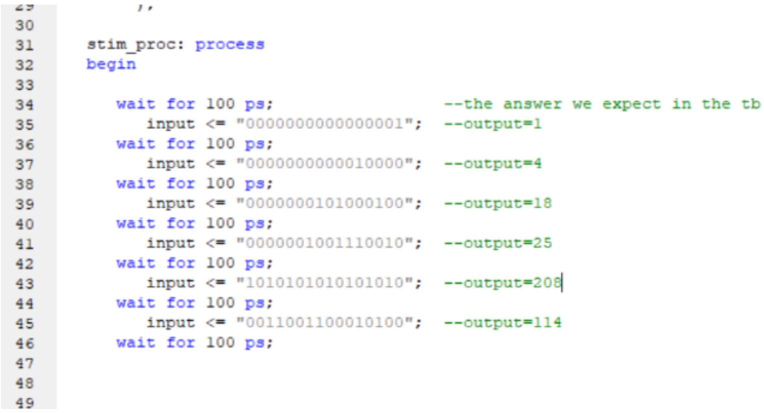


```
=========================================================================
HDL Synthesis Report

Macro Statistics
# Xors                                                 : 104
 1-bit xor2                                            : 52
 1-bit xor3                                            : 52

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Xors                                                 : 104
 1-bit xor2                                            : 52
 1-bit xor3                                            : 52

=========================================================================
```

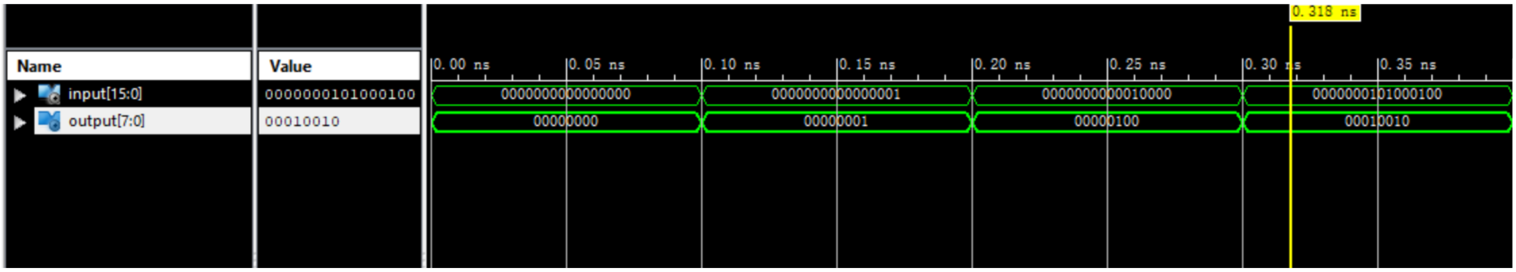


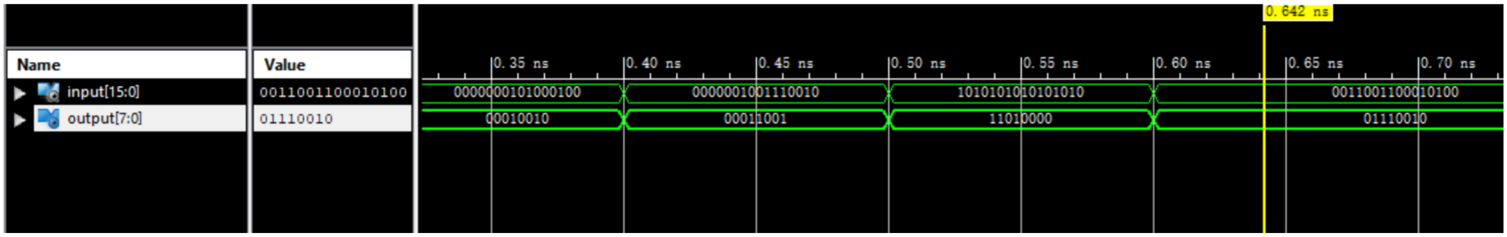
```
-------------------------------------------------------------------------

Device utilization summary:
---------------------------

Selected Device : 3s400pq208-4

 Number of Slices:                      39  out of   3584     1%
 Number of 4 input LUTs:                69  out of   7168     0%
 Number of IOs:                         24
 Number of bonded IOBs:                 24  out of    141    17%

---------------------------
```

کد تست بنچ و شبیه سازی:



```
      );

   stim_proc: process
   begin

      wait for 100 ps;                  --the answer we expect in the tb
         input <= "0000000000000001";   --output=1
      wait for 100 ps;
         input <= "0000000000010000";   --output=4
      wait for 100 ps;
         input <= "0000000101000100";   --output=18
      wait for 100 ps;
         input <= "0000001001110010";   --output=25
      wait for 100 ps;
         input <= "1010101010101010";   --output=208
      wait for 100 ps;
         input <= "0011001100010100";   --output=114
      wait for 100 ps;
```


0.318 ns
Name
Value
input[15:0]
0000000101000100
output[7:0]
00010010
0.00 ns
0.05 ns
0.10 ns
0.15 ns
0.20 ns
0.25 ns
0.30 ns
0.35 ns
0000000000000000
0000000000000001
0000000000010000
0000000101000100
00000000
00000001
00000100
00010010


0.642 ns
Name
Value
input[15:0]
0011001100010100
output[7:0]
01110010
0.35 ns
0.40 ns
0.45 ns
0.50 ns
0.55 ns
0.60 ns
0.65 ns
0.70 ns
0000000101000100
0000001001110010
1010101010101010
0011001100010100
00010010
00011001
11010000
01110010