# EE671: Assignment 1

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Roll No: 210010010

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## 1 Question 1

For this question, I first ran the sample code with the pre-specified values and noted the rise and fall times. The last two digits of my roll no are 10 and hence I had to achieve a rise and fall time of **220 ps**. I changed the width of the PMOS transistor and achieved the rise time specification. This was followed by the subsequent tuning of the width of the NMOS transistor.
The width of the PMOS after designing is **1.865** $\mu$**m** and the width of the NMOS transistor is **0.6465** $\mu$**m**. The lengths of both the transistors have been kept constant at **0.18** $\mu$**m**.
This is the code that I have written:

```
Question 1
.include models-180nm
*Name: Anoushka Dey
*Roll 210010010 :  nn = 10

*Rise and Fall times to achieve: 200+2*10=220 ps

*Parameters
*geometry parameters
.param pw = 1.865U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}

.param nw = 0.6465U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
```

```
.param nps = {2*(nw + 2*nl)}

* Minimum Inverter
.subckt inv supply Inp Output
*  This subcircuit defines a CMOS inverter with equal n and p widths
MP1 Output Inp Supply Supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN1 Output Inp 0      0      cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends

vdd supply 0 dc 1.8

*  Device under test
x3  supply Ck dutout inv

* Load Capacitor
C3 dutout 0 0.05pF


*TRANSIENT ANALYSIS with pulse inputs
VCk  Ck   0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.tran 1pS 35nS 0nS

.control
run
plot 4.0+V(Ck) V(dutout)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62 RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18 FALL=2
.endc
.end
```

# 2 Question 2

Here we had to plot the static characteristics graph and calculate the noise margins by setting

$$\frac{\partial V_o}{\partial V_{in}} = -1 \tag{1}$$

.
From this I got the $V_{IL}, V_{IH}, V_{OH}$ and $V_{OL}$ values and calculated the noise margins.
Low noise margin= $V_{IL} - V_{OL}$= 0.602 V
High noise margin=$V_{OH} - V_{IH}$= 0.714 V

```
Question 2
.include models-180nm
*Name: Anoushka Dey
*Roll 210010010 :  nn = 10

*Rise and Fall times to achieve: 200+2*10=220 ps

*Parameters
*geometry parameters
.param pw = 1.865U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}

.param nw = 0.6465U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
.param nps = {2*(nw + 2*nl)}

* Minimum Inverter
.subckt inv supply Inp Output
*  This subcircuit defines a CMOS inverter with equal n and p widths
MP1 Output Inp Supply Supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN1 Output Inp 0      0      cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends

vdd supply 0 dc 1.8

*  Device under test
x3  supply Ck dutout inv

* Load Capacitor
C3 dutout 0 0.05pF


*TRANSIENT ANALYSIS with pulse inputs
VCk  Ck   0 DC
.dc VCk 0 1.8 0.001
```

```
.control
run
plot V(dutout) vs V(Ck)

let dVout = deriv(V(dutout))
meas dc VIL find V(Ck) when dVout=-1
meas dc VIH find V(Ck) when dVout = -1 rise=last
meas dc VOH find V(dutout) when V(ck) = VIL
meas dc VOL find V(dutout) when V(ck) = VIH

let hnoisemarg= VOH - VIH
let lonoisemarg = VIL - VOL
*High noise margin= 0.714V
*Low noise margin= 0.602V

print hnoisemarg
print lonoisemarg
.endc
.end
```

# 3 Question 3

In this question, we had to design the logic $\overline{A.(B+C)}$. This involved designing the system such that the B and C input NMOSes were in parallel with each other and in series with NMOS A and PMOS B and PMOS C were in series with each other and in parallel with PMOS A. After designing the circuit, I provided the appropriate inputs as specified in the question and noted down the rise and fall times.

Part a:
Rise time=510.73ps
Fall time=408.87ps
Part b:
Rise time=510.74ps
Fall time=424.45ps
Part c:
Rise time=274.43ps
Fall time=408.81ps

```
Question 3
.include models-180nm
*Name: Anoushka Dey
*Roll 210010010 :  nn = 10
```

```
*Rise and Fall times to achieve: 200+2*10=220 ps

*Parameters
*geometry parameters
.param pw = 1.865U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}

.param nw = 0.6465U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
.param nps = {2*(nw + 2*nl)}

* Minimum Inverter
.subckt inv supply Inp Output
*  This subcircuit defines a CMOS inverter with equal n and p widths
MP1 Output Inp Supply Supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN1 Output Inp 0      0      cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends

.subckt cmoslogic supply A B C Output
MP1 Output A supply supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MP2 node1 B supply supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MP3 Output C node1 node1 cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}

MN1 Output A node2 node2 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN2 node2 B 0 0 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN3 node2 C 0 0 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends
vdd supply 0 dc 1.8
* device under test
x3 supply A B C dutout cmoslogic
* load capacitor
```

```
C3 dutout 0 0.05pF


*Part a
*Rise time=510.73ps
*Fall time=408.87ps
*VC C 0 DC 0 PULSE(0.18 1.62 0nS 20pS 20pS 4nS 8nS)
*VA A 0 DC 1.62
*VB B 0 DC 0.18

*Part b
*Rise time=510.74ps
*Fall time=424.45ps
*VB B 0 DC 0 PULSE(0.18 1.62 0nS 20pS 20pS 4nS 8nS)
*VA A 0 DC 1.62
*VC C 0 DC 0.18

*Part c
*Rise time=274.43ps
*Fall time=408.81ps
VA A 0 DC 0 PULSE(0.18 1.62 0nS 20pS 20pS 4nS 8nS)
VC C 0 DC 1.62
VB B 0 DC 0.18


*transient analysis
.tran 1pS 35nS 0nS
.control
run
plot 4.0+V(A) 8.0+V(B) 12.0+V(C) V(dutout)

* output 10% - 80% rise and fall time
meas tran outrise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62 RISE=2
meas tran outfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18 FALL=2
.endc
.end
```