
```
close all; clear; clc;
```

Q1.5

```
t = 0:0.001:2*pi;
V = 3.3*sin(t)+1.65;
minV = min(V);
maxV = max(V);

% Convert to bins
bins = voltage2bin(V,minV,maxV,12);

figure()
hold on;
plot(bins,'linewidth',1)
ylabel('Bin Number');
yyaxis right;
plot(V,'r--','linewidth',0.5);
ax = gca;
ax.YAxis(1).Color = 'b';
ax.YAxis(2).Color = 'r';

legend('Bin Number','Actual Voltage');
grid minor;
xlabel('Array Number');
ylabel('Voltage (V)');
title('Sinusoid Voltage to Bin Conversion')

function [bins] = voltage2bin(v,min_voltage,max_voltage,bits)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% This function determines which bin number in decimal and binary a voltage
% signal would be placed in by an A/D converter. This function takes in
% voltages and the bin for each one so bins can be plotted against voltage

% Inputs:
% v: A vector of voltage values to convert to bins
% min_voltage: Minimum voltage value taht will be received by the ADC
% max_voltage: Maximum voltage that will be received by the ADC
% bits (usually 1-12): Number of bits used to resolve voltage

% Output:
% bins: a vector of the bin number corresponding to each value in v
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

n = length(v);

% A check that all values are within the desired range since equipment can
% be damaged outside of these ranges.
for i = 1:n
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        if v(i)>max_voltage&&v(i)<min_voltage
            disp("Error- Voltage is outside min and max range. ");
        end
    end

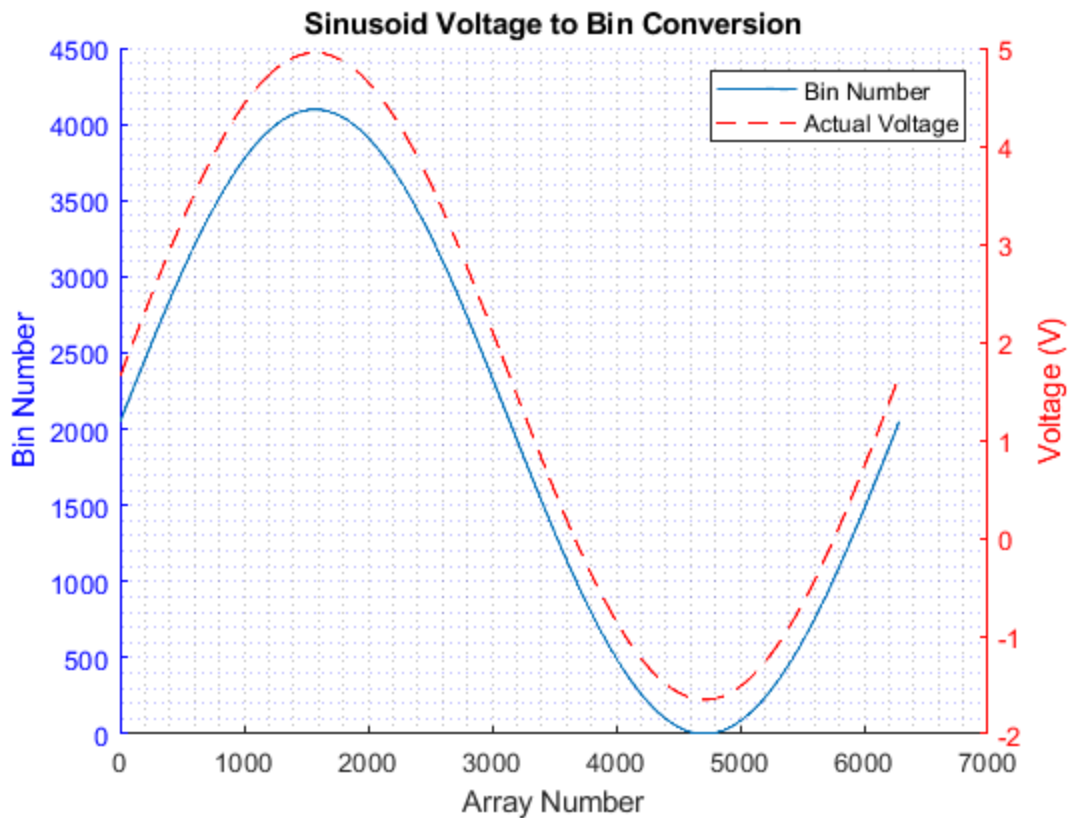
    % Least Significant Bit
    LSB = (max_voltage-min_voltage)/(2^bits);

    %Calculating the values of all the different bins in V
    bin_values = min_voltage:LSB:max_voltage;

    bins = zeros(n,1);
    % Determining which bin each voltage value falls in based on it's magnitude
    for i = 1:n
        for j = 1:length(bin_values)-1
            if (v(i)<bin_values(j+1)&&v(i)>=bin_values(j))
                bins(i) = j;
            elseif (v(i)>max(bin_values(j)))
                bins(i)=j;
            end
        end
    end
end

end

```



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