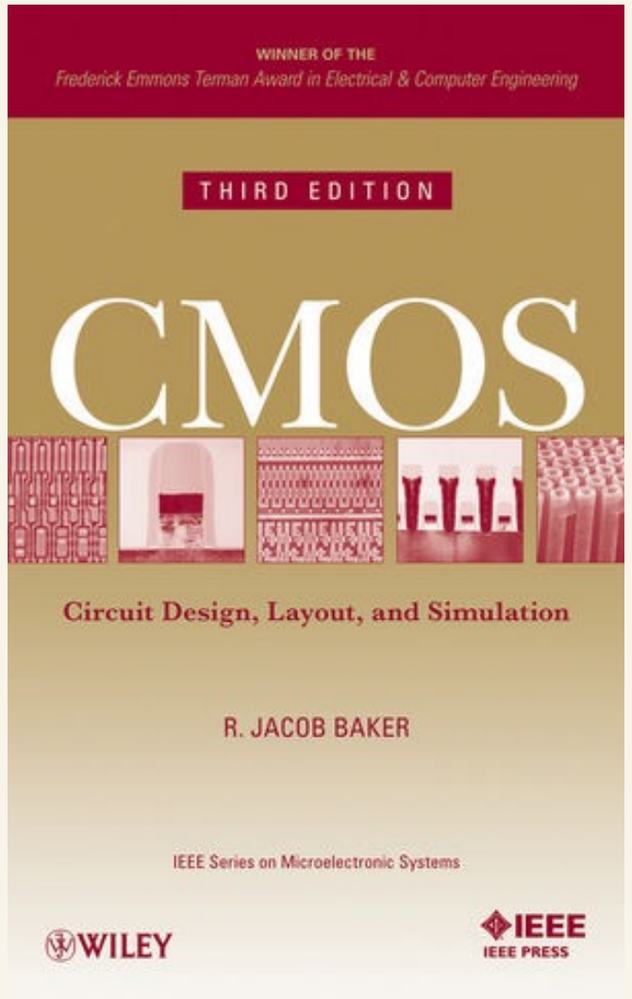
Models for Digital Design

- Miller Capacitance
- The Digital MOSFET Model
- The MOSFET Pass Gate



Chap 10

Miller Capacitance

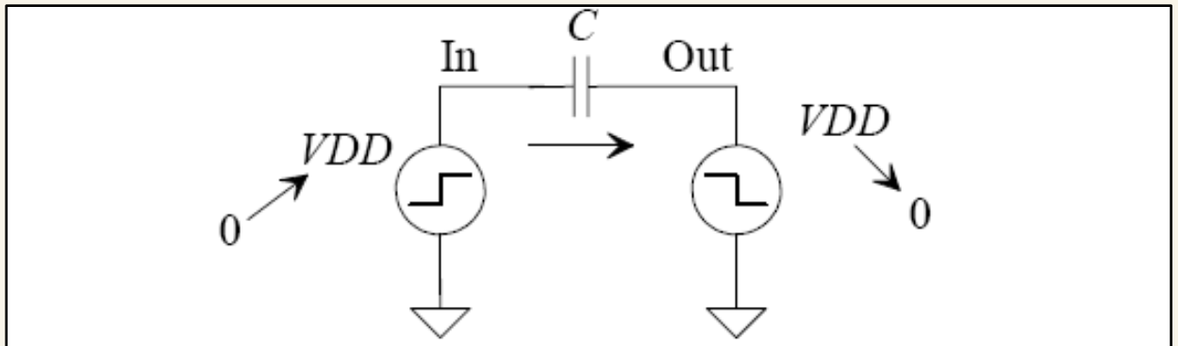
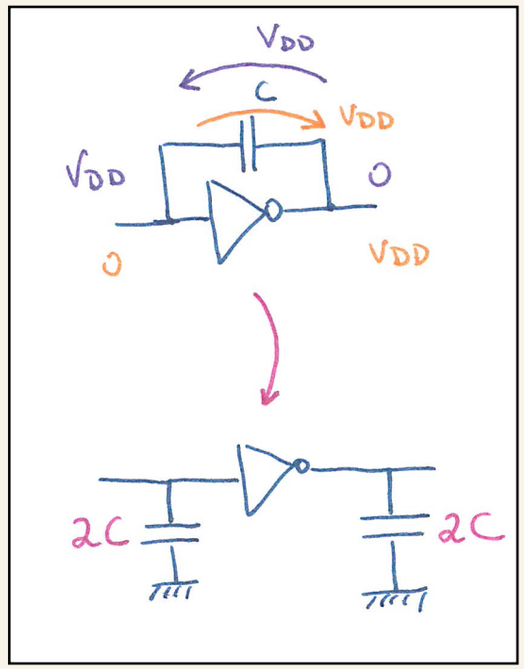


Figure 10.2 Determining the charge through a capacitor.



$$Q_{tot} = Q_{final} - Q_{init} = 2C \cdot VDD$$

(a) Input circuit (b) Output circuit

Figure 10.3 Splitting the capacitor in Fig. 10.2 up into two equivalent capacitors for developing a model.

The Digital MOSFET Model

- Effective Switching Resistance

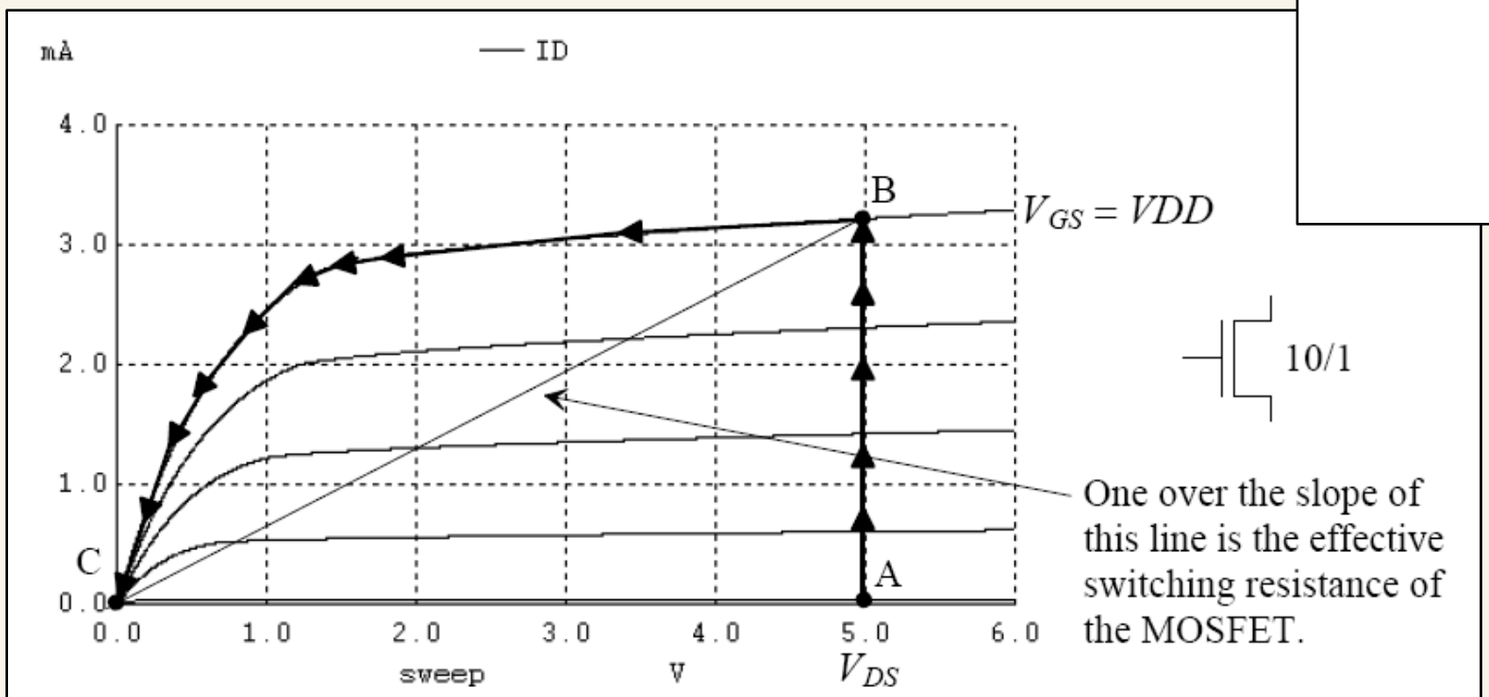


Figure 10.5 IV plot for a 10/1 NMOS device to estimate average switching resistance.

$$R_n = R'_n \cdot \frac{L}{W} = \frac{VDD}{I_{D,sat}} = \frac{5}{3.3\ mA} \rightarrow R'_n \approx 15\ k\Omega$$

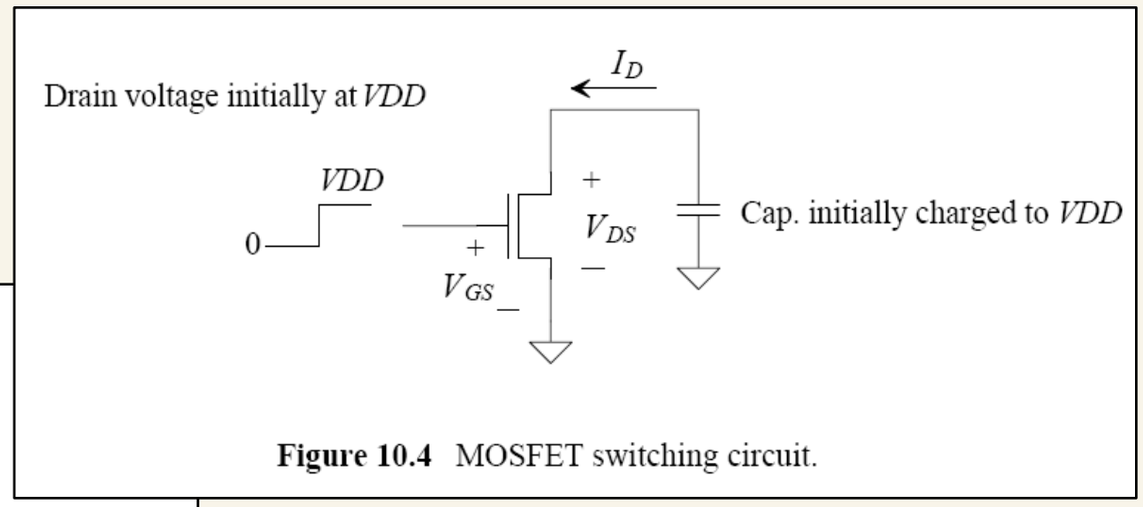


Figure 10.4 MOSFET switching circuit.

$$R_n = \frac{VDD}{\frac{KP_n}{2}\frac{W}{L} \cdot (VDD - V_{THN})^2} = R'_n \cdot \frac{L}{W}$$

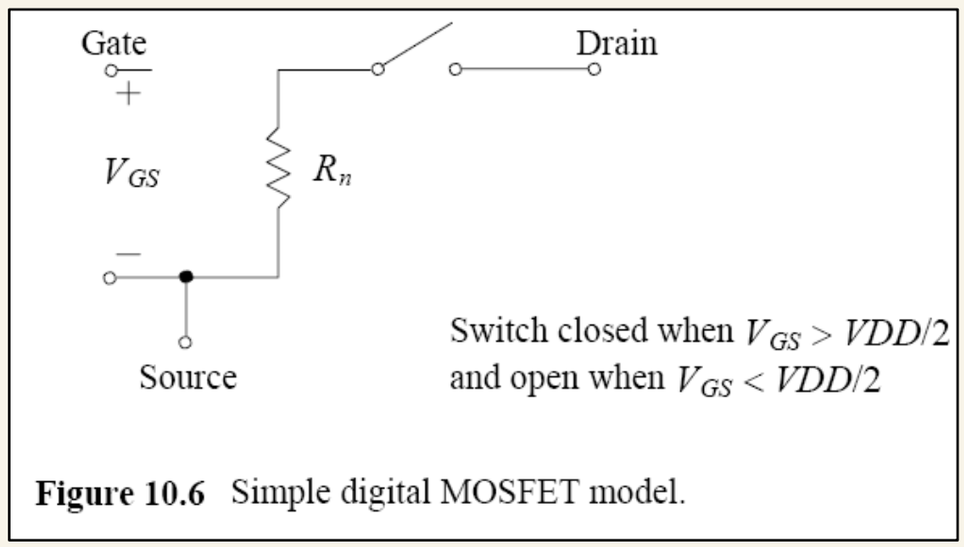


Figure 10.6 Simple digital MOSFET model.

- Capacitive Effects

» Depletion capacitances are neglected when doing hand calculations

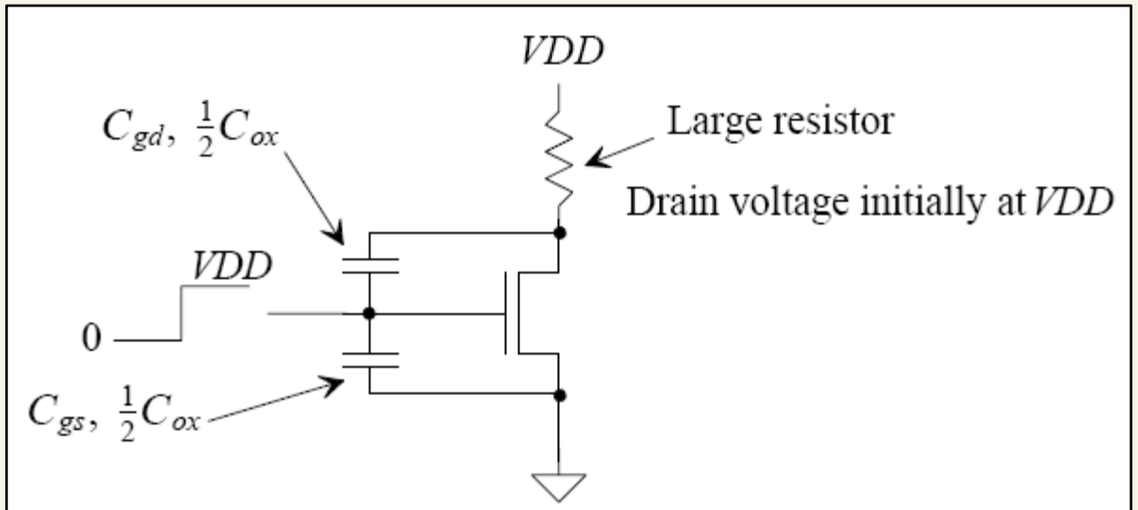
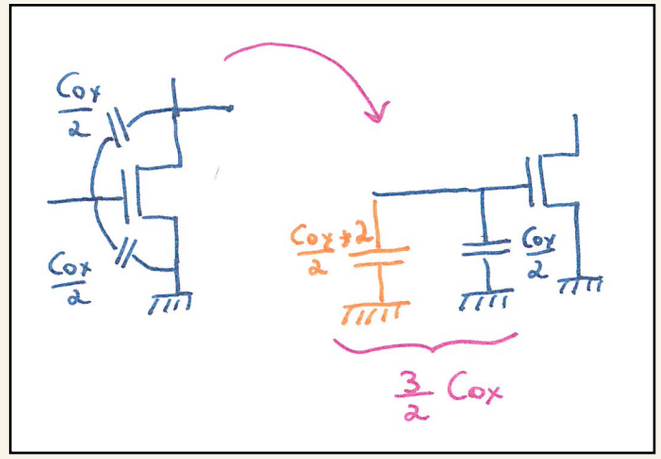


Figure 10.7 MOSFET switching circuit with capacitances.



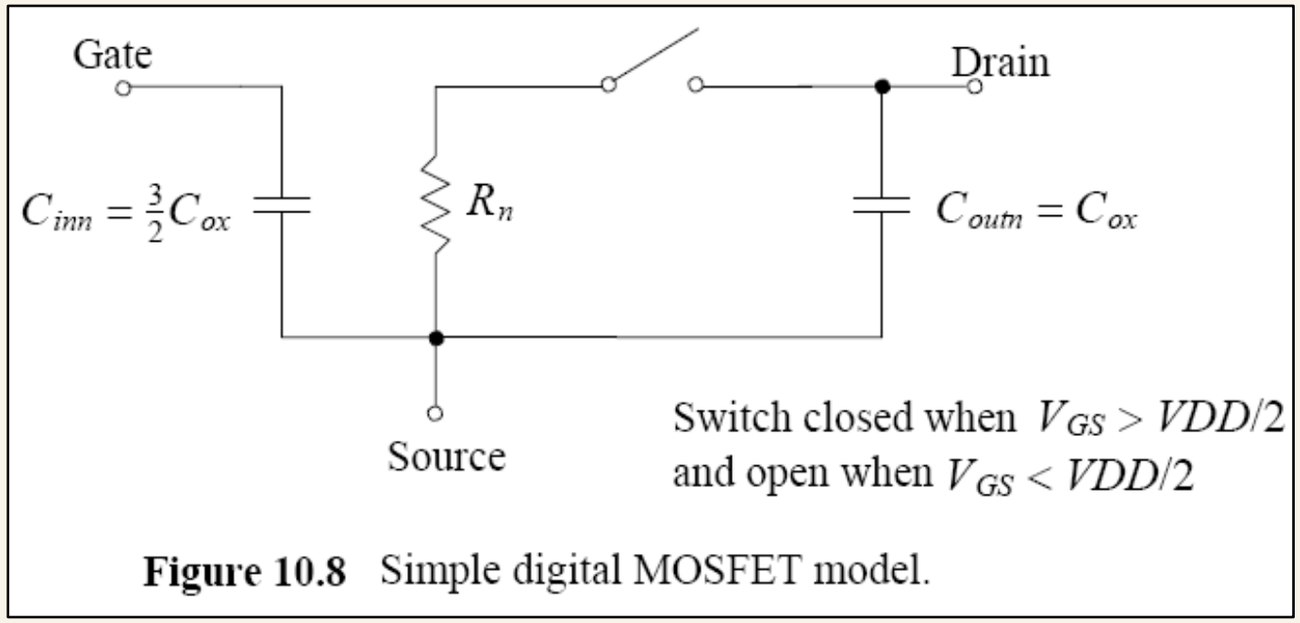


Figure 10.8 Simple digital MOSFET model.

- Process Characteristic Time Constant
  - Long-Channel Process

$$\tau_n = R_n C_{ox} = \frac{2L \cdot VDD}{KP_n W(VDD - V_{THN})^2} \cdot C'_{ox} WL \cdot (scale)^2 = \frac{2C'_{ox} \cdot VDD \cdot (L \cdot scale)^2}{KP_n \cdot (VDD - V_{THN})^2}$$

  - Short-Channel Process

$$\tau_n = R_n C_{ox} = \frac{2L \cdot VDD}{KP_n W(VDD - V_{THN})^2} \cdot C'_{ox} WL \cdot (scale)^2 = \frac{2C'_{ox} \cdot VDD \cdot (L \cdot scale)^2}{KP_n \cdot (VDD - V_{THN})^2}$$

* Ne dépend pas de W
* $\div L^2$
* $\div \frac{1}{V_{DD}}$ ($V_{DD} \uparrow \tau \downarrow$)

Table 10.1 Digital model parameters used for hand calculations in the long- and short-channel CMOS processes used in this book. Note that the widths, W, and lengths, L, seen in this table are drawn lengths (minimum length is 1 while minimum width is 10).

Technology	R_n	R_p	Scale factor	$C_{ox} = C'_{ox} WL \cdot (scale)^2$
1 μm (long-channel)	$15k\frac{L}{W}$	$45k\frac{L}{W}$	1 μm	$(1.75\,fF) \cdot WL$
50 nm (short-channel)	$\frac{34k}{W}$	$\frac{68k}{W}$	50 nm	$(62.5\,aF) \cdot WL$

- Delay and Transition Times

$$t_{PHL} \approx 0.7 \cdot R_n \cdot C_{tot} \text{ and } t_{PLH} \approx 0.7 \cdot R_p \cdot C_{tot}$$

$$t_{HL} \approx 2.2 \cdot R_n \cdot C_{tot} \text{ and } t_{LH} \approx 2.2 \cdot R_p \cdot C_{tot}$$

Ref. Book p 50

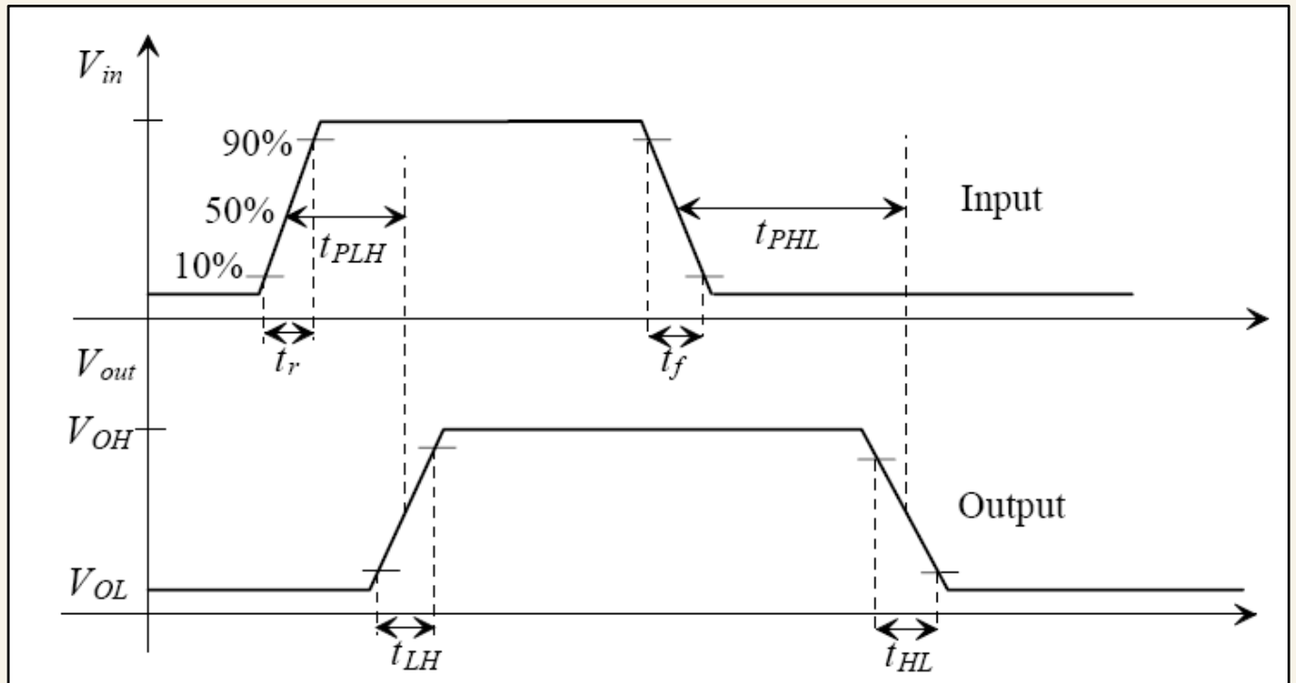


Figure 10.9 Definition of delays and transition times.

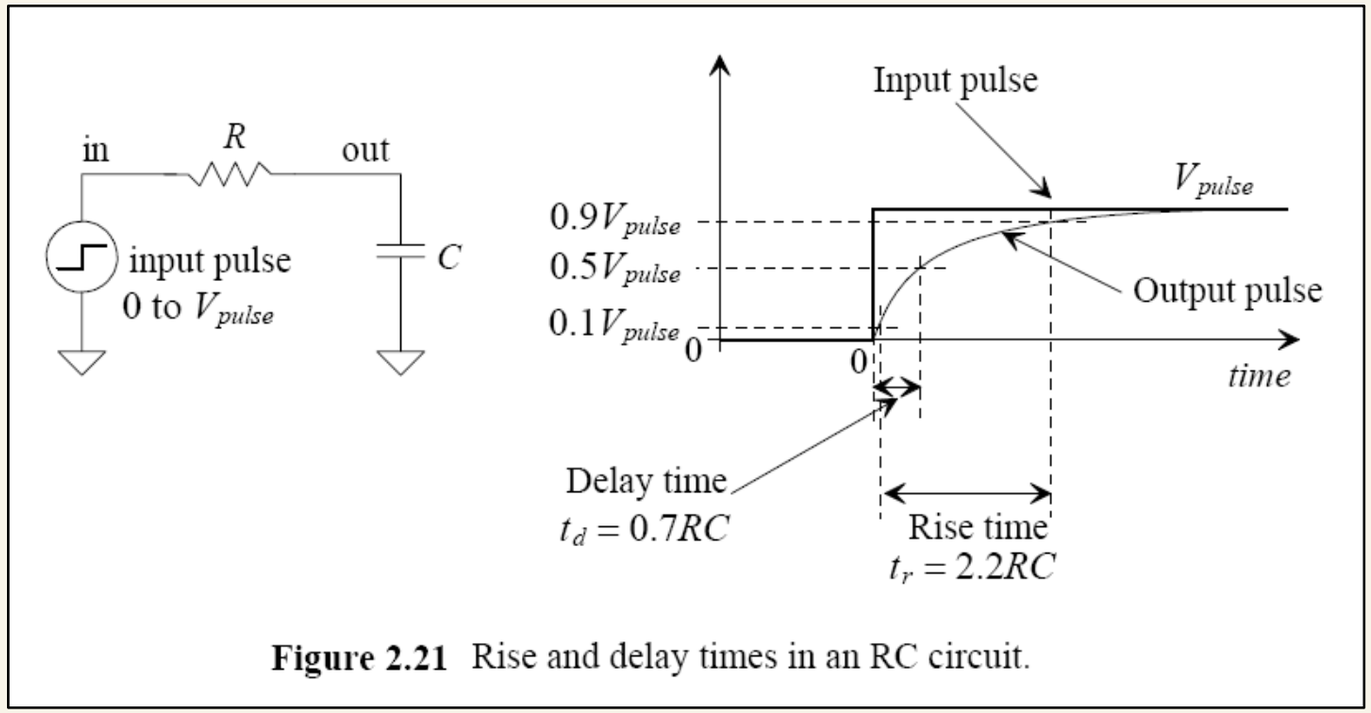
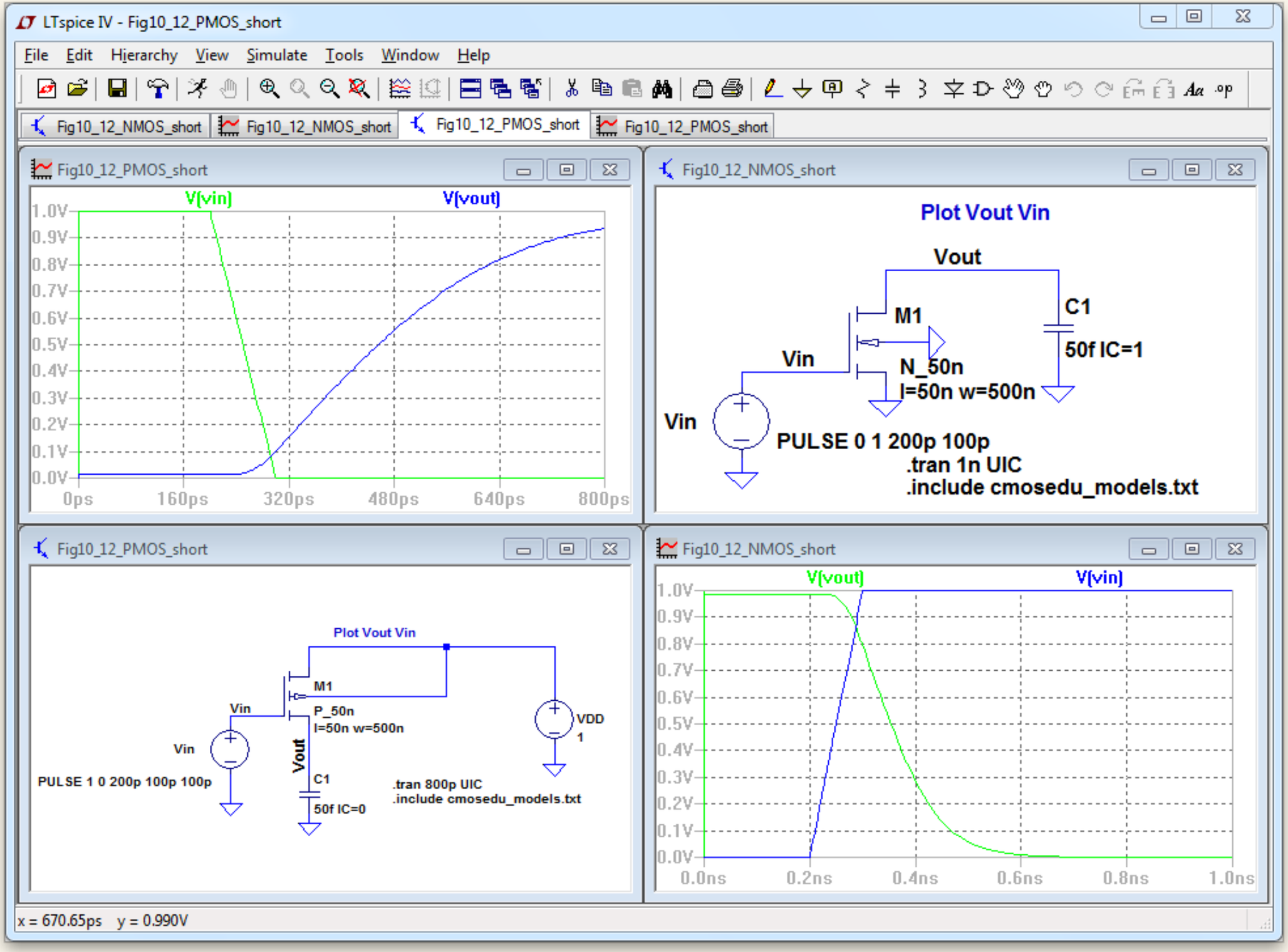


Figure 2.21 Rise and delay times in an RC circuit.

– Example


LTspice IV - Fig10_12_PMOS_short
File Edit Hierarchy View Simulate Tools Window Help
Fig10_12_NMOS_short
Fig10_12_NMOS_short
Fig10_12_PMOS_short
Fig10_12_PMOS_short
Fig10_12_PMOS_short
V(vin)
V(vout)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0ps
160ps
320ps
480ps
640ps
800ps
Fig10_12_NMOS_short
Plot Vout Vin
Vout
M1
C1
50f IC=1
Vin
N_50n
l=50n w=500n
Vin
PULSE 0 1 200p 100p
.tran 1n UIC
.include cmosedu_models.txt
Fig10_12_PMOS_short
Plot Vout Vin
M1
Vin
P_50n
l=50n w=500n
VDD
1
Vin
Vout
C1
PULSE 1 0 200p 100p 100p
.tran 800p UIC
.include cmosedu_models.txt
50f IC=0
Fig10_12_NMOS_short
V(vout)
V(vin)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0.0ns
0.2ns
0.4ns
0.6ns
0.8ns
1.0ns
x = 670.65ps y = 0.990V

- General Digital Design

Table 10.2 Parameters for general digital design using the long-channel (scale factor is 1 μm) or short-channel (scale factor of 50 nm) CMOS process **used in this book**.

Technology	Drawn	Actual size	$R_{n,p}$	$C_{ox,n,p}$
NMOS (long-channel)	10/1	10 μm by 1 μm	1.5k	17.5 *fF*
PMOS (long-channel)	30/1	30 μm by 1 μm	1.5k	52.5 *fF*
NMOS (short-channel)	10/1	0.5 μm by 50 nm	3.4k	625 *aF*
PMOS (short-channel)	20/1	1 μm by 50 nm	3.4k	1.25 *fF*

The MOSFET Pass Gate

- The NMOS Pass Gate

  » An NMOS device is good at passing a "0" and bad at passing a "1"

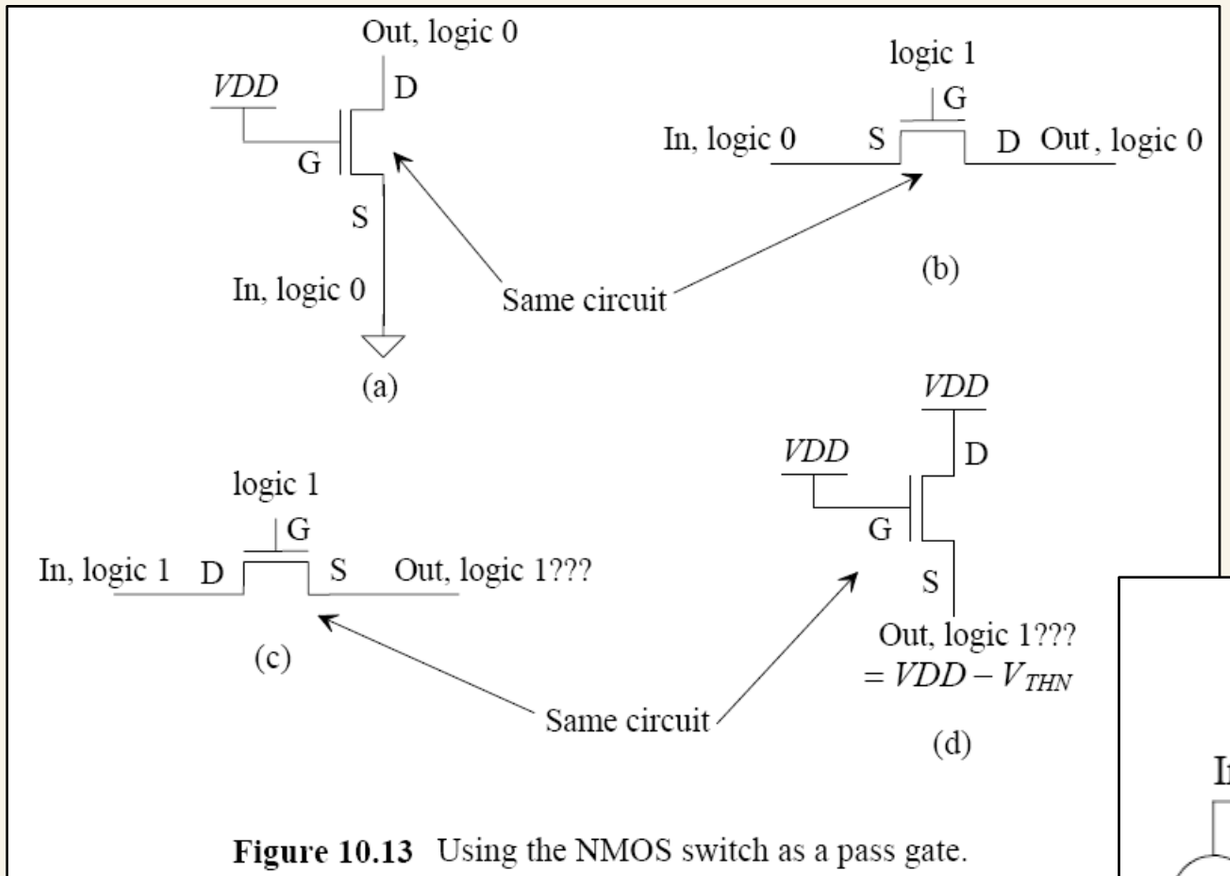


Figure 10.13 Using the NMOS switch as a pass gate.

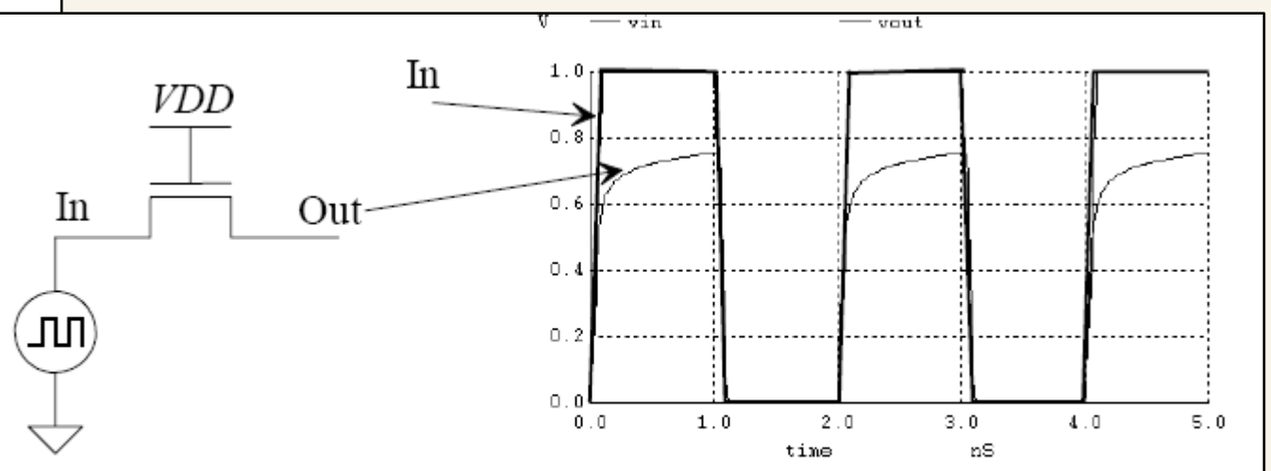


Figure 10.14 The input and output of an NMOS pass gate.

- The PMOS Pass Gate

  » A PMOS device is good at passing a "1" and bad at passing a "0"

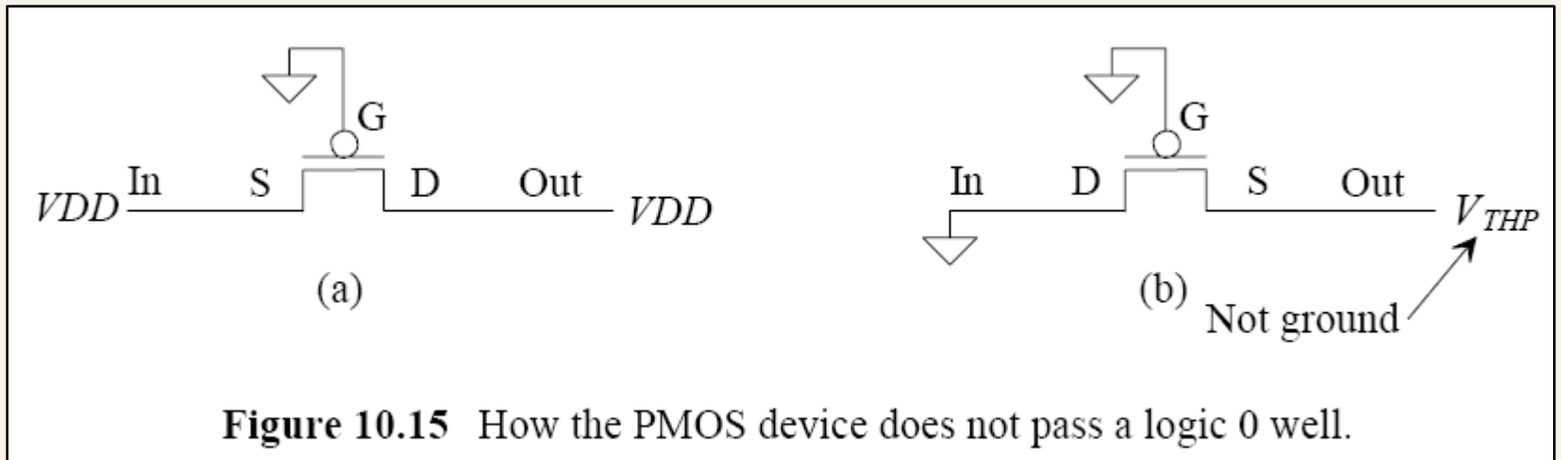


Figure 10.15 How the PMOS device does not pass a logic 0 well.

- Example

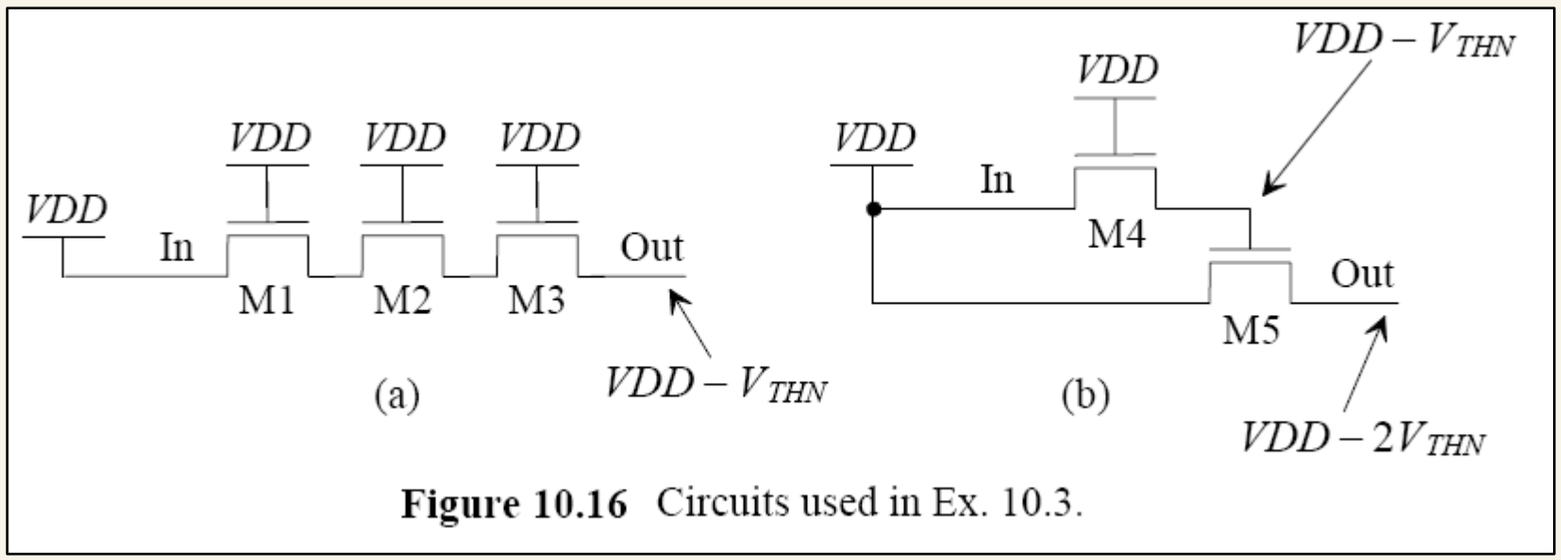
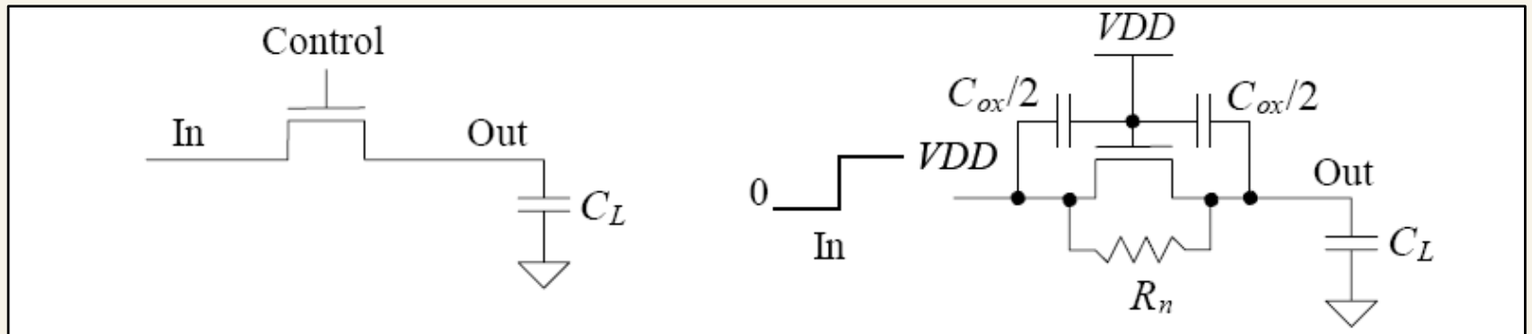


Figure 10.16 Circuits used in Ex. 10.3.

- Delay through a Pass Gate

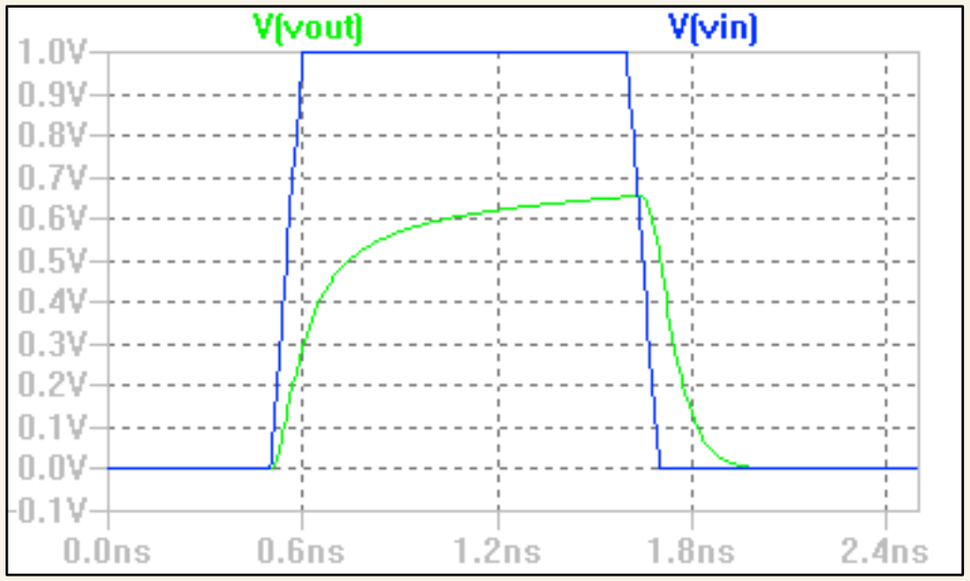
$$t_{delay} = 0.7 \cdot R_n C_{tot} = 0.7 \cdot R_n \cdot \left(C_L + \frac{C_{ox}}{2} \right)$$

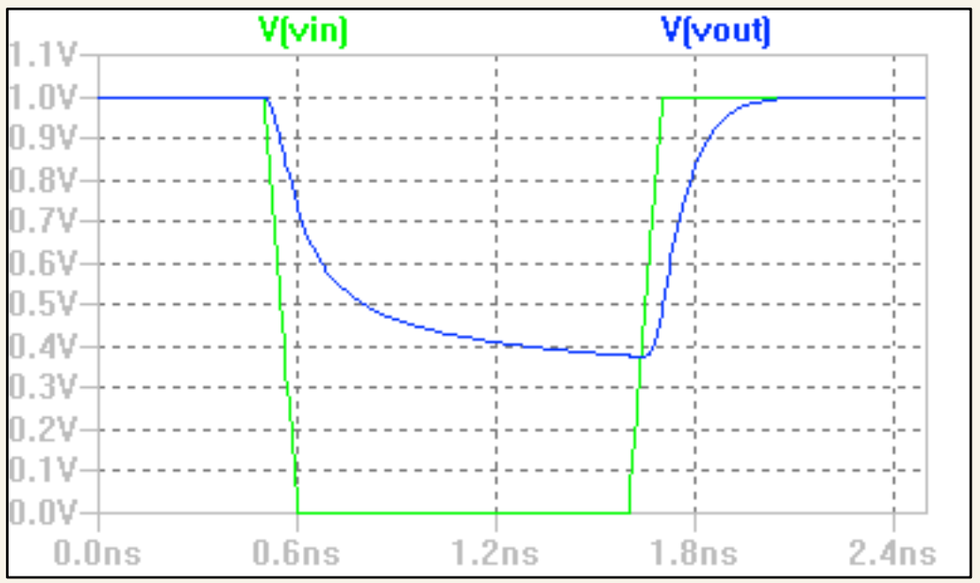


(a) Delay from the input to the output through a pass gate.

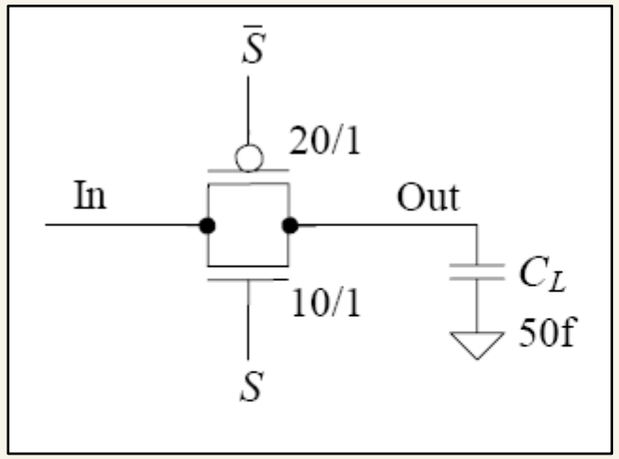
(b) The capacitances and effective resistance when turning the MOSFET on with an input 1.

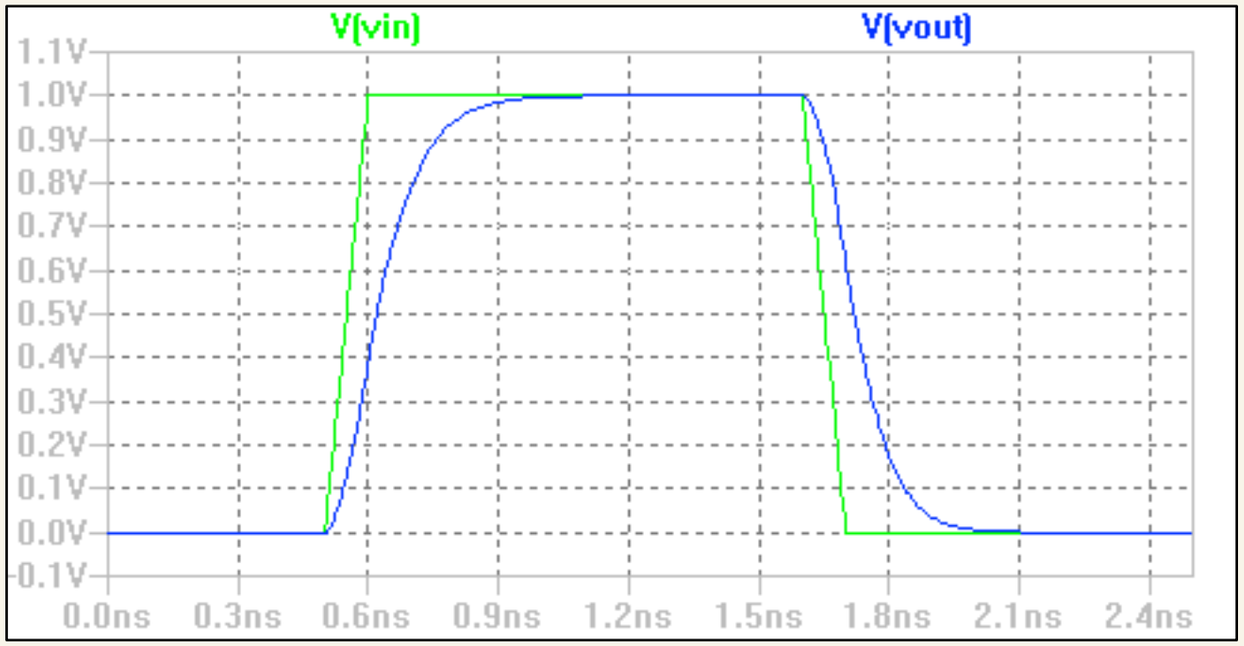
Figure 10.17 Estimating the delay through a pass transistor.





- The Transmission Gate (TG)





- Delay through Series-Connected PGs

$$t_{delay} \approx 0.35 \cdot R_n \cdot C_{ox} \cdot l^2$$

Ref. Book p 51