Ralink
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MT7621S DATASHEET

Overview

The MT7621S integrates a single-core MIPS1004Kc (880MHz), HNAT/ HQoS/ Samba/ VPN accelerators, 5-port GbE switch, RGMII, USB3.0, USB2.0, 3xPCIe, SD-XC. The powerful CPU with rich portfolio is suitable for 802.11ac, LTE cat4/5, edge, hotspot, VPN, AC (Access Control). It can also connect to touch-panel, ZigBee/Z-Wave for Internet Service Router and Home Security Gateway.

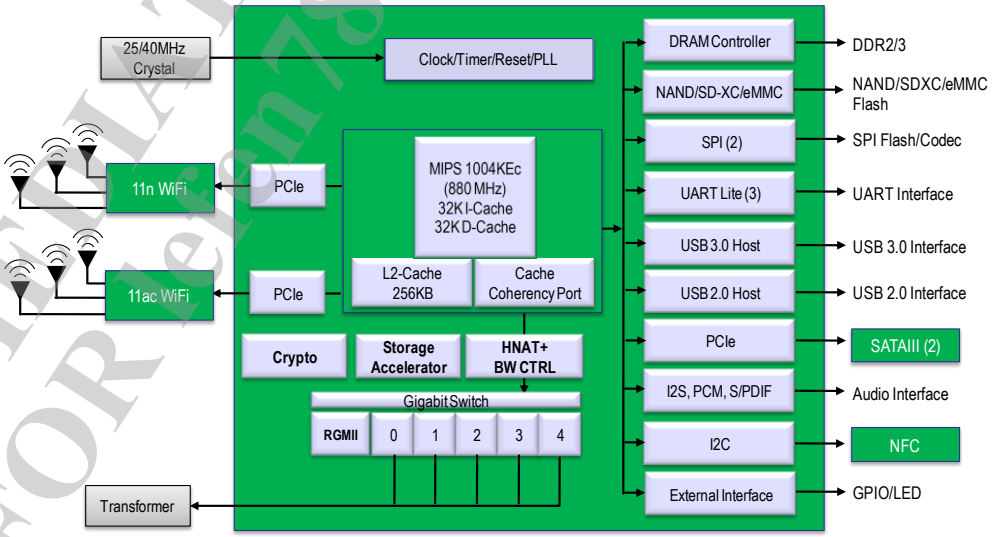
For the next generation router, MT7621S provides several dedicated hardware engines to accelerate the NAT, QoS, Samba and VPN traffic. These accelerators relief the CPU for other upper layer applications.

Applications:
- Internet service router
- Wireless router
- Home security gateway
- NAS devices
- iNICs
- Switch control processor

Features

- Embedded MIPS1004Kc (880 MHz)
  - 32 KB I-Cache and 32 KB D-Cache
  - 256 KB L2 Cache
- Gigabit Switch
  - 5 ports with full-line rate
  - 5-port 10/100/1000Mbps MDI transceivers
- One RGMII/MII interface
- 16-bit DDR2/3 up to 256/512 Mbytes
- SPI(2 chip select), NAND Flash(SLC), SDXC, eMMC(4 bits)
- USB3 x 1+ USB2 x 1 or USB2 x 2 (all host)
- PCIe host x 3
- I2C, UART Lite x 3, JTAG, MDC, MDIO, GPIO
- VoIP support (I2S, PCM)
- Audio interface (SPDIF-Tx, I2S, PCM)
- Deliver the superb Samba performance via USB 2.0/USB 3.0/SD-XC
- HW storage accelerator
- HW NAT
  - 2Gbps wired speed
  - L2 bridge
  - IPv4 routing, NAT, NAPT
  - IPv6 routing, DS-Lite, 6RD, 6to4
- HW QoS
  - 16 hardware queues to guarantee the min/max bandwidth of each flow.
  - Seamlessly co-work with HW NAT engine.
  - 2Gbps wired speed.
- HW Crypto Engine
  - Deliver 400~500 Mbps IPSec throughput
- Green
  - Intelligent Clock Scaling (exclusive)
  - DDR2/3: ODT off, Self-refresh mode
- Firmware: Linux 2.6 SDK, OpenWRT
- RGMII iNIC Driver: Linux 2.4/2.6

Functional Block Diagram



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1. Main Features

The following table covers the main features offered by the MT7621S. Overall, the MT7621S supports the requirements of an high-level AP/router, and a number of interfaces together with a large maximum RAM capacity.

Table 1-1 Main Features

Features	MT7621S
CPU	MIPS1004Kc (880 MHz, single-core)
I-Cache, D-Cache	32 KB, 32 KB
L2 Cache	256KB
HNAT/HQoS	HQoS 16 queues HNAT 2 Gbps forwarding (IPv4, IPv6 routing, DS-Lite, 6RD, 6to4)
Memory	
DRAM Controller	16-bit
DDR2	800 Mbps (max 256 MByte)
DDR3	1200 Mbps (max 512 MByte)
NAND	Small page 512-Byte (max 512 Mbit) Large page 2k-Byte (max 8 Gbit)
SPI Flash	3B addr mode (max 128 Mbit) 4B addr mode (max 512 Mbit)
SD **eMMC**	SD-XC class 10 (max 128 GByte) 4-bit eMMC (max 8 GByte)
PCIe	3
USB	USB3 x 1+ USB2 x 1 or USB2 x 2
Ethernet	5-port GSW + RGMII(1)
I2S	1
PCM	1
I2C	1
SPDIF-Tx	1
UART Lite	3
JTAG	1
Package	TFBGA 11.7 mm x 13.6 mm

1.1 Switch core

1.1.1 Overview

MT7621S switch is a highly integrated Ethernet switch with high performance and non-blocking transmission. It includes a 5-port Gigabit Ethernet MAC and a 5-port Gigabit Ethernet PHY for Dumb and Smart Switch applications. MT7621S enables an advanced power-saving feature to meet the market requirement. It complies with IEEE803.3az for Energy Efficient Ethernet and cable-length/link-down power saving mode. MediaTek's industry-leading techniques provide customers with the most cost-competitive and lowest power consumption Ethernet product in the industry.

1.1.2 Features

- 5-port 10/100/1000Mbps MDI transceivers
- Accessible MAC address table with 2048 entries and auto aging and learning capabilities
- Programmable aging timer for MAC address table
- Supports programmable 1518/1536/1552 and 9K Jumbo frame length
- Supports SVL and IVL with 8 filtering database
- Supports RSTP and MSTP
- Supports 802.1X
- Supports 4K VLAN entries
- Supports VLAN ID tag and un-tag options for each port
- Supports double tagging VLAN
- Supports hardware port isolation
- Supports 8 priority queues per port
- Supports SP, WFQ, and SP+WFQ latency scheduler
- Supports Max-Min bandwidth scheduler
- Supports ingress and egress rate control
- Supports 64 sets of ACL rules
- Supports IPv4 and IPv6 multicast frames hardware forwarding
- Supports 40 MIB counters per port
- Supports Loop detection indicator
- Supports Broadcast/Multicast/Unknown frames storm suppression
- 10Base-T, 10Base-Te, 100Base-TX, and 1000Base-T compliant Transceivers
- Compliant with IEEE 802.3 Auto-Negotiation
- Supports 3 LEDs per GEPHY port
- Supports short-cable power saving
- Integrated MDI resistors
- Supports IEEE 802.3az Energy Efficient Ethernet

2. Pins

2.1 Ball Map (Top View)

Table 2-1 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	GND	RDQ3	RDQ8		RDQ12		RDQS0		GND		RDQ2		RBA2		RWE_	RA3	RCKE	GND	A
B	DDRTEST	RDQ5	RDQ1	RDQ10	RDQM0	RDQS1_	RDQS0_	RDQM1	RDQ13	RDQ11	GND	RDQ4	RA13	RODT	RCS_	RA5	RBA1	RA1	B
C	ND_D6	RDQ7	DVDD_VREF	GND	RDQ14	GND	RDQS1	RDQ15	RCLK	RDQ9	RDQ0	RDQ6	GND	RRAS_	RCAS_	RBA0	RA14	RA11	C
D	ND_D4	ND_D5	ND_D7	GND	GND	DVDD_DRIO	DVDD_DRIO	GND	RCLK_	GND	DDR3RSTB	DVDD_DRIO	RA9	RA2	RA12	RA8	RA6		D
E		ND_D2	ND_D1	ND_D3	GND	DVDD_DRIO	DVDD_DRIO	GND	GND	GND	RA7	GND	RA10	RA0	RA4	AVDD33_MEMPLL	TP_MEMPLL	TN_MEMPLL	E
F	ND_RB_N	ND_D0	ND_RE_N	ND_WP	GND	GND	DVDDK	DVDDK	GND	GND	DVDD_DRIO	DVDD_DRIO	AVSS33_MEMPLL	GND	DVDD33_IO_4	JTCLK	JTRST_N		F
G		ND_CS_N	ND_CLE	ND_WE_N	ND_ALE	GND	GND	DVDDK	GND	GND	GND	DVDDK	GND	PERST_N	WDT_RST_N	JTDI	JTDO	JTMS	G
H	TXD3	TXD2	RXD3	RXD2	CTS3_N	DVDD33_IO_2	GND	GND	DVDDK	GND	DVDDK	GND	PCIE_CKN0	PCIE_CKP0	GND	PCIE_TXP0	PCIE_TXN0		H
J	AVDD12_SSUSB	GND	RTS2_N	RTS3_N	CTS2_N	DVDD33_IO_1	GND	DVDDK	GND	DVDDK	GND	GND	GND	GND	GND	PCIE_RXN0	PCIE_RXP0	AVDD12_PE	J
K	USB_DM_1P	USB_DP_1P	GND	AVDD33_SSUSB	AVDD33_USB	AVDD33_XDRV	GND	GND	GND	GND	DVDDK	GND	PCIE_CKP1	PCIE_CKN1	GND	PCIE_RXN1	PCIE_RXP1		K
L		SSUSB_VRT	GND	GND	GND	GND	GND	GND	GND	CBG_AVOUTP	CBG_AVOUTN	GND	GND	GND	GND	CBG_VRT	PCIE_TXN1	PCIE_TXP1	L
M	SSUSB_TXN	SSUSB_TXP	GND	USB_DM	USB_DP	DVDD_GE1_VREF	DVDD_GE1_IO	DVDD_GE1_IO	GND	GND	GND	GND	PCIE_CKP2	PCIE_CKN2	GND	GND	PCIE_RXP2	PCIE_RXN2	M
N		SSUSB_RXP	SSUSB_RXN	GND	GND	AVDD10_AFE_P0		AVDD10_AFE_P2		DVDD_K_1	AVDD33_PE	GND	GND	GND	GND	PCIE_TXP2	PCIE_TXN2		N
P	GND	GND	GND	GND	GND	AVDD10_AFE_P1	GND	AVDD10_AFE_P3	GND	DVDD_K_1	AVDD33_XPTL	GPIO0	I2C_SCLK	I2C_SD	GND	GND	XPTL_XI	XPTL_XO	P
R	GND	ESW_TXVP_B_P0	ESW_TXVN_B_P0	GND	ESW_TXVN_A_P0	AVDD10	GND	AVDD10_AFE_P4	GND	DVDD_K_1	DVDD33_IO_3	PORST_N	RXD1	TXD1	GND	GND	GE2_RXCLK		R
T		ESW_TXVP_C_P0	ESW_TXVN_C_P0	ESW_TXVP_A_P1	ESW_TXVP_A_P0	GND	GND	GND	GND	DVDD_K_1	DVDD_GE2_IO	ESW_DBG_B	SCL	GND	MDC	GE2_RXDV	GE2_RXD0	GE2_RXD1	T
U	ESW_TXVP_D_P0	ESW_TXVN_D_P0	GND	ESW_TXVN_A_P1	AVDD33_LD_P0	AVDD33_LD_P1	AVDD33_LD_P2	AVDD33_PLL_I	AVDD33_LD_P3	AVDD33_LD_P4	DVDD_GE2_IO	DVDD33_IO_4	DVDD33_IO_4	GND	MDIO	GE2_RXD2	GE2_RXD3		U
V		ESW_TXVP_B_P1	ESW_TXVN_B_P1	GND	ESW_ATEST	GND	ESW_DBG_I	ESW_DBG_O	GND	ESW_TXVP_D_P3	GND	GND	GND			GE2_TXEN	GND	GE2_TXCLK	V
W	ESW_TXVP_C_P1	ESW_TXVN_C_P1	ESW_TXVN_B_P2	AVSS33_VBG	ESW_REXT	ESW_TXVP_C_P2	ESW_TXVP_D_P2	ESW_TXVP_A_P3	ESW_TXVP_B_P3	ESW_TXVN_D_P3	GND	ESW_TXVN_B_P4	GND	ESW_TXVN_D_P4	ESW_P2_LED_0	ESW_DTEST	GE2_TXD1	GE2_TXD0	W
Y	ESW_TXVP_D_P1	ESW_TXVN_D_P1	ESW_TXVP_B_P2			ESW_TXVN_C_P2	ESW_TXVN_D_P2	ESW_TXVN_A_P3	ESW_TXVN_B_P3	ESW_TXVP_C_P3	ESW_TXVN_A_P4	ESW_TXVP_B_P4	ESW_TXVN_C_P4	ESW_TXVP_D_P4	ESW_P4_LED_0	ESW_P1_LED_0	GE2_TXD3	GE2_TXD2	Y
AA	GND	ESW_TXVP_A_P2	ESW_TXVN_A_P2			GND		GND		ESW_TXVN_C_P3	ESW_TXVP_A_P4		ESW_TXVP_C_P4		ESW_P3_LED_0		ESW_P0_LED_0	GND	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

2.2 Pin Descriptions

Table 2-2 Pin Description

Pin	Name	Type	Driving	Description
GPIO				
P12	GPIO0	O, IPU	4 mA	GPO0 (output only)
UART				
R13	RXD1	I, IPU	4 mA	UART Lite RX Data
R14	TXD1	O, IPU	4 mA	UART Lite TX Data
H4	RXD2	I, IPD	4 mA	UART RX Data
H2	TXD2	O, IPD	4 mA	UART TX Data
J5	CTS2_N	I, IPD	4 mA	UART Clear To Send
J3	RTS2_N	O, IPD	4 mA	UART Request To Send
H3	RXD3	I, IPD	4 mA	UART RX Data
H1	TXD3	O, IPD	4 mA	UART TX Data
H5	CTS3_N	I, IPD	4 mA	UART Clear To Send
J4	RTS3_N	O, IPD	4 mA	UART Request To Send
JTAG				
G17	JTDO	O, IPD	4 mA	JTAG Data Output
G16	JTDI	I/O, IPD	4 mA	JTAG Data Input
G18	JTMS	I/O, IPD	4 mA	JTAG Mode Select
F16	JTCLK	I/O, IPD	4 mA	JTAG Clock
F17	JTRST_N	I/O, IPU	4 mA	JTAG Target Reset
I2C				
P13	I2C_SCLK	I/O, IPD	4 mA	I2C Clock
P14	I2C_SD	O, IPD	4 mA	I2C Data
NAND				
G2	ND_CS_N	O, IPU	4 mA	NAND Flash Chip Select
F3	ND_RE_N	O, IPU	4 mA	NAND Flash Read Enable
G4	ND_WE_N	O, IPU	4 mA	NAND Flash Write Enable
F4	ND_WP	O	6 mA	NAND Flash Write Protect
G3	ND_CLE	O	6 mA	NAND Flash Command Latch Enable
G5	ND_ALE	O	6 mA	NAND Flash ALE Latch Enable
F1	ND_RB_N	I	6 mA	NAND Flash Ready/Busy
F2	ND_D0	I/O	6 mA	NAND Flash Data0
E3	ND_D1	I/O	6 mA	NAND Flash Data1
E2	ND_D2	I/O	6 mA	NAND Flash Data2
E4	ND_D3	I/O	6 mA	NAND Flash Data3
D1	ND_D4	I/O, IPU	4 mA	NAND Flash Data4
D2	ND_D5	I/O, IPU	4 mA	NAND Flash Data5
C1	ND_D6	I/O, IPU	4 mA	NAND Flash Data6
D3	ND_D7	I/O, IPU	4 mA	NAND Flash Data7
RGMII/MII (3.3 V)				

Pin	Name	Type	Driving	Description
R17	GE2_RXCLK	I/O	12 mA	RGMII2 Rx Clock
T16	GE2_RXDV	I	12 mA	RGMII2 Rx Data Valid
T17	GE2_RXD0	I	12 mA	RGMII2 Rx Data bit #0
T18	GE2_RXD1	I	12 mA	RGMII2 Rx Data bit #1
U16	GE2_RXD2	I	12 mA	RGMII2 Rx Data bit #2
U17	GE2_RXD3	I	12 mA	RGMII2 Rx Data bit #3
V18	GE2_TXCLK	I/O	12 mA	RGMII2 Tx Clock
V16	GE2_TXEN	O	12 mA	RGMII2 Tx Data Valid
W18	GE2_TXD0	O	12 mA	RGMII2 Tx Data bit #0
W17	GE2_TXD1	O	12 mA	RGMII2 Tx Data bit #1
Y18	GE2_TXD2	O	12 mA	RGMII2 Tx Data bit #2
Y17	GE2_TXD3	O	12 mA	RGMII2 Tx Data bit #3
PHY Management (3.3 V)				
T15	MDC	O	6 mA	PHY Management Clock. Shared with GPIO23
U15	MDIO	I/O	6 mA	PHY Management Data. Shared with GPIO22
5-Port GiGa(10/100/1000) Switch				
AA17	ESW_P0_LED_0	I/O	4 mA	Port #0 PHY LED indicators
W16	ESW_DTEST	I/O	4 mA	Digital test
Y16	ESW_P1_LED_0	I/O	4 mA	Port #1 PHY LED indicators
W15	ESW_P2_LED_0	I/O	4 mA	Port #2 PHY LED indicators
AA15	ESW_P3_LED_0	I/O	4 mA	Port #3 PHY LED indicators
Y15	ESW_P4_LED_0	I/O	4 mA	Port #4 PHY LED indicators
W5	ESW_REXT	A		Band gap resistor which is connected to AVSS33_BG through a 24kΩ (±1%) resistor
V5	ESW_ATEST	A		Analog test
R5	ESW_TXVN_A_P0	A		Port #0 MDI Transceivers
R3	ESW_TXVN_B_P0	A		Port #0 MDI Transceivers
T3	ESW_TXVN_C_P0	A		Port #0 MDI Transceivers
U2	ESW_TXVN_D_P0	A		Port #0 MDI Transceivers
T5	ESW_TXVP_A_P0	A		Port #0 MDI Transceivers
R2	ESW_TXVP_B_P0	A		Port #0 MDI Transceivers
T2	ESW_TXVP_C_P0	A		Port #0 MDI Transceivers
U1	ESW_TXVP_D_P0	A		Port #0 MDI Transceivers
U4	ESW_TXVN_A_P1	A		Port #1 MDI Transceivers
V3	ESW_TXVN_B_P1	A		Port #1 MDI Transceivers
W2	ESW_TXVN_C_P1	A		Port #1 MDI Transceivers
Y2	ESW_TXVN_D_P1	A		Port #1 MDI Transceivers
T4	ESW_TXVP_A_P1	A		Port #1 MDI Transceivers
V2	ESW_TXVP_B_P1	A		Port #1 MDI Transceivers
W1	ESW_TXVP_C_P1	A		Port #1 MDI Transceivers
Y1	ESW_TXVP_D_P1	A		Port #1 MDI Transceivers
AA3	ESW_TXVN_A_P2	A		Port #2 MDI Transceivers

Pin	Name	Type	Driving	Description
W3	ESW_TXVN_B_P2	A		Port #2 MDI Transceivers
Y6	ESW_TXVN_C_P2	A		Port #2 MDI Transceivers
Y7	ESW_TXVN_D_P2	A		Port #2 MDI Transceivers
AA2	ESW_TXVP_A_P2	A		Port #2 MDI Transceivers
Y3	ESW_TXVP_B_P2	A		Port #2 MDI Transceivers
W6	ESW_TXVP_C_P2	A		Port #2 MDI Transceivers
W7	ESW_TXVP_D_P2	A		Port #2 MDI Transceivers
Y8	ESW_TXVN_A_P3	A		Port #3 MDI Transceivers
Y9	ESW_TXVN_B_P3	A		Port #3 MDI Transceivers
AA10	ESW_TXVN_C_P3	A		Port #3 MDI Transceivers
W10	ESW_TXVN_D_P3	A		Port #3 MDI Transceivers
W8	ESW_TXVP_A_P3	A		Port #3 MDI Transceivers
W9	ESW_TXVP_B_P3	A		Port #3 MDI Transceivers
Y10	ESW_TXVP_C_P3	A		Port #3 MDI Transceivers
V10	ESW_TXVP_D_P3	A		Port #3 MDI Transceivers
Y11	ESW_TXVN_A_P4	A		Port #4 MDI Transceivers
W12	ESW_TXVN_B_P4	A		Port #4 MDI Transceivers
Y13	ESW_TXVN_C_P4	A		Port #4 MDI Transceivers
W14	ESW_TXVN_D_P4	A		Port #4 MDI Transceivers
AA11	ESW_TXVP_A_P4	A		Port #4 MDI Transceivers
Y12	ESW_TXVP_B_P4	A		Port #4 MDI Transceivers
AA13	ESW_TXVP_C_P4	A		Port #4 MDI Transceivers
Y14	ESW_TXVP_D_P4	A		Port #4 MDI Transceivers
V7	ESW_DBG_I	I		Debug pin
V8	ESW_DBG_O	O		Debug pin
T12	ESW_DBG_B	I		Debug pin
PCIe				
G14	PERST_N	O, IPU	4 mA	PICe reset.
H13	PCIE_CKN0	O		PCIe0 reference clock (negative)
H14	PCIE_CKP0	O		PCIe0 reference clock (positive)
H17	PCIE_TXN0	O		PCIe0 differential transmit TX -
H16	PCIE_TXP0	O		PCIe0 differential transmit TX+
J16	PCIE_RXN0	I		PCIe0 differential receive RX -
J17	PCIE_RXP0	I		PCIe0 differential receive RX +
K14	PCIE_CKN1	O		PCIe1 reference clock (negative)
K13	PCIE_CKP1	O		PCIe1 reference clock (positive)
L17	PCIE_TXN1	O		PCIe1 differential transmit TX -
L18	PCIE_TXP1	O		PCIe1 differential transmit TX+
K16	PCIE_RXN1	I		PCIe1 differential receive RX -
K17	PCIE_RXP1	I		PCIe1 differential receive RX +
M14	PCIE_CKN2	O		PCIe2 reference clock (negative)
M13	PCIE_CKP2	O		PCIe2 reference clock (positive)

Pin	Name	Type	Driving	Description	
N17	PCIE_TXN2	O		PCIe2 differential transmit TX -	
N16	PCIE_TXP2	O		PCIe2 differential transmit TX+	
M18	PCIE_RXN2	I		PCIe2 differential receive RX -	
M17	PCIE_RXP2	I		PCIe2 differential receive RX +	
USB					
L2	SSUSB_VRT	I/O		USB Port0 reference pin (USB3.0)	
N3	SSUSB_RXN	I/O		USB Port0 SS data pin RX- (USB3.0)	
N2	SSUSB_RXP	I/O		USB Port0 SS data pin RX+ (USB3.0)	
M1	SSUSB_TXN	I/O		USB Port0 SS data pin TX- (USB3.0)	
M2	SSUSB_TXP	I/O		USB Port0 SS data pin TX+ (USB3.0)	
M4	USB_DM_P0	I/O		USB Port0 HS/FS/LS data pin Data- (USB3.0)	
M5	USB_DP_P0	I/O		USB Port0 HS/FS/LS data pin Data+ (USB3.0)	
K1	USB_DM_P1	I/O		USB Port1 data pin Data- (USB2.0)	
K2	USB_DP_P1	I/O		USB Port1 data pin Data+ (USB2.0)	
DDR				**DDR3**	**DDR2**
C11	RDQ0	I/O		Data bit #0	Data bit #6
B3	RDQ1	I/O		Data bit #1	Data bit #7
A11	RDQ2	I/O		Data bit #2	Data bit #1
A2	RDQ3	I/O		Data bit #3	Data bit #0
B12	RDQ4	I/O		Data bit #4	Data bit #4
B2	RDQ5	I/O		Data bit #5	Data bit #2
C12	RDQ6	I/O		Data bit #6	Data bit #3
C2	RDQ7	I/O		Data bit #7	Data bit #5
A3	RDQ8	I/O		Data bit #8	Data bit #10
C10	RDQ9	I/O		Data bit #9	Data bit #11
B4	RDQ10	I/O		Data bit #10	Data bit #13
B10	RDQ11	I/O		Data bit #11	Data bit #12
A5	RDQ12	I/O		Data bit #12	Data bit #15
B9	RDQ13	I/O		Data bit #13	Data bit #9
C5	RDQ14	I/O		Data bit #14	Data bit #8
C8	RDQ15	I/O		Data bit #15	Data bit #14
E14	RA0	O		Address bit #0	Address bit #1
B18	RA1	O		Address bit #1	Address bit #0
D14	RA2	O		Address bit #2	Address bit #10
A16	RA3	O		Address bit #3	Address bit #12
E15	RA4	O		Address bit #4	Address bit #4
B16	RA5	O		Address bit #5	RAS
D17	RA6	O		Address bit #6	Address bit #8
E11	RA7	O		Address bit #7	WE
D16	RA8	O		Address bit #8	Address bit #13
D13	RA9	O		Address bit #9	Bank Address bit #1
E13	RA10	O		Address bit #10	Address bit #3

Pin	Name	Type	Driving	Description	
C18	RA11	O		Address bit #11	Address bit #11
D15	RA12	O		Address bit #12	CAS
B13	RA13	O		Address bit #13	Bank Address #2
C17	RA14	O		Address bit #14	Address bit #6
C16	RBA0	O		Bank Address #0	Address bit #9
B17	RBA1	O		Bank Address #1	Address bit #2
A13	RBA2	O		Bank Address #2	Bank Address #0
C14	RRAS_	O		RAS	Address bit #5
C15	RCAS_	O		CAS	Address bit #7
A15	RWE_	O		WE	NC
C9	RCLK	O		Clock	Clock
D9	RCLK_	O		Clock	Clock
B5	RDQM0	O		DM#0	DM#0
B8	RDQM1	O		DM#1	DM#1
B15	RCS_	O		CS	CS
A7	RDQS0	I/O		DQS#0	DQS#0
B7	RDQS0_	I/O		DQS#0	DQS#0
C7	RDQS1	I/O		DQS#1	DQS#1
B6	RDQS1_	I/O		DQS#1	DQS#1
A17	RCKE	O		CKE	CKE
B14	RODT	O		ODT	ODT
D11	DDR3RSTB	O		Reset	NC
B1	DDRTEST	A		DDR Test	
XTAL					
P17	XPTL_XI	I		XTAL clock input	
P18	XPTL_XO	0		XTAL clock output (for single-end mode, this pin will be XTAL clock input)	
Misc					
R12	PORST_N	I		Power on reset	
G15	WDT_RST_N	O, IPU	4 mA	Watchdog reset	
L16	CBG_VRT	A		24K 1% raccurate resistor	
L11	CBG_AVOUTN	A		CBG test	
L10	CBG_AVOUTP	A		CBG test	
E18	TN_MEMPLL	A		PLL test	
E17	TP_MEMPLL	A		PLL test	
T13	SCL	I/O		SCAN	
Power					
J6, H6, R11, U12, U13, F15	DVDD33_IO_1/2/3/4	P		3.3 V digital I/O power supply	

Pin	Name	Type	Driving	Description
F7, F8, G8, J8, H9, J10, H11, K11, G12	DVDDK	P		1.1 V digital SOC core power supply
N10, P10, R10, T10	DVDD_K_1			1.0 V digital ESW core power supply
C3	DVDD_VREF	P		0.75V/0.9 V reference voltage power supply for DDR3/DDR2
D6, D7, D12, E7, E6, F11, F12	DVDD_DDRIO	P		1.5 V/1.8 V power supply for DDR3/DDR2
M6	DVDD_GE1_VREF	P		0.75V/0.9 V reference voltage power supply for GE1
M7, M8	DVDD_GE1_IO	P		1.5V/1.8V power supply for GE1
T11, U11	DVDD_GE2_IO	P		2.5V/3.3V power supply for GE2
R6	AVDD10	P		1.0V analog ESW power supply
N6, P6, N8, P8, R8	AVDD10_AFE_P0/1/2/3/4	P		1.0V analog ESW power supply
J18	AVDD12_PE	P		1.2V analog PCIe power supply
J1	AVDD12_SSUSB	P		1.2V analog USB power supply
U5, U6, U7, U9, U10	AVDD33_LD_P0/1/2/3/4	P		3.3V analog ESW power supply
E16	AVDD33_MEMPLL	P		3.3V analog PLL power supply
N11	AVDD33_PE	P		3.3V analog PCIe power supply
U8	AVDD33_PLL_1	P		3.3V analog ESW power supply
K4	AVDD33_SSUSB	P		3.3V analog USB power supply
K5	AVDD33_USB	P		3.3V analog USB power supply
K6	AVDD33_XDRV	P		3.3V analog XTAL drive power supply
P11	AVDD33_XPTL	P		3.3V analog XTAL power supply
Ground				
F13	AVSS33_MEMPLL	G		
W4	AVSS33_VBG	G		

Pin	Name	Type	Driving	Description
A1, A18, A9, AA1, AA18, AA6, AA8, B11, C13, C4, C6, D10, D4, D5, D8, E10, E5, E8, E9, F10, E12 F14, F5, F6, F9, G10, G13, G6, G7, G9, G11, H10, H12, H15, H7, H8, J11, J12, J13, J14, J15, J2, J7, J9, K10, K12, K15, K3, K6, K7, K8, K9, L12, L13, L14, L15, L3, L4, L5, L6, L7, L8, L9, M10, M11, M12, M15, M16, M3, M9, N12, N13, N14, N15, N4, N5, P1, P15, P16, P2, P3, P4, P5, P7, P9, R1, R15, R16, R4, R7, R9, T14, T6, T7, T8, T9, U14, U3, V11, V12, V13, V17, V4, V6, V9, W11, W13	GND	G		Ground
Total: 346 balls				

NOTE:

IPD:	Internal pull-down	IO:	Bi-directional
IPU:	Internal pull-up	P:	Power
I:	Input	G:	Ground
O:	Output	NC:	Not connected

2.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. The MT7621S provides up to 49 GPIO pins. Users can configure SYSCFG and GPIOMODE registers in the System Control block to specify the pin function, or they can use the registers specified below. For more information, see the Programmer's Guide. Unless specified explicitly, all the GPIO pins are in input mode after reset.

2.3.1 GPIO pin share scheme

Table 2-3 GPIO Pin Share

Pin Group	Normal Mode	GPIO Mode	Strap Mode
GPIO	GPIO0	GPO#0	CHIP_MODE[0]
UART	RXD1	GPIO#1	
	TXD1	GPIO#2	CHIP_MODE[1]
I2C	I2C_SD	GPIO#3	
	I2C_SCLK	GPIO#4	
UART	RTS3_N	GPIO#5	CHIP_MODE[2]
	CTS3_N	GPIO#6	
	TXD3	GPIO#7	
	RXD3	GPIO#8	
UART	RTS2_N	GPIO#9	CHIP_MODE[3]
	CTS2_N	GPIO#10	
	TXD2	GPIO#11	DRAM_TYPE
	RXD2	GPIO#12	
JTAG	JTDO	GPIO#13	
	JTDI	GPIO#14	
	JTMS	GPIO#15	
	JTCLK	GPIO#16	
	JTRST_N	GPIO#17	
WDT_RST_N	WDT_RST_N	GPIO#18	
PCIe	PERST_N	GPIO#19	OCP_RATIO
MDC/MDIO	MDIO	GPIO#20	
	MDC	GPIO#21	XTAL_MODE[0]
GE2	GE2_TXD0	GPIO#22	
	GE2_TXD1	GPIO#23	
	GE2_TXD2	GPIO#24	
	GE2_TXD3	GPIO#25	
	GE2_TXEN	GPIO#26	
	GE2_TXCLK	GPIO#27	
	GE2_RXD0	GPIO#28	
	GE2_RXD1	GPIO#29	
	GE2_RXD2	GPIO#30	

Pin Group	Normal Mode	GPIO Mode	Strap Mode
	GE2_RXD3	GPIO#31	
	GE2_RXDV	GPIO#32	
	GE2_RXCLK	GPIO#33	
NAND	ND_CS_N	GPIO#34	XTAL_MODE[1]
	ND_WE_N	GPIO#35	XTAL_MODE[2]
	ND_RE_N	GPIO#36	
	ND_D4	GPIO#37	
	ND_D5	GPIO#38	
	ND_D6	GPIO#39	
	ND_D7	GPIO#40	
	ND_WP	GPIO#41	
	ND_RB_N	GPIO#42	DRAM_FROM_EE
	ND_CLE	GPIO#43	
	ND_ALE	GPIO#44	
	ND_D0	GPIO#45	
	ND_D1	GPIO#46	
	ND_D2	GPIO#47	
	ND_D3	GPIO#48	

2.3.2 UART pin share scheme

Table 2-4 UART_1 Pin Share

Pin Name	0	1
RXD1	TXD1	GPIO#1
TXD1	RXD1	GPIO#2

Note: Controlled by the UART1_MODE register.

Table 2-5 UART_2 Pin Share

Pin Name	0	1	2	3
RTS2_N	RTS2_N	GPIO#9	PCM_DTX	GPIO#9
CTS2_N	CTS2_N	GPIO#10	PCM_DRX	GPIO#10
TXD2	TXD2	GPIO#11	PCM_CLK	SPDIF_TX
RXD2	RXD2	GPIO#12	PCM_FS	GPIO#12

Note: Controlled by the UART2_MODE register.

Table 2-6 UART_3 Pin Share

Pin Name	0	1	2	3
RTS3_N	RTS3_N	GPIO#5	I2S_SDO	SPDIF_TX
CTS3_N	CTS3_N	GPIO#6	I2S_CLK	GPIO#6
TXD3	TXD3	GPIO#7	I2S_WS	GPIO#7

Pin Name	0	1	2	3
RXD3	RXD3	GPIO#8	I2S_SDI	GPIO#8

Note: Controlled by the UART3_MODE register.

2.3.3 RGMII pin share schemes

Table 2-7 RGMII Pin Share

Pin Name	0	1
GE2_RXCLK	GE2_RXCLK	GPIO#33
GE2_RXDV	GE2_RXDV	GPIO#32
GE2_RXD0 to 3	GE2_RXD0 to 3	GPIO#28 to 31
GE2_TXCLK	GE2_TXCLK	GPIO#27
GE2_TXEN	GE2_TXEN	GPIO#26
GE2_TXD0 to 3	GE2_TXD0 to 3	GPIO#22 to 25

Note: Controlled by the RGMII2_MODE register.

2.3.4 WDT_RST_MODE pin share scheme

Table 2-8 WDT_RST Pin Share

Pin Name	0	1	2, 3
WDT_RST_N	WDT_RST_N	GPIO#18	REFCLK0_OUT

Note: Controlled by the WDT_RST_MODE register.

2.3.5 PERST_N pin share scheme

Table 2-9PERST_N Pin Share

Pin Name	0	1	2, 3
PERST_N	PERST_N	GPIO#19	REFCLK0_OUT

Note: Controlled by the PERST_MODE register.

2.3.6 MDC/MDIO pin share scheme

Table 2-10 MDC/MDIO Pin Share

Pin Name	0	1	2, 3
MDIO	MDIO	GPIO #20	GPIO #20
MDC	MDC	GPIO #21	REFCLK0_OUT

Note: Controlled by the the MDIO_MODE register.

2.3.7 NAND/SDXC/SPI pin share scheme

Table 2-11 NAND Pin Share

Pin Name	0	1	2, 3
ND_WP	SD_WP	GPIO#41	ND_WP
ND_RB_N	SD_CLK	GPIO#42	ND_RB_N
ND_CLE	SD_CD	GPIO#43	ND_CLE
ND_ALE	SD_CMD	GPIO#44	ND_ALE
ND_D0	SD_DATA0	GPIO#45	ND_D0
ND_D1	SD_DATA1	GPIO#46	ND_D1
ND_D2	SD_DATA2	GPIO#47	ND_D2
ND_D3	SD_DATA3	GPIO#48	ND_D3

Note: Controlled by the SDXC_MODE register.

Pin Name	0	1	2, 3
ND_CS_N	SPI_CS0	GPIO#34	ND_CS_N
ND_WE_N	SPI_CS1	GPIO#35	ND_WE_N
ND_RE_N	SPI_CLK	GPIO#36	ND_RE_N
ND_D4	SPI_MISO	GPIO#37	ND_D4
ND_D5	SPI_MOSI	GPIO#38	ND_D5
ND_D6	SPI_WP	GPIO#39	ND_D6
ND_D7	SPI_HOLD	GPIO#40	ND_D7

Note: Controlled by the SPI_MODE register.

2.3.8 Pin share function description

Pin Name	I/O	Pin Share Function description
PCMDTX	O	PCM Data Transmit DATA signal sent from the PCM host to the external codec.
PCMDRX	I	PCM Data Receive DATA signal sent from the external codec to the PCM host.
PCMCLK	I/O	PCM Clock The clock signal can be generated by the PCM host (Output direction), or provided by an external clock (input direction). The clock frequency should match the slot configuration of the PCM host. e.g. 4 slots, PCM clock out/in should be 256 kHz. 8 slots, PCM clock out/in should be 512 kHz. 16 slots, PCM clock out/in should be 1.024 MHz. 32 slots, PCM clock out/in should be 2.048 MHz. 64 slots, PCM clock out/in should be 4.096 MHz. 128 slots, PCM clock out/in should be 8.192 MHz.
PCMFS	I/O	PCM SYNC signal. In our design, the direction of this signal is independent of the direction of PCMCLK. Its direction and mode is configurable.
I2SSDI	I	I^2S Data input
I2SSDO	O	I^2S Data output
I2SWS	I/O	I^2S Channel Selection (or Word selection) In master mode the pin data direction is set to output, in slave mode it is set to input.
I2SCLK	I/O	I^2S clock In master mode the pin data direction is set to output, in slave mode it is set to input.
SD_WP	I	SDXC write protect
SD_CLK	O	SDXC clock
SD_CD	I	SDXC card detection
SD_CMD	I/O	SDXC command / Bus state
SD_DATA0	I/O	SDXC DATA line bit 0
SD_DATA1	I/O	SDXC DATA line bit 1
SD_DATA2	I/O	SDXC DATA line bit 2
SD_DATA3	I/O	SDXC DATA line bit 3
SPI_CS0	O	SPI chip select 0
SPI_CS1	O	SPI chip select 1
SPI_CLK	O	SPI clock
SPI_MISO	I/O	Master input/Slave output
SPI_MOSI	I/O	Master output/Slave input
SPI_WP	O	GPO function
SPI_HOLD	O	GPO function
SPDIF_TX	O	SPDIF transmit

2.3.9 xMII PHY/MAC Pin Mapping

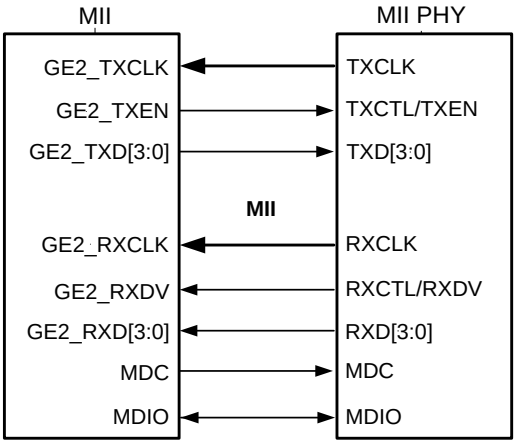


Figure 2-1 MII → MII PHY

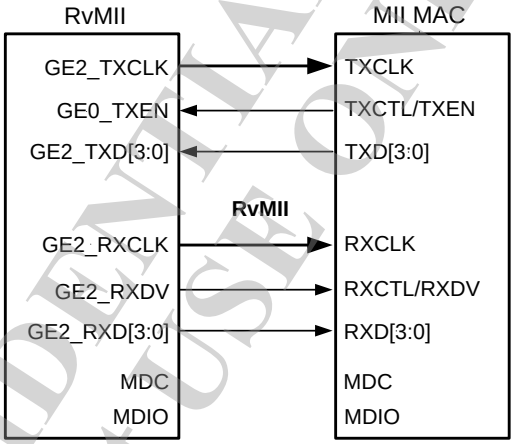


Figure 2-2 RvMII → MII MAC

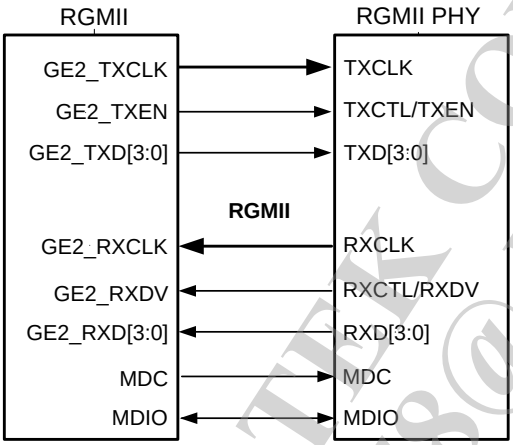


Figure 2-3 RGMII → RGMII PHY

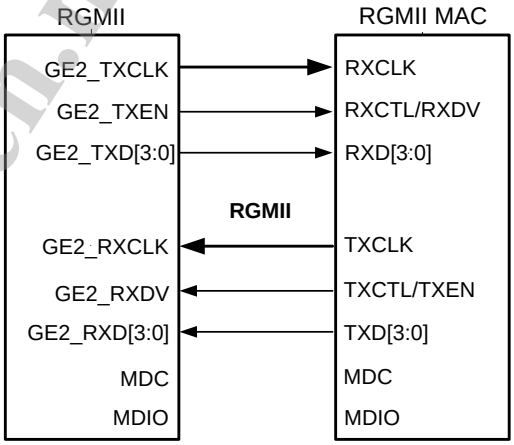


Figure 2-4 RGMII→ RGMII MAC

2.4 Strapping Options

Table 2-12 Strapping

Pin Name	Strapping Name	Description
ND_RB_N	DRAM_FROM _EE	Validate at iNIC mode or Boot from NAND. 0: DRAM/PLL configuration from EEPROM 1: DRAM configuration from Auto Detect[2]
{ND_WE_N ,ND_CS_N , MDC}	XTAL_MODE[1]	0: Reserved 1: Reserved 2: Reserved 3: 40 MHz, Self Oscillation mode[2] 4: 40 MHz, Single end input 5: 40 MHz, differential input 6: 25 MHz, Self Oscillation mode 7: 25 MHz, Single end input
PERST_N	OCP_RATIO	0: 1:3[2] 1: 1:4
TXD2	DRAM_TYPE	0: DDR3 [2] 1: DDR2
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	

	Mode	Description
0	N/A	N/A
1	Normal	Boot from ROM (NAND page 2k+64 bytes)
2	Normal	Boot from SPI 3-byte address[2]
3	Nomal	Boot from SPI 4-byte address
4	iNIC RGMII	Boot from ROM
5	iNIC MII	Boot from ROM
6	iNIC RVMII	Boot from ROM
7	iNIC PHY	Boot from ROM
8	N/A	N/A
9	Normal	Boot from internal SRAM
10	Normal	Boot from ROM (NAND page 2k+128 bytes)
11	Normal	Boot from ROM (NAND page 4k+128 bytes)
12	Normal	Boot from ROM (NAND page 4k+224 bytes)
13	Debug	Engineer debug
14	N/A	N/A
15	N/A	N/A

Note: 1. The XPTL_XO will be XTAL clock input pin while XTAL_MODE is single-end mode.
2. DDR3 reference board setting.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	DC supply voltage for IO	-0.2	-	3.6	V
VDD18	DC supply voltage for DDR2	-0.5	-	2.3	V
VDD15	DC supply voltage for DDR3	-0.4	-	1.975	V
VDD12	DC supply voltage for core	-0.2	-	1.32	V
VDD11	DC supply voltage for core	-0.2	-	1.21	V
VDD10	DC supply voltage for core	-0.3	-	1.15	V
V_{ESD}	ESD protection (HBM)	-	-	2000	V

3.2 Recommended Operating Range

Table 3-2 Recommended Operating Range

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	DC supply voltage for IO	3.14	3.3	3.46	V
VDD18	DC supply voltage for DDR2	1.7	1.8	1.9	V
VDD15	DC supply voltage for DDR3	1.425	1.5	1.575	V
VDD12	DC supply voltage for core	1.1	1.2	1.26	V
VDD11	DC supply voltage for core	1.08	1.14	1.21	V
VDD10	DC supply voltage for core	0.95	1.0	1.10	V
Ta	Ambient temperature for MT7621S	-20	-	55	°C
Ta	Ambient temperature for MT7621IS	-40	-	85	°C

3.3 DC Characteristics

Table 3-3 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input hihg voltage	2.0	-	3.63	V
V_{OL}	Output low voltage	-	-	0.4	V
V_{OH}	Output high voltage	2.4	-	-	V
R_{PU}	Input pull-up resistance	40	75	190	KΩ
R_{PD}	Input pull-down resistance	40	75	190	KΩ

3.4 Thermal Characteristics

Thermal characteristics when stationary, without an external heat sink in an air-conditioned environment.

Table 3-4 Thermal Characteristics

Symbol	Description	Performance	
		Typ	Unit
T_J	Maximum junction temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance for JEDEC 2L system PCB	27.10	°C/W
θ_{JA}	Thermal Resistance for JEDEC 4L system PCB	20.85	°C/W
θ_{JC}	Thermal Resistance for JEDEC system PCB	7.0	°C/W
ψ_{Jt}	Thermal Characterization parameter for JEDEC 2L system PCB	3.7	°C/W
ψ_{Jt}	Thermal Characterization parameter for JEDEC 4L system PCB	3.3	°C/W

Note: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4”x4.5”)

3.5 Current Consumption

Please check with application note.

Table 3-5 Current Consumption

3.6 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 0 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

3.7 External Xtal Specfication

Table 3-6 External Xtal Specifications

Frequency	25/40 Mhz
Frequency offset	+/-20 ppm
Duty cycle	45% to 55%

3.8 AC Electrical Characteristics

3.8.1 DDR SDRAM Interface

The DDR2 SDRAM interface complies with 400 MHz timing requirements for standard DDR2 SDRAM. The interface drivers are SSTL_18 drivers matching the EIA/JEDEC standard JESD79-2B.
The DDR3 SDRAM interface complies with 600 MHz timing requirements for standard DDR3 SDRAM. The interface drivers are SSTL_15 drivers matching the EIA/JEDEC standard JESD79-3E.

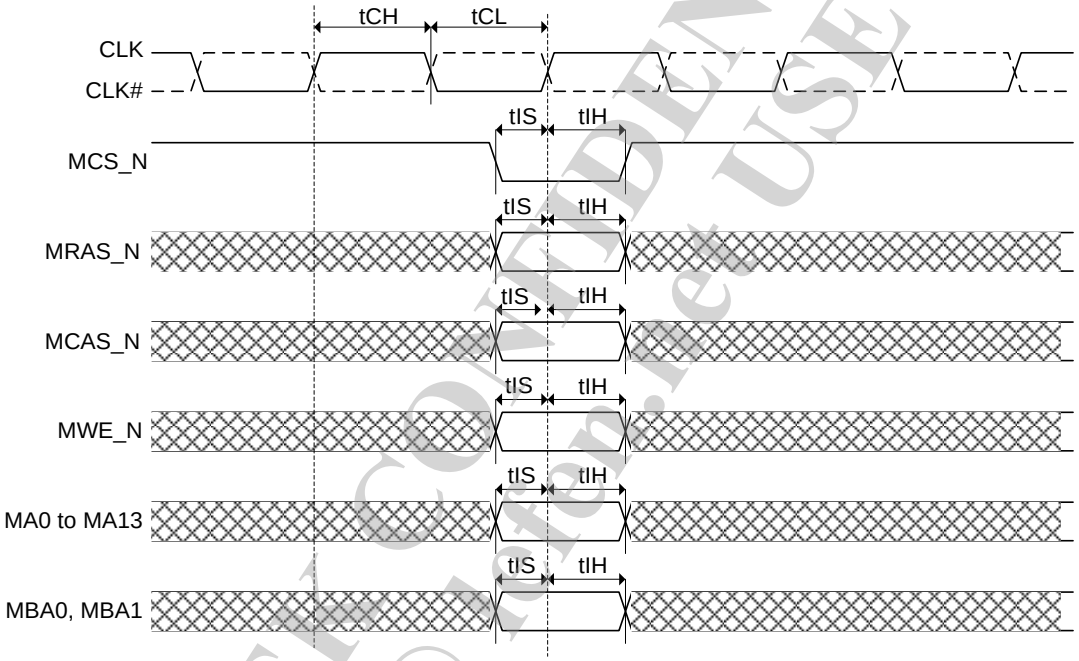


Figure 3-1 DDR2 SDRAM Command Timing

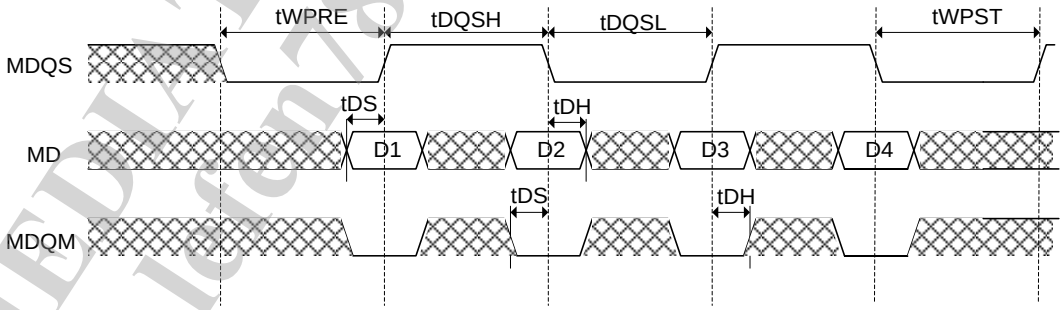


Figure 3-2 DDR2 SDRAM Write Timing

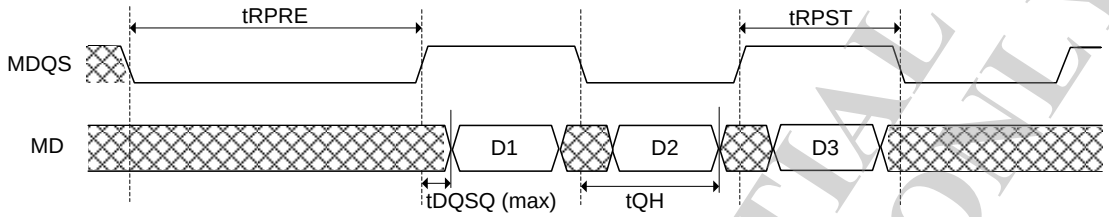


Figure 3-3 DDR2 SDRAM Read Timing

Table 3-7 DDR2 SDRAM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Clock cycle time	2.5	-	ns	
tAC	DQ output access time from SDRAM CLK	-0.35	0.35	ns	
tDQSCK	DQS output access time from SDRAM CLK	-0.5	0.5	ns	
tCH	SDRAM CLK high pulse width	0.48	0.52	tCK(avg)	
tCL	SDRAM CLK low pulse width	0.48	0.52	tCK(avg)	
tHP	SDRAM CLK half period	Min(tCH,tCL)	-	ns	
tIS	Address and control input setup time	175	-	ps	
tIH	Address and control input hold time	250	-	ps	
tDQSQ	Data skew of DQS and associated DQ	-	0.2	ns	
tQH	DQ/DQS output hold time from DQS	tHP-0.3	-	ns	
tRPRE	DQS read preamble	0.9	1.1	tCK	
tRPST	DQS read postamble	0.4	0.6	tCK	
tDQSS	DQS rising edge to CK rising edge	-0.25	0.25	tCK	
tDQSH	DQS input-high pulse width	0.35	-	tCK	
tDQSL	DQS input-low pulse width	0.35	-	tCK	
tDSS	DQS falling edge to SDRAM CLK setup time	0.2	-	tCK	
tDSH	DQS falling edge hold time from SDRAM CLK	0.2	-	tCK	
tWPRE	DQS write preamble	0.35	-	tCK	
tWPST	DQS write postamble	0.4	0.6	tCK	
tDS	DQ and DQM input setup time	*0.05	-	ns	
tDH	DQ and DQM input hold time	*0.125	-	ns	

NOTE: Depends on slew rate of DQS and DQ/DQM for single ended DQS.

3.8.2 RGMII Interface

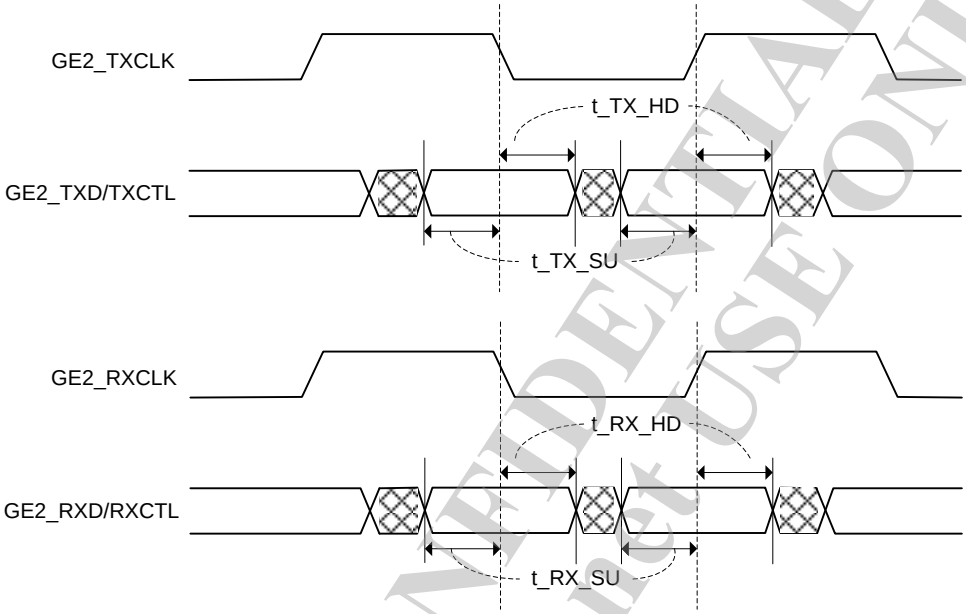


Figure 3-4 RGMII Timing

Table 3-8 RGMII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_SU	Setup time for output signals (e.g. GE0_TXD*, GE0_TXEN)	1.2	-	ns	output load: 5 pF
t_TX_HD	Hold time for output signals	1.2	-	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	1.0	-	ns	
t_RX_HD	Hold time for input signals	1.0	-	ns	

3.8.3 MII Interface (25 Mhz)

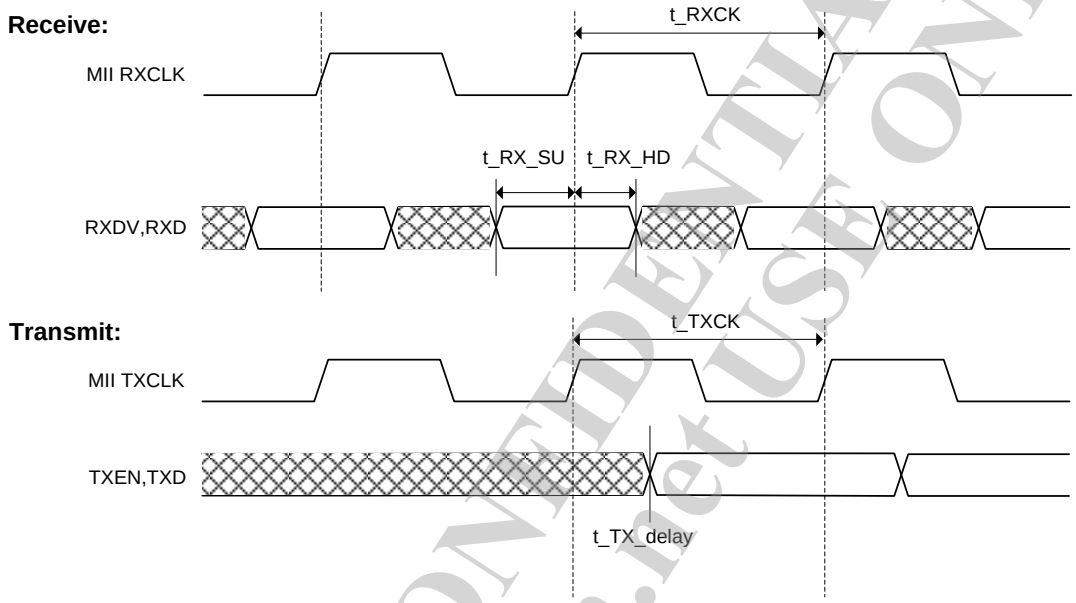


Figure 3-5 MII Timing

Table 3-9 MII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_delay	Delay to output signals (e.g. GE0_TXD*, GE0_TXEN)	6	22	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	10	-	ns	
t_RX_HD	Hold time for input signals	5	-	ns	

Note: For 25 Mhz TXCLK & RXCLK

3.8.4 RvMII Interface (PHY Mode MII Timing) (25 Mhz)

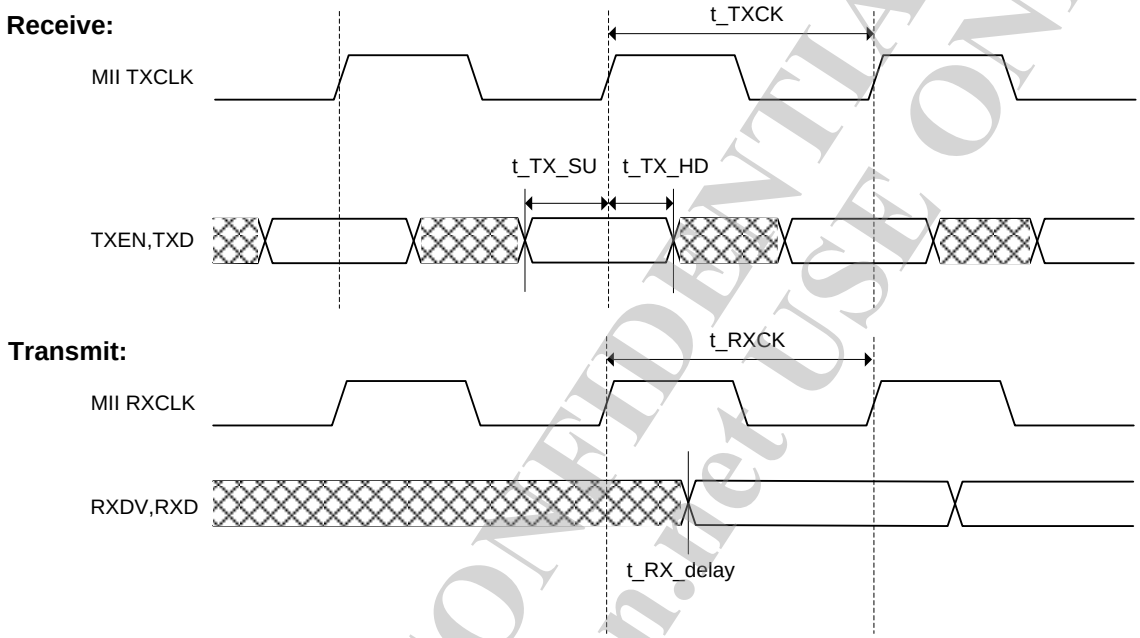


Figure 3-6 RvMII Timing

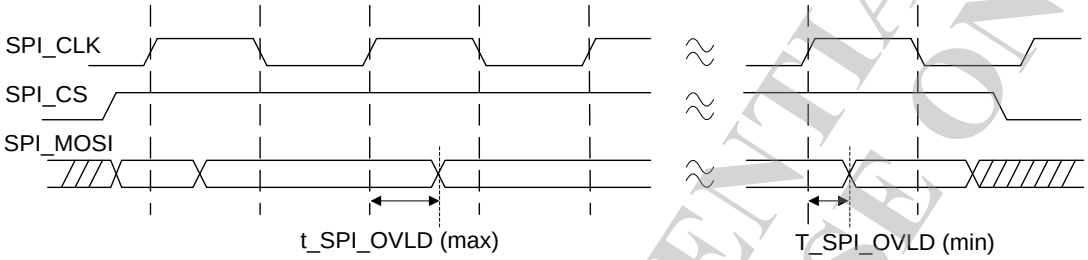
Table 3-10 RvMII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_RX_delay	Delays to output signals (e.g. GE0_TXD*, GE0_TXEN)	5	25	ns	output load: 5 pF
t_TX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	15	-	ns	
t_TX_HD	Hold time for input signals	6	-	ns	

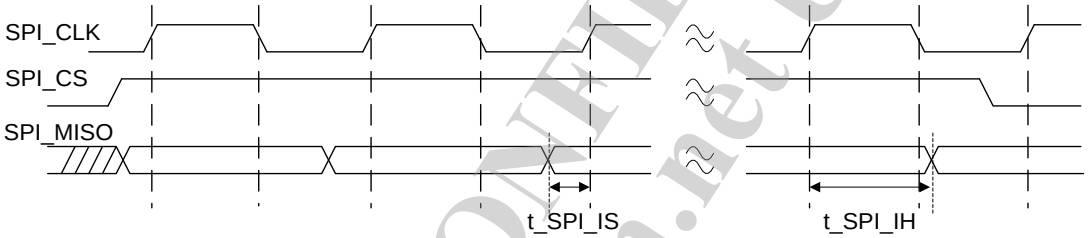
Note: For 25 Mhz TXCLK & RXCLK

3.8.5 SPI Interface

Write operation (driven by clock rising edge)



Read operation (Driven by clock rising edge (slave-device) and latched by clock rising edge)



NOTE: 1) SPI_CLK is a gated clock.
2) SPI_CS is controlled by software

Figure 3-7 SPI Timing

Table 3-11 SPI Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_SPI_IS	Setup time for SPI input	6.0	-	ns	
t_SPI_IH	Hold time for SPI input	-1.0	-	ns	
t_SPI_OVLD	SPI_CLK to SPI output valid	-2.0	3.0	ns	output load: 5 pF

3.8.6 I2S Interface

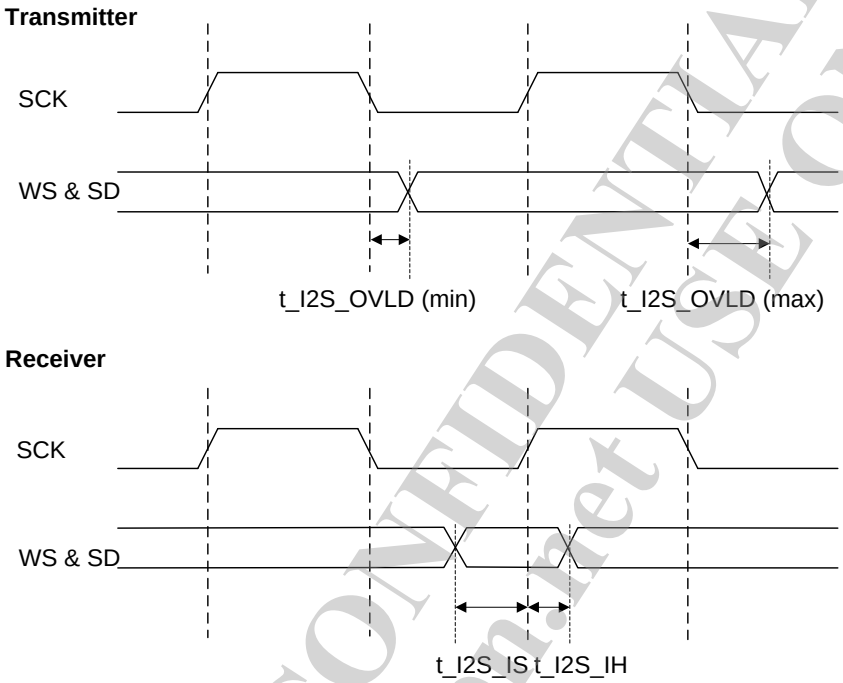


Figure 3-8 I2S Timing

Table 3-12 I2S Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_I2S_IS	Setup time for I2S input (data & WS)	3.5	-	ns	
t_I2S_IH	Hold time for I2S input (data & WS)	0.5	-	ns	
t_I2S_OVLD	I2S_CLK to I2S output (data & WS) valid	2.5	10.0	ns	output load: 5 pF

3.8.7 PCM Interface

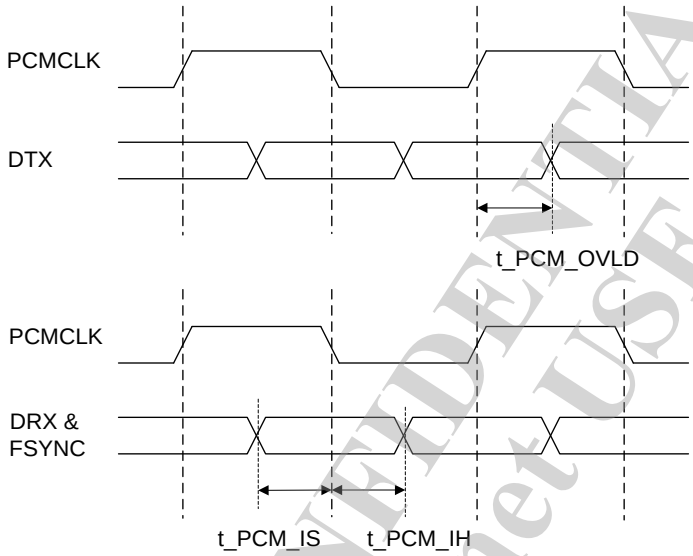


Figure 3-9 PCM Timing

Table 3-13 PCM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_PCM_IS	Setup time for PCM input to PCM_CLK fall	3.0	-	ns	
t_PCM_IH	Hold time for PCM input to PCM_CLK fall	1.0	-	ns	
t_PCM_OVLD	PCM_CLK rise to PCM output valid	10.0	35.0	ns	output load: 5 pF

3.8.8 I2C Interface

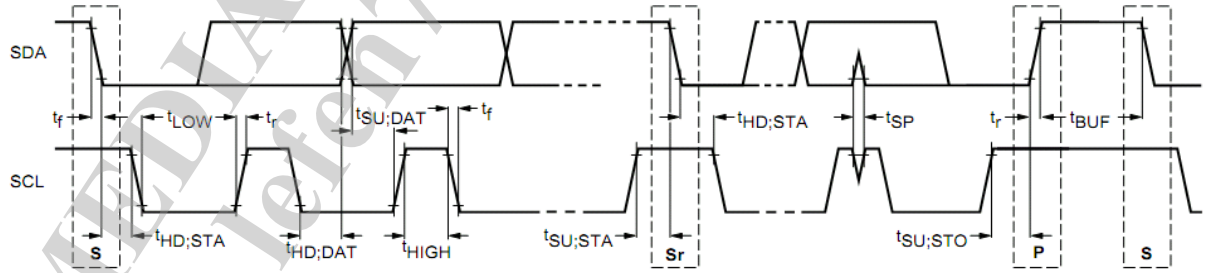


Figure 3-10 I2C Timing

Table 3-14 I2S Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
fSCL	SCL clock frequency	0	100	kHz	

Symbol	Description	Min	Max	Unit	Remark
tBUF	Bus free time between a STOP and START condition	4.7		us	
tHD	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4		us	
tLOW	LOW period of the SCL clock	4.7		us	
tHIGH	HIGH period of the SCL clock	4		us	
tSU:STA	Setup time for a repeated START condition	4.7		us	
Thd:DAT	Data hold time:	5		us	
tSU:DAT	Data setup time	250		ns	
tr	Rise time of both SDA and SCL signals		1000	ns	
tf	Fall time of both SDA and SCL signals		300	ns	
tSU:STO	Setup time for STOP condition	4		us	

3.8.9 SDIO Interface

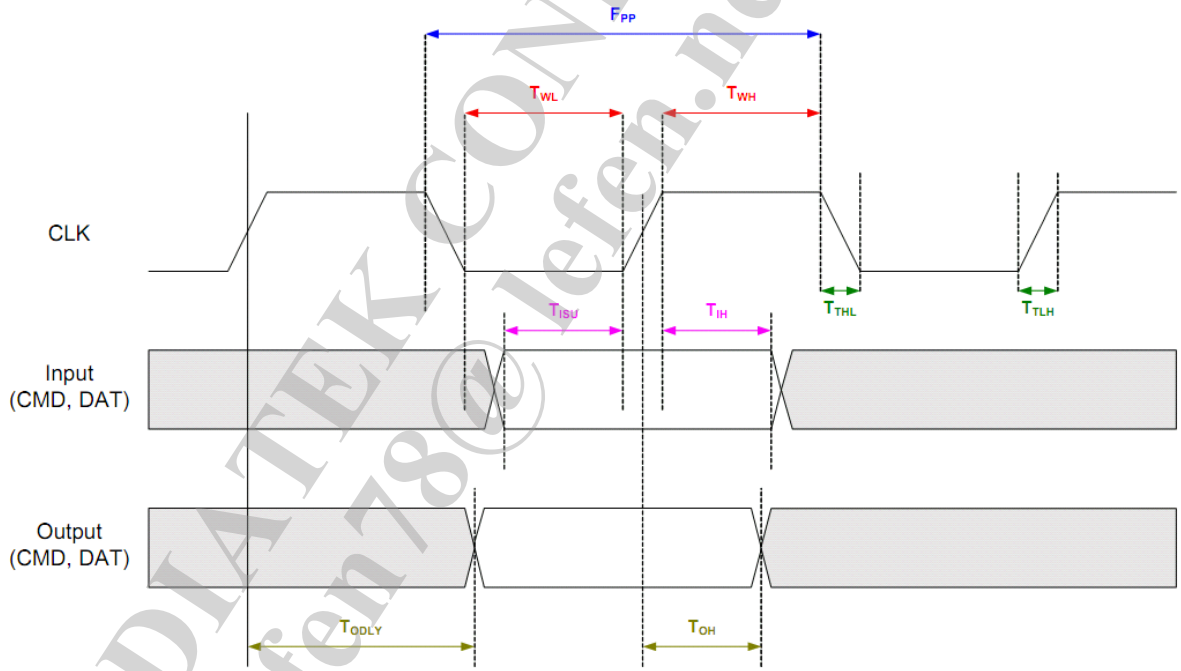


Figure 3-11 SDIO Timing

Table 3-15 SDIO Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
fPP	Clock frequency data transfer mode	0	50	MHz	
tWL	Clock low	7		ns	
tWH	Clock high	7		ns	
tTLH	Clock rise		10	ns	

Symbol	Description	Min	Max	Unit	Remark
tTHL	Clock fll		10	ns	
tISU	Input setup	6		ns	
tIH	Input hold	2		ns	
tOH	Output hold	2.5		ns	
tO_DLY(max)	Output dellay time	0	50	ns	

3.8.10 NAND Flash Interface (Samsung Compatibel Device)

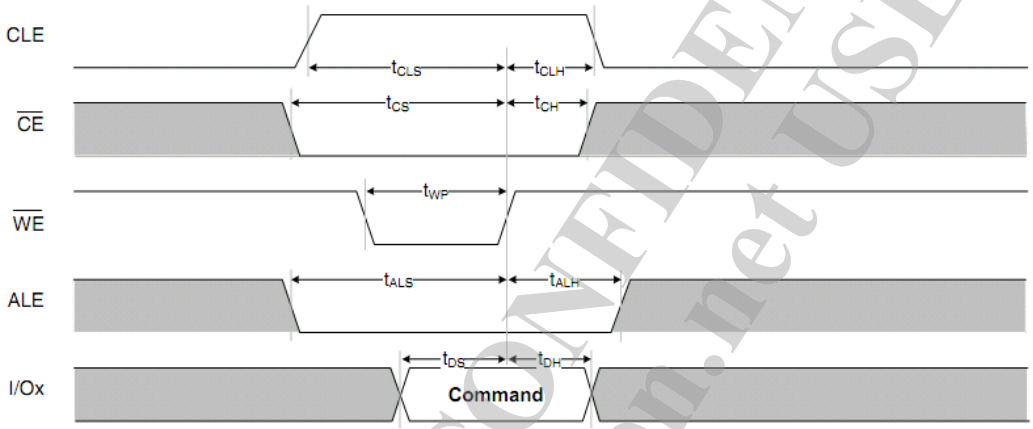


Figure 3-12 NAND Flash Command Timing

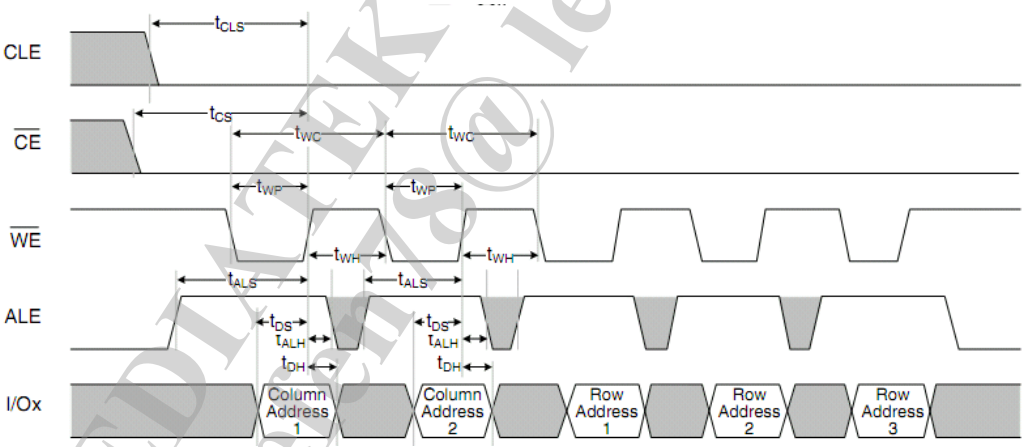


Figure 3-13 NAND Flash Address Latch Timing

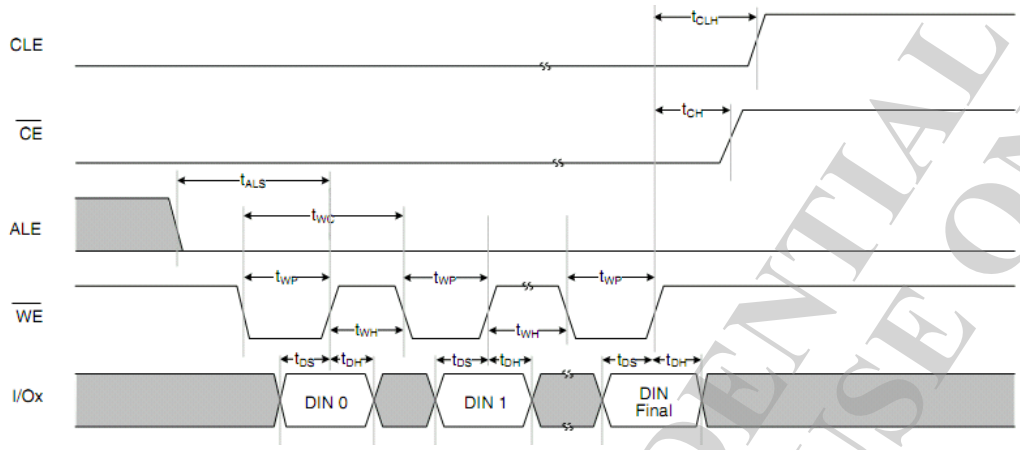


Figure 3-14 NAND Flash Write Timing

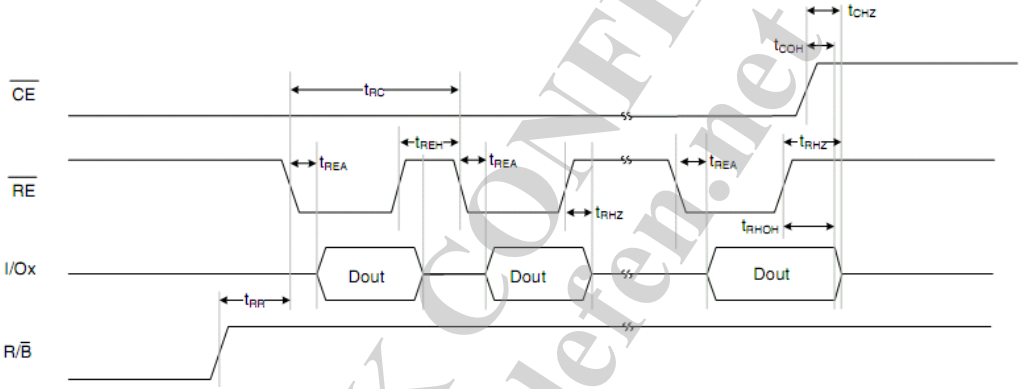


Figure 3-15 NAND Flash Read Timing

Table 3-16 NAND Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCLS	CLE setup time	15	-	ns	
tCLH	CLE hold time	5		ns	
Tcs	CE setup time	20		ns	
tCH	CE hold time	5		ns	
tWP	WE pulse width	15		ns	
tALS	ALE setup time	15		ns	
tALH	ALE hold time	5		ns	
tDS	Data setup time	15		ns	
tDH	Data hold time	5		ns	
tWC	Write cycle time	30		ns	
tWH	WE high hold time	10		ns	
tRR	Ready to RE low	20		ns	
tWB	WE high to busy		100	ns	
tRC	Read cycle time	30		ns	

Symbol	Description	Min	Max	Unit	Remark
tREA	RE access time		20	ns	
tRHZ	RE high to output Hi-Z		100	ns	
tCHZ	CE high to output Hi-Z		30	ns	
tRHOH	RE high to output hold	15		ns	
tCOH	CE high to output hold	15		ns	
tREH	RE high hold time	10		ns	

3.8.11 Power On Sequence

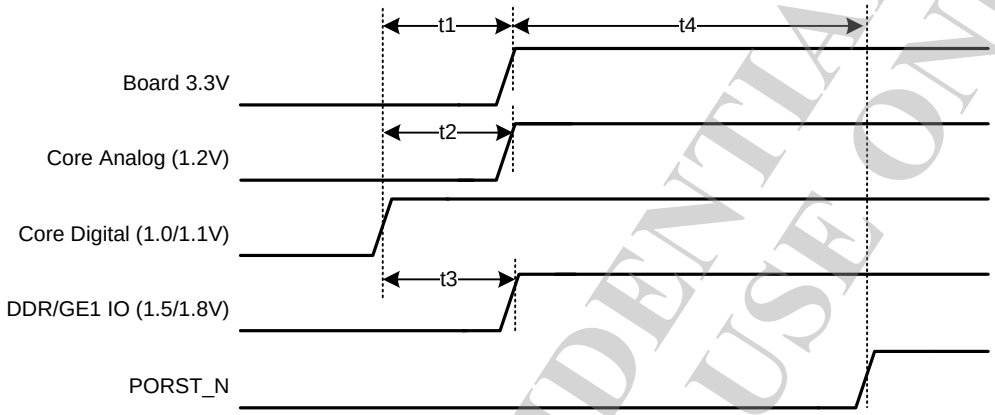


Figure 3-16 Power ON Sequence

Table 3-17 Power ON Sequence Diagram Key

Symbol	Description	Min	Max	Unit
t1	3.3V power on to digital core power	1	-	ms
t2	1.2V power on to digitalcore power	1	-	ms
t3	1.5/1.8V power on to digitalcore power	1	-	ms
t4	3.3V power on to PORST_N de-assertion	100	-	ms

4. Package Information

4.1 Dimensions - TFBGA (11.7 mm x 13.6 mm)

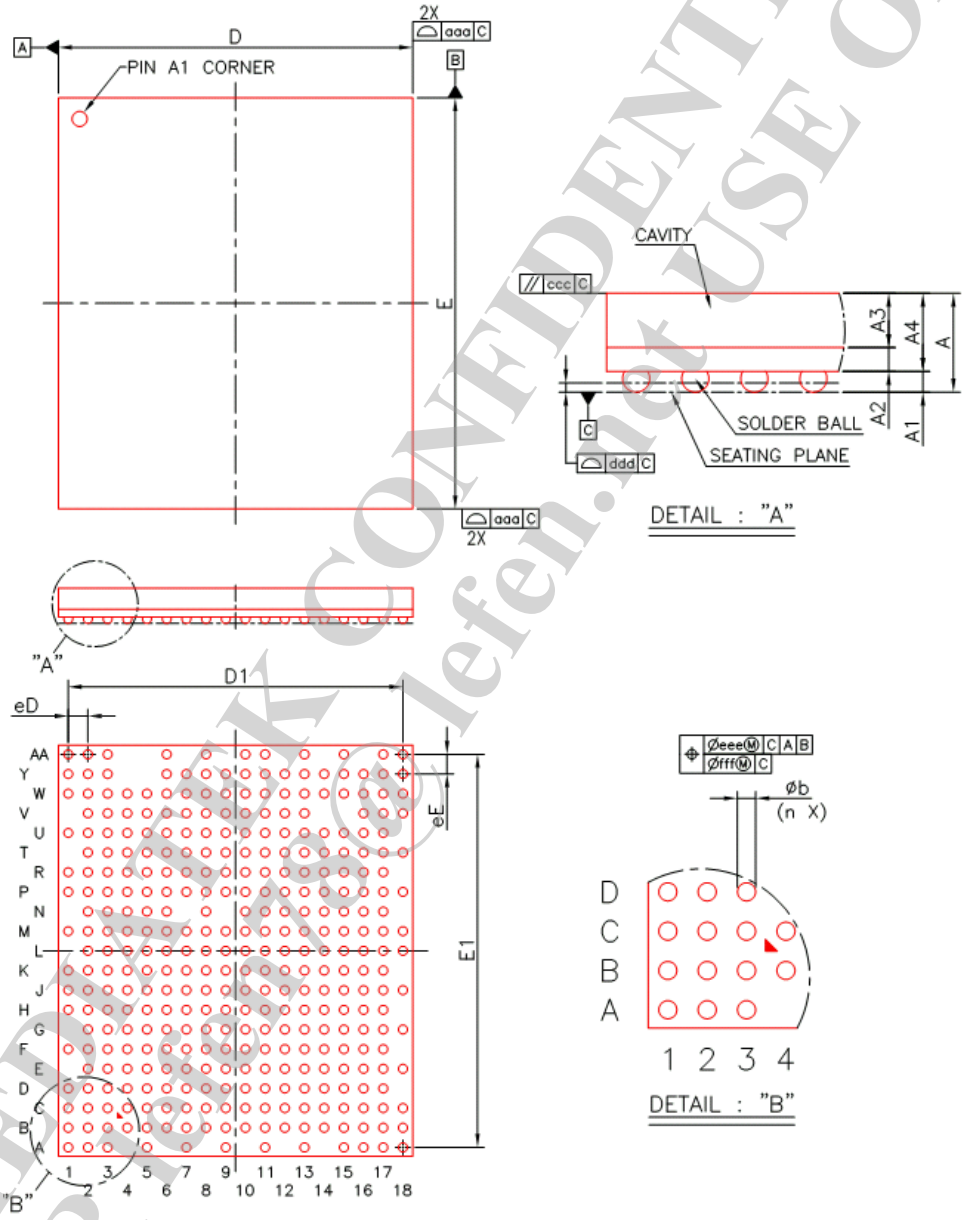


Figure 4-1 Package Dimension

4.1.1 Diagram Key

Table 4-1 Package Diagram Key

Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			LFBGA		
Body Size	X	D	11.60	11.70	11.80
	Y	E	13.50	13.60	13.70
Ball Pitch	X	eD		0.65	
	Y	eE		0.65	
Total Thickness		A	–	–	1.30
Mold Thickness		A3		0.70 Ref.	
Substrate Thickness		A2		0.26 Ref.	
Substrate+Mold Thickness		A4	0.90	0.96	1.02
Ball Diameter				0.30	
Stand Off		A1	0.16	0.21	0.26
Ball Width		b	0.25	0.30	0.35
Package Edge Tolerance		aaa		0.10	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.08	
Ball Count		n		346	
Edge Ball Center to Center	X	D1		11.05	
	Y	E1		13.00	

NOTE:
1. Controlling dimensions are in millimeters.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Special characteristics C class: bbb, ddd.
5. The pattern of pin 1 fiducial is for reference only.

4.2 Reflow Profile Guideline

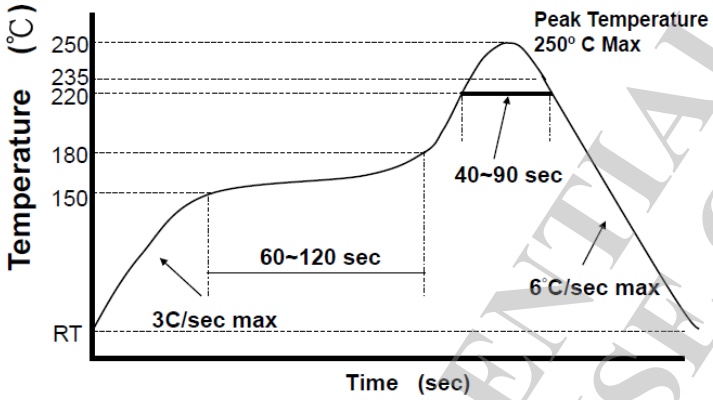


Figure 4-2 Reflow profile

Notes:
1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

4.3 Top Marking

MT7621S: Part number
YYWW : Date code
: Internal control code
LLLLLLLLL : Lot number
"." : Pin #1 dot

Figure 4-3 Top marking

4.4 Ordering Information

Part Number	Package (Green/RoHS Compliant)	Ambient Temperature
MT7621IS	11.7 x 13.6, 346-balls TFBGA	-40 ~ 85 ℃
MT7621S	11.7 x 13.6, 346-balls TFBGA	-20 ~ 55 ℃

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5. Abbreviations

Abbrev.	Description
AC	Access Category
ACK	Acknowledge/ Acknowledgement
ACPR	Adjacent Channel Power Ratio
AD/DA	Analog to Digital/Digital to Analog converter
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AGC	Auto Gain Control
AIFS	Arbitration Inter-Frame Space
AIFSN	Arbitration Inter-Frame Spacing Number
ALC	Asynchronous Layered Coding
A-MPDU	Aggregate MAC Protocol Data Unit
A-MSDU	Aggregation of MAC Service Data Units
AP	Access Point
ASIC	Application-Specific Integrated Circuit
ASME	American Society of Mechanical Engineers
ASYNC	Asynchronous
BA	Block Acknowledgement
BAC	Block Acknowledgement Control
BAR	Base Address Register
BBP	Baseband Processor
BGSEL	Band Gap Select
BIST	Built-In Self-Test
BSC	Basic Spacing between Centers
BJT	
BSSID	Basic Service Set Identifier
BW	Bandwidth
CCA	Clear Channel Assessment
CCK	Complementary Code Keying
CCMP	Counter Mode with Cipher Block Chaining Message Authentication Code Protocol
CCX	Cisco Compatible Extensions
CF-END	Control Frame End
CF-ACK	Control Frame Acknowledgement

Abbrev.	Description
CLK	Clock
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSR	Control Status Register
CTS	Clear to Send
CW	Contention Window
CWmax	Maximum Contention Window
CWmin	Minimum Contention Window
DAC	Digital-To-Analog Converter
DCF	Distributed Coordination Function
DDONE	DMA Done
DDR	Double Data Rate
DFT	Discrete Fourier Transform
DIFS	DCF Inter-Frame Space
DMA	Direct Memory Access
DSP	Digital Signal Processor
DW	DWORD
EAP	Expert Antenna Processor
EDCA	Enhanced Distributed Channel Access
EECS	EEPROM chip select
EEDI	EEPROM data input
EEDO	EEPROM data output
EEPROM	Electrically Erasable Programmable Read-Only Memory
eFUSE	electrical Fuse
EESK	EEPROM source clock
EIFS	Extended Inter-Frame Space
EIV	Extend Initialization Vector
EVM	Error Vector Magnitude
FDS	Frequency Domain Spreading
FEM	Front-End Module
FEQ	Frequency Equalization
FIFO	First In First Out
FSM	Finite-State Machine
GF	Green Field
GND	Ground
GP	General Purpose

Abbrev.	Description
GPO	General Purpose Output
GPIO	General Purpose Input/Output
HCCA	HCF Controlled Channel Access
HCF	Hybrid Coordination Function
HT	High Throughput
HTC	High Throughput Control
ICV	Integrity Check Value
IFS	Inter-Frame Space
iNIC	Intelligent Network Interface Card
IV	Initialization Vector
I^2C	Inter-Integrated Circuit
I^2S	Integrated Inter-Chip Sound
I/O	Input/Output
IPI	Idle Power Indicator
IQ	In phase/Quadrature phase
JEDEC	Joint Electron Devices Engineering Council
JTAG	Joint Test Action Group
kbps	kilo (1000) bits per second
KB	Kilo (1024) Bytes
LDO	Low-Dropout Regulator
LDODIG	LDO for DIGital part output voltage
LED	Light-Emitting Diode
LNA	Low Noise Amplifier
LO	Local Oscillator
L-SIG	Legacy Signal Field
MAC	Medium Access Control
MCU	Microcontroller Unit
MCS	Modulation and Coding Scheme
MDC	Management Data Clock
MDIO	Management Data Input/Output
MEM	Memory
MFB	MCS Feedback
MFS	MFB Sequence
MIC	Message Integrity Code
MIMO	Multiple-Input Multiple-Output
MLNA	Monolithic Low Noise Amplifier
MM	Mixed Mode

Abbrev.	Description
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPDU	MAC Protocol Data Units
MSB	Most Significant Bit
NAV	Network Allocation Vector
NAS	Network-Attached Server
NAT	Network Address Translation
NDP	Null Data Packet
NVM	Non-Volatile Memory
ODT	On-die Termination
Oen	Output Enable
OFDM	Orthogonal Frequency-Division Multiplexing
OSC	Open Sound Control
PA	Power Amplifier
PAPE	Provider Authentication Policy Extension
PBC	Push Button Configuration
PBF	Packet Buffer
PCB	Printed Circuit Board
PCF	Point Coordination Function
PCM	Pulse-Code Modulation
PHY	Physical Layer
PIFS	PCF Interframe Space
PLCP	Physical Layer Convergence Protocol
PLL	Phase-Locked Loop
PME	Physical Medium Entities
PMU	Power Management Unit
PN	Packet Number
PROM	Programmable Read-Only Memory
PSDU	Physical layer Service Data Unit
PSI	Power supply Strength Indication
PSM	Power Save Mode
PTN	Packet Transport Network
QoS	Quality of Service
RDG	Reverse Direction Grant
RAM	Random Access Memory
RF	Radio Frequency
	Reduced Gigabit Media Independent Interface

Abbrev.	Description
RH	Relative Humidity
RoHS	Restriction on Hazardous Substances
ROM	Read-Only Memory
RSSI	Received Signal Strength Indication (Indicator)
RTS	Request to Send
RvMII	Reverse Media Independent Interface
Rx	Receive
RXD	Received Data
RXINFO	Receive Information
RXWI	Receive Wireless Information
S	Stream
SDXC	Secure Digital eXtended Capacity
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SEC	Security
SGI	Short Guard Interval
SIFS	Short Inter-Frame Space
SoC	System-on-a-Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSCG	Spread Spectrum Clock Generator
STBC	Space–Time Block Code
SW	Switch Regulator
TA	Transmitter Address
TBTT	Target Beacon Transmission Time
TDLS	Tunnel Direct Link Setup

Abbrev.	Description
TKIP	Temporal Key Integrity Protocol
TRSW	Tx/Rx Switch
TSF	Timing Synchronization Function
TSSI	Transmit Signal Strength Indication
Tx	Transmit
TxBF	Transmit Beamforming
TXD	Transmitted Data
TXDAC	Transmit Digital-Analog Converter
TXINFO	Transmit Information
TXOP	Opportunity to Transmit
TXWI	Tx Wireless Information
UART	Universal Asynchronous Rx/ Tx
USB	Universal Serial Bus
UTIF	Universal Test Interface
VGA	Variable Gain Amplifier
VCO	Voltage Controlled Amplifier
VIH	High Level Input Voltage
VIL	Low Level Input Voltage
VoIP	Voice over IP
WCID	Wireless Client Identification
WEP	Wired Equivalent
WI	Wireless Information
WIV	Wireless Information Valid
WMM	Wi-Fi Multimedia
WPA	Wi-Fi Protected Access
WPDMA	Wireless Polarization Division Multiple Access
WS	Word Select

6. Revision History

Rev	Date	Description
0.0	2013/4/29	Initial Release
0.1	2013/6/10	Preliminary release Add package information, power on sequence
0.2	2013/9/30	Add power data, switch feature
0.3	2013/11/5	Update Main Feature table
0.4	2013/12/16	Add eMMC into feature list Update pin description section for DDR2/3 Update power on sequence section Update VDD11 operating range

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