A 500 nA Quiescent, 100 mA Maximum Load CMOS Low-dropout Regulator

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***Abstract*—Ultra low quiescent, wide output current range low-dropout regulators (LDO) are in high demand in portable applications to extend battery lives. This paper presents a 500 nA quiescent, 0 to 100 mA load, 3.5-7 V input to 3 V output LDO in a digital 0.35 μm 2P3M CMOS technology. The challenges in designing with nano-ampere of quiescent current are discussed, namely the leakage, the parasitics, and the excessive DC gain. CMOS super source follower voltage buffer and input excessive gain reduction are then proposed. The LDO is internally compensated using Ahuja method with a minimum phase margin of 55° across all load conditions. The maximum transient voltage variation is less than 150 and 75 mV when used with 1 and 10 μF external capacitor. Compared with existing work, this LDO achieves the best transient figure-of-merit with close to best dynamic current efficiency (maximum-to-quiescent current ratio).**

I. Introduction

Extremely low quiescent current power management circuits are highly desirable for battery-powered applications, as any current drained from the battery would encroach into the remaining battery capacity. But unlike many low power applications like passive RFIDs [1], portable multimedia electronics, such as smart phones, laptops, and tablets, require their power supply modules to source a much wider output current range to support the ever increasing functionality and processing power in the gadgets.

Low-dropout regulators (LDOs) are one of the most widely used power supply modules for noise-sensitive analog [2]. The challenge in designing an ultra-low quiescent current, wide output current range LDO in a mainstream CMOS process is two-folded: on one hand, the leakage current from the power MOSFET, which needs to be sized large enough to source the maximum load current, becomes significant. On the other hand, low power analog design often leads to larger parasitics. Combined with the need for a large pass element, the compensation of the LDO proves difficult.

Prior studies on extremely low power, nanoampere quiescent LDOs have been reported. A 110 nA voltage regulator was presented in [1] as a post-regulator in a passive RFID tag. The maximum load current, however, is only 25 μA. A transient-enhanced, 200 mA maximum load CMOS LDO was proposed in [2], but the quiescent current at zero load was 20 μA. Partially or fully digital implementation of an LDO have been reported as a viable alternative to achieve ultra-low quiescent current and maximum load simultaneously. Digital error amplifier [3] and shift register controlled switch-array [4] have been proposed, but they either need common-voltage control circuits to work properly [3], or suffer from different amount of output ripple based on the shift register's frequency [4].

This paper presents a 500 nA quiescent, 0 to 100 mA load, dynamically biased analog low-dropout regulator in 0.35 μm CMOS technology. The LDO adopts a dynamically biased CMOS super source follower [5] as the buffer between the error amplifier and the pass element. It also takes advantage of input source-degeneration to trade excessive DC gain for stability [6] at nanopower settings.

II. Nano-ampere Challenges and Design

A general analog LDO usually consists of three parts: an error amplifier, a pass element, and a feedback network. Though this configuration works well when sourcing mili-amperes of load with micro-amperes of quiescent current (I_Q), it faces great challenges when I_Q needs to be scaled down to nano-ampere range but the maximum load requirement remains intact.

This section will discuss the nano-ampere I_Q challenges for each block in a bottom-up fashion, namely the leakage, the parasitics, and the excessive gain. Super source follower and input degeneration are then proposed as a viable solution.

A. Leakage of the Pass Element

With nano-amperes of total quiescent current budget, the leakage from the pass element cannot be ignored. In order to source the maximum load current with a low dropout voltages, the pass element has to be sized reasonable large to achieve the target $R_{ds,on}$, as indicated by Eq. 1

$$R_{ds,on} = \frac{1}{\mu_p C_{ox} W/L(V_{GS} - V_{TH})} \quad (1)$$

Meanwhile, minimum channel length L_{min} is often used to reduce the pass element size and its gate parasitics, as $C_{gate} \propto W \cdot L$. However, today's advanced sub-micron and

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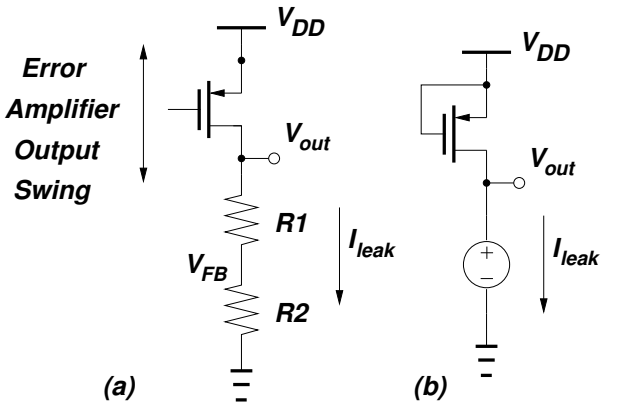

Fig. 1. Test bench for the pass element's off-state leakage

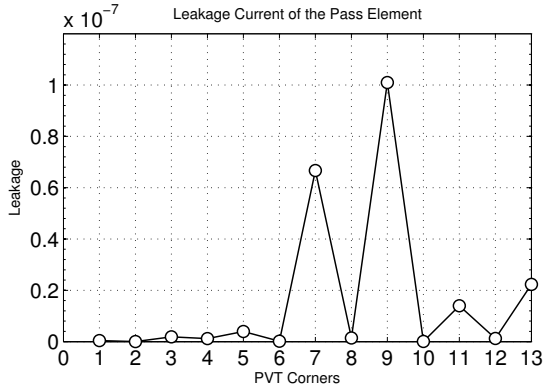

Fig. 2. Off-state leakage in different PVT corners

nanometer technologies are increasingly leaky. The off-state drain current $I_{D,off}$ for a large MOSFET array can easy reach nano-ampere range under worst-case process, voltage, and temperature (PVT) corner.

This leakage can be found using the test bench in Fig. 1 (b). Depending on the error amplifier's output swing, the output current can be completely cut off with various V_{SG}, as seen in Fig. 1 (a). Assume that the LDO is in regulation at dropout and $V_{SG} = 0$, the $I_{leak,max}$ can be found for different transistor ratios. In this 0.35 μm CMOS process, a 30000/1.3 PMOS has $I_{leak,max}$ of 100 nA at hot temperature and strong process corner, as shown in Fig. 2. The resistive network R_1, R_2 is therefore designed to conduct as least 100 nA quiescent current. Further reduction in the quiescent current will cause the output voltage to drift toward the supply V_{DD} at zero load.

It is important to point out that this LDO is designed to be always ON with no pre-knowledge of load changes. If a load change indication signal is available, I_{leak} can be reduced effectively by power gating [1].

B. CMOS Super Source Follower Buffer

Due to the large parasitic capacitance at the gate of the pass element, a voltage buffer is usually inserted between the error amplifier and the power MOSFET, as shown in Fig. 3 (a) and (b) [2], [7]. The buffer isolates the capacitance from the high impedance at the error amplifier output, which will extends the bandwidth of the LDO. It also increases the slew rate of the error amplifier, further improving the LDO's transient response.

[1]It can be implemented as simple as a voltage controlled switch in series of R_1, R_2 to block I_{leak}.

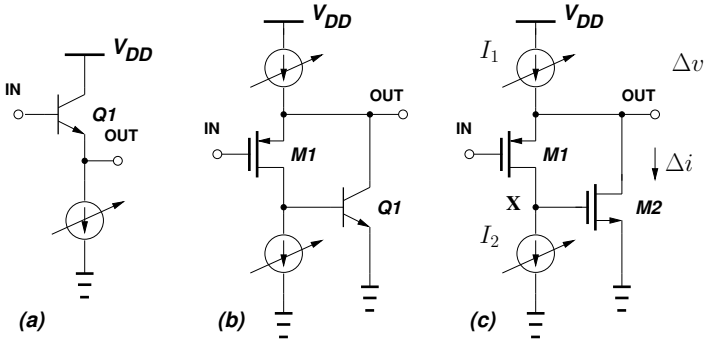

Fig. 3. Existing and Proposed Voltage Buffers in LDO

The emitter follower buffer in Fig. 3 (a) [7] , however, needs a finite bias current I_b that may worsen the offset in the preceding error amplifier. The PMOS source follower buffer in Fig. 3 (b) eliminates I_b and and reduces r_o through feedback. The output impedance of the buffer is approximately [2]

$$r_o = \frac{1}{g_{m1}(1+\beta)} \tag{2}$$

As such, both buffers require bipolar transistors. Though BiCMOS technologies provide high performance bipolar and CMOS transistors, the construction of NPN BJTs in a CMOS technology usually require a twin-well process. Furthermore, the vertical parasitic NPN may not have a high enough forward current gain β to reduce the output impedance effectively, as seen in Eq. 2.

This paper proposes replacing the feedback NPN transistor Q_1 in Fig. 3 (b) with an NMOS, leading to an all MOS structure also known as a super source follower [5]. Its output impedance can be derived through inspection. If the body effects can be ignored and $r_{o1}, r_{o2} \to \infty$, a voltage step Δv applied at the output will change the voltage at node X to

$$v_x = g_{m1} r_{o1} \Delta v \tag{3}$$

$$\Delta i = g_{m2} v_x \tag{4}$$

$$\therefore r_o = \frac{\Delta v}{\Delta i} = \frac{1}{g_{m1}} \frac{1}{g_{m2} r_{o1}} \tag{5}$$

Eq. 5 is in agreement with a detailed analysis based on the small-signal equivalent circuit [5]. Finally, the choice of I_2 given the the total quiescent current budget I_1 is not trivial. It can be shown that $I_2 = 1/2 I_1$ achieves the minimal r_o. Assume that M_1, M_2 are in the saturation region [2]

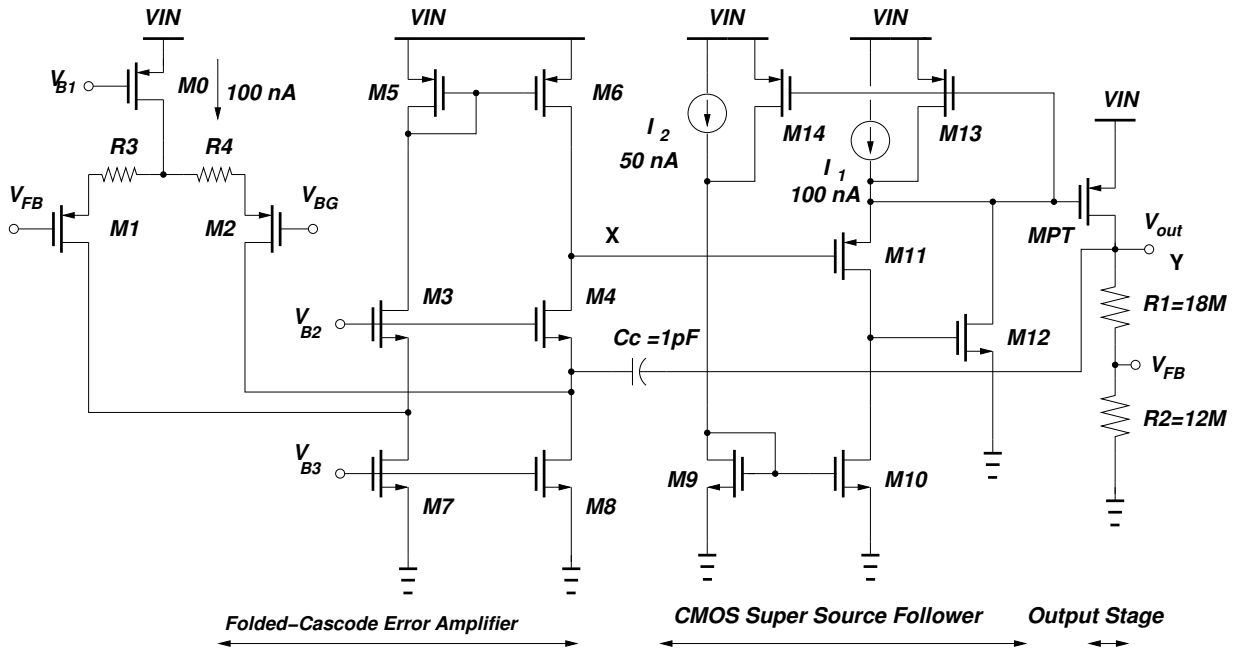

Fig. 4. Schematics of the Proposed LDO

$$g_{m1} \propto \sqrt{I_{D1}}, g_{m2} \propto \sqrt{I_{D2}} \tag{6}$$

$$r_o \propto \frac{1}{g_{m1}g_{m2}} \propto \frac{1}{\sqrt{I_{D1}I_{D2}}} \tag{7}$$

$$\because \sqrt{I_{D1}I_{D2}} \leq \frac{I_{D1}+I_{D2}}{2} = I_1/2 \tag{8}$$

$$\therefore r_o \geq \frac{1}{g_{m1}^2 r_{o1}} \propto \frac{4}{I_1^2 r_{o1}} \text{ when } I_{D1} = I_{D2} \tag{9}$$

C. Compensation and Excessive Gain Reduction

The full schematic of the proposed LDO is shown in Fig. 4. In order to source output current over six orders of magnitude (from $1\mu A$ to 100 mA), a folded cascode error amplifier is chosen to maximize the output swing of the error amplifier. An external capacitor of $1\mu F$ with no minimum ESR requirement is placed at the LDO output to smooth the transient response.

The LDO is compensated internally using the Ahuja method [1], [2]. Thanks to the low output impedance of the proposed buffer, the pole at the gate of the pass element is pushed to high frequency. Thus, there are only two poles in the LDO structure located at the output of the error amplifier (node X) and the output of the LDO (node Y). They are given by

$$p_{EA} = 1/(r_{o1}C_1) \tag{10}$$

$$p_{out} = 1/(R_{out}C_{out}) \tag{11}$$

where r_{o1} is output impedance of the error amplifier, C_1 is the total parasitic capacitance at node X, R_{out} is the output impedance of the LDO, and C_{out} is the total capacitance at node Y.

Depending on the load current, the two poles shift positions relatively. At light load, p_{out} is the dominant pole, and the bandwidth is very limited such that p_{EA} is beyond the unity gain frequency (UGF). At heavy load, however, the Ahuja compensation takes effect. The increased gain in the pass element pushes p_{EA} to a much lower frequency by enhancing C_1 with a Miller capacitance $(g_{mp}R_{out})C_c$. The enhanced gain also pushes p_{out} to a higher frequency beyond UGF by lowering R_{out} to $1/g_{mp}$. As a result, an equivalent single-pole system is always accomplished regardless of the output current. The worst-case stability resides between light load and heavy load with a minimum phase margin of [2]

$$PM_{min} = \frac{4}{g_{m1}r_{o1}} \cdot \frac{C_c}{C_1} \tag{12}$$

From Eq. 12, it can be seen that any nano-ampere quiescent current design will be very challenging. Low power design in most CMOS technologies will require longer channel length for transistors (for small W/L). This would lead to high output impedance in r_{o1} and large parasitics in C_1.

As a result, excessive gain reduction [6] is applied to this design through input g_{m1} degeneration using resistors R_3, R_4. Resistive degeneration was preferred over simply increasing the channel length of M_1, M_2 because the later would further increase the transistors' output impedance, making the compensation more difficult.

III. Simulation Results

The proposed LDO was designed and simulated in a 0.35 μm 2P3M CMOS process with breakdown voltage of 7 V.

[2]The same conclusion can be reached if both are in the subthreshold region. Simply replace $g_m \propto \sqrt{I_D}$ with $g_m \propto I_D$.

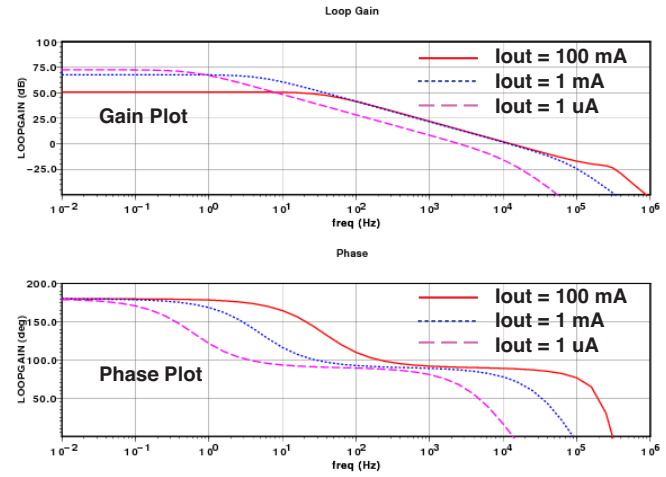

Fig. 5. LDO Loop Gain at Different Output Load Conditions. $C_{out} = 1\mu F$

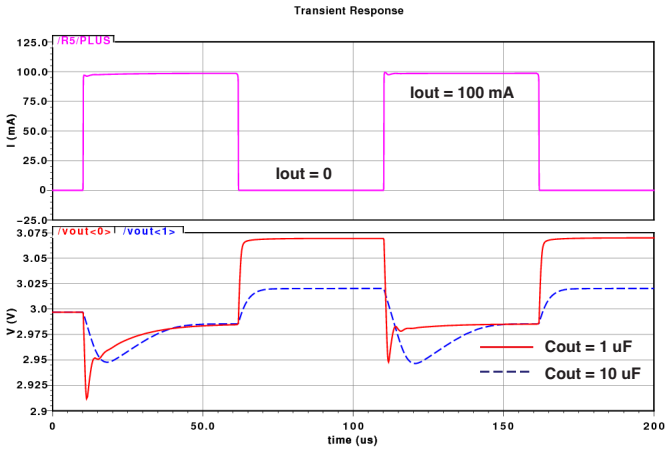

Fig. 6. Transient Response of the Proposed LDO (a) $C_{out} = 1\mu F$ (b) $C_{out} = 10\mu F$. V_{in}=3.5 V, ESR=5 $m\Omega$, and $t_{rise} = 1\mu s$ for both cases.

The LDO is designed to operate under 3.3 to 7 V input and regulates 3 V output. The output current range is from 0 to 100 mA. At zero load, the LDO core consumes only 450 nA I_Q, with an additional 50 nA used for biasing. At 100 mA load, however, I_Q went up to as much as 350 μA thanks to the dynamic biasing in the proposed buffer.

The stability of the LDO under different load conditions were verified. Fig. 5 shows the magnitude and phase of the loop gain when I_{out} is 1 μA, 1 mA, and 100 mA respectively. As predicted in Section II-C, an equivalent single-pole system was achieved with worse-case stability at moderate loads (around 1 mA). The minimum phase margin was around 55°.

The load transient response with different external capacitor value was also simulated. The total output voltage error, including undershot, overshot, and DC error was less than 150 mV and 75 mV for C_{out} of 1 and 10 μF. The settling time was less than 10 μs and 30μs, respectively.

Finally, the performance of the proposed LDO is summarized in Table I. The maximum-to-quiescent current ratio I_{max}/I_Q is introduce to benchmark LDO's dynamic current

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH EXISTING WORK

	[1]	[2]	[3]	[4]	This Work
Year	2006	2007	2008	2010	2011
Technology	CMOS 0.15 um	CMOS 0.35 um	CMOS 0.35 um	CMOS 65 nm	CMOS 0.35 um
V_{in} (V)	1.25-2.2	2-7	0.9	0.5	3.3-7
V_{out} (V)	1.25	1.8	0.5	0.45	3
I_{max} (mA)	0.025	200	50	0.2	100
I_Q (μA)	0.11	20	0.103	2.7	0.5
I_{max}/I_Q (10^3)	0.23	10	485	0.074	200
ΔV_{out} (mV)	20	54	300	70	150
C_L (μF)	0.00025	1	cap-free	0.1	1
T_r (μs)	0.2	0.27	N/A	35	1.5
FOM (ns)	0.88	0.027	N/A	472.5	0.0075

efficiency that is critical for battery-powered applications. A figure of merit (FOM) = $T_r \times I_Q/I_{max}$ where $T_r = (C_L \Delta V_{out})/I_{max}$ commonly used [2] to compare the transient performance of an LDO is also adopted. The smaller the FOM, the better transient response an LDO achieves. With the second highest dynamic current efficiency (I_{max}/I_Q ratio), this work achieves the best transient response.

IV. CONCLUSION

This paper presents an ultra-low quiescent current, low-dropout regulator in 0.35 μm CMOS technology. The LDO dissipates only 500 nA quiescent current at zero load, and it can source up to 100 mA of output current. CMOS super source follower and excessive DC gain reduction were proposed, in addition to Ahuja compensation, which guaranteed stability across all load conditions. The LDO also achieved optimum transient response with next to best maximum-to-quiescent current ratio.

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