Analog Integr Circ Sig Process (2010) 63:107–112
DOI 10.1007/s10470-009-9441-4

MIXED SIGNAL LETTER

Sleep-mode ready, area efficient capacitor-free low-dropout regulator with input current-differencing

John Hu · Wei Liu · Mohammed Ismail

Received: 14 July 2009 / Revised: 9 September 2009 / Accepted: 6 December 2009 / Published online: 31 December 2009

Abstract This paper proposes an input current-differencing technique in designing a capacitor-free low-dropout regulator to simultaneously achieve sleep-mode efficiency and silicon real estate saving. With no minimum output current required to be stable, the regulator could greatly improve SoC efficiency during standby, which is extremely attractive for battery powered applications. Designed in TSMC 0.18-μm CMOS technology, it regulates 1.8–1.2 V supply down to 1 V with 100 mA maximum output current and can drive up to 100 pF of load parasitic capacitance. Compared with prior arts with the same sleep-mode compatibility and similar output current range, it reduces the on-chip compensation capacitance from 21 to 4.5 pF.

Keywords Sleep-mode ready · Area efficient · Low-dropout regulator · Capacitor-free · CMOS · Input current-differencing

1 Introduction

Industry is pushing for highly integrated power management solutions especially for wireless and battery-powered applications [1]. Linear regulator has an advantage over its switching counterparts in noise, ripple rejection, and cost despite its limit of efficiency [2]. Capacitor-free low-dropout regulator (LDO) is becoming increasingly popular [3–5] because it does not require a bulky off-chip capacitor at its output, which saves pin count, board area, and bill-of-material (BoM). This is especially attractive for complex system-on-a-chip (SoC), where LDOs are deployed in large numbers [4].

A major challenge in designing a capacitor-free LDO is stabilizing the voltage regulation loop without the external capacitor a conventional LDO counts on. It is well known that a capacitor-free LDO experiences the worst case for stability at $I_{out,\min}$. In prior arts, either a significant amount of on-chip compensation capacitance (23 pF) was employed to compensate for full load range (0–$I_{out,\max}$) [4], or sleep mode compatibility was sacrificed by requiring a minimum load current of $I_{out,\min}$ ranging from 1 mA [3] to 100 μA [5].

Although 100 μA is small compared to $I_{out,\max}$ of 100 mA, it is still larger than the average SoC sleep current in standby-power-critical applications [6]. It greatly reduces the battery life, since most portable electronics typically spend more time in sleep than in active mode [2]. Even if an LDO is not required to operate under extremely low I_{out}, in which cases the LDO itself will be shut down to save power (also known as hibernate mode), having a truly stable regulator at zero output current helps guard against unexpected load transient dips. On the other hand, the tight area constraints on LDOs put a limit on the maximum on-chip compensation capacitance. Hence, a new capacitor-free topology that is both sleep-mode ready and area efficient is needed.

2 Circuit description

The schematic of the proposed capacitor-free LDO is shown in Fig. 1. Instead of using an operational amplifier as the error amplification block, it consists of a current-differencing (CD) stage (M_1–M_6), a positive gain stage

J. Hu (✉) · W. Liu · M. Ismail
Department of Electrical and Computer Engineering, The Ohio State University, 2015 Neil Avenue, Columbus, OH 43210, USA
e-mail: Hu.193@osu.edu
URL: http://www.ece.osu.edu/∼hua

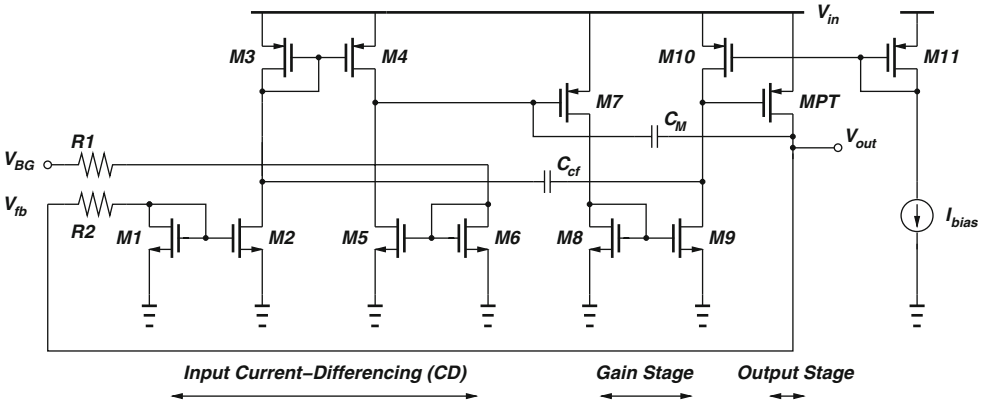

Fig. 1 Proposed LDO schematic

Transistor aspect ratio (W/L) (um)

M1=6/2	M4=8/2	M7=20/1	M10=M11=24/1	I_{bias} =20uA
M2=2/2	M5=2/2	M8=5/1	MPT=40000/0.18	C_M =4pF
M3=8/2	M6=6/2	M9=5/1	R1=R2=100K	C_{Cf} =500fF

(M_7–M_{10}), a PMOS pass element (MPT), and the resistive network (R_1, R_2). The CD stage is a CMOS version of [7], also widely used in analog signal processing and frequency filtering [8]. The LDO is internally compensated by MOSFET capacitance C_M and C_{cf} of 4 pF and 500 fF, respectively. No external capacitor is needed. Other component values and transistor aspect ratios are listed in Fig. 1.

2.1 Principle of input current-differencing

Input current-differencing technique was originally proposed in [7] for bipolar monolithic opamp design. As shown in Fig. 2(a), a "current mirror" was added across the common-emitter input, resulting in a current mode operation where the input currents are compared or differenced. With input resistance converting input voltage into current, a wide common-mode input range can be accommodated since both inputs are built-in biased with only $+V_{BE}$ above ground. A CMOS version, however, requires a third current mirror, as shown in Fig. 2(b), due to its zero gate current.

There are two major advantages when the technique is applied in an LDO. First of all, it allows low voltage operation. Notice that M_2, M_3, M_4, M_6 can be viewed as an N-input differential pair, except for the removal of the tail current source due to the built-in biasing by the diode-connected M_1 and M_5. As a result, the minimum supply voltage could be as low as $V_{gs} + V_{ov} \approx$ 0.9–1.1 V. In [4], the conventional P-input differential pair would require $V_{gs} + 2V_{ov}$ or $Vref + V_{gs} + V_{ov}$, whichever is higher, as shown in Fig. 2(c).

Secondly, this configuration renders a smaller feedback factor f that helps reducing the excessive loop gain that threatens stability in zero load [4]. An alternative approach to lower loop gain would be reducing g_m, since changes in r_o shifts dc gain and the dominant pole simultaneously (constant GBW). Since $g_m = \frac{2I_D}{V_{ov}}$ in saturation region, reducing g_m would require either increasing V_{ov}, which is already limited in a low voltage situation, or lowering I_D, which is effective only to a certain extent before the input devices enters weak inversion, where $g_m = \frac{2I_D}{V_{ov}}$ is no longer valid.

2.2 Stability analysis

Fig. 3(a) shows that the LDO consists of a basic amplifier $a(j\omega)$ and a feedback network $f(j\omega)$ using two-port analysis. Fig. 3(b) show the gain magnitude versus frequency for the basic amplifier of the LDO, where different feedback factor f influencing the loop gain. The key to stabilizing the LDO is designing a small feedback factor$f = \frac{1/g_{m_M1}}{1/g_{m_M1}+R_2}$ in reducing the loop gain to avoid the residual $a(j\omega)$ peaking in addition to the Q-reduction compensation [4].

The stability of the LDO can be analyzed in details with the small-signal equivalent circuit in Fig. 3(c). Let g_{m_Mi} be the transconductance of transistor $M_i (i = 1, 2, \ldots, 10)$. Let g_{mI}, g_{mG} and g_{mL} be the transconductance for the CD stage (M_1–M_6), the gain stage (M_7–M_{10}), and the output stage (MPT), respectively. Let r_i, C_i $(i = 1, 2, 3)$ be the output resistance and capacitance for each of the three stages. Let r_{cf}, C_p be the output resistance and capacitance associated with the drain of M_2, and C_{gd} be the gate-drain capacitance of MPT.

Assuming ideal frequency response of the Q-reduction current buffer (M_3–M_4) [4], the loop gain of the LDO can be found by breaking the voltage feedback before R_2 and calculating the open-loop transfer function from V_{fb} to V_{out}:

$$L(s)=\frac{v_{out}(s)}{v_{fb}(s)}=\frac{\frac{1/g_{m\_M1}}{1/g_{m\_M1}+R_2}\times g_{mI}g_{mG}g_{mL}r_1r_2r_3\left\{1+s\left(r_{cf}C_{cf}-\frac{C_{gd}}{g_{mL}}\right)-s^2\left(\frac{C_m(C_{gd}+C_2)}{g_{mG}g_{mL}}+\frac{C_{gd}r_{cf}C_{cf}}{g_{mL}}\right)\right\}}{(1+sC_Mg_{mG}g_{mL}r_1r_2r_3)\left(1+s\frac{C_mC_{gd}(g_{mL}-g_{mG})+C_{cf}C_3g_{mG}+C_mC_{cf}g_{mG}g_{mL}r_{cf}}{C_mg_{mG}g_{mL}}+s^2\frac{(C_{gd}+C_2+C_{cf})\times C_3}{g_{mG}g_{mL}}\right)} \quad (1)$$

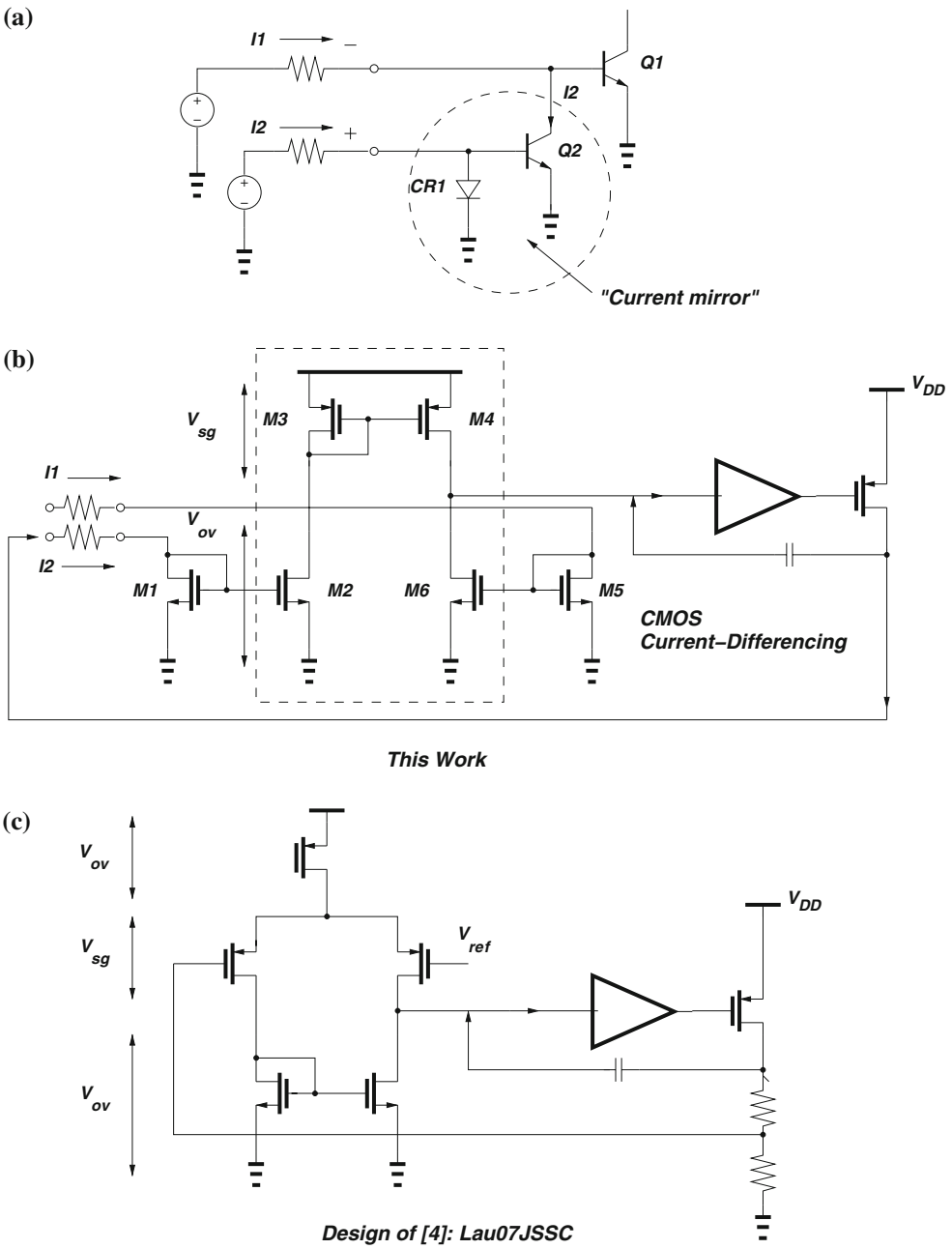

Fig. 2 Principle of input current-differencing (**a**) bipolar implementation (**b**) CMOS version (**c**) advantage over prior art

Since the transconductance of the pass element g_{mL} varies greatly with the output current, the stability of the LDO should be analyzed in three different load conditions.

In the case of moderate to high output current (I_{out}>1 mA), the loop gain can be simplified as:

$$L_h(s)=\frac{v_{out}(s)}{v_{fb}(s)}=\frac{\frac{1/g_{m\_M1}}{1/g_{m\_M1}+R_2}\times g_{mI}g_{mG}g_{mL}r_1r_2r_3(1+sr_{cf}C_{cf})}{(1+s/p_1)\left(1+s\frac{C_{gd}+C_{cf}}{g_{mG}}+s^2\frac{(C_{gd}+C_2+C_{cf})\times C_3}{g_{mG}g_{mL}}\right)} \quad (2)$$

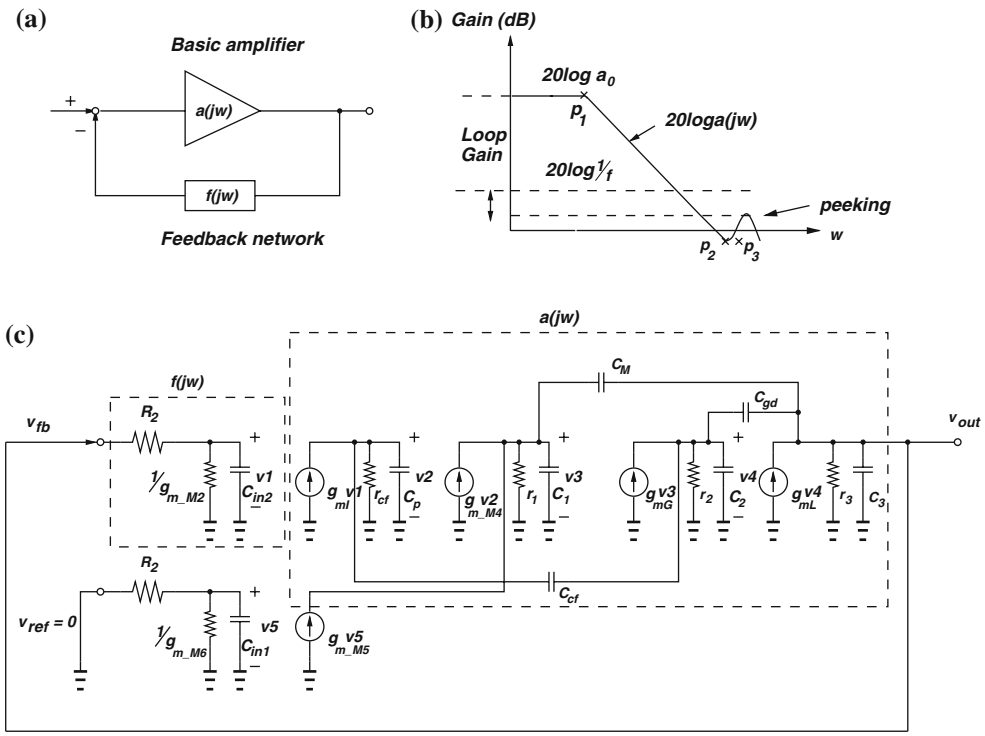

Fig. 3 LDO stability analysis (**a**) two-port model (**b**) gain magnitude versus frequency (**c**) small-signal equivalent circuit

where $p_1 = 1/(sC_M g_{mG} g_{mL} r_1 r_2 r_3)$ is the dominant pole. Two real roots p_2, p_3 exists for the quadratic function as $(4(C_{gd} + C_2 + C_{cf}) \times C_3)/g_{mL} \leq (C_{gd} + C_{cf})^2/g_{mG}$ holds due to a big g_{mL}. $z_1 = 1/r_{cf}C_{cf}$ cancels p_2, and p_3 is located at a much higher frequency.

In the case of low output current (I_{out}:100 μA–1 mA), the loop gain expression needs to be analyzed in full as (1). Though $p_1 = 1/(sC_M g_{mG} g_{mL} r_1 r_2 r_3)$ remains the dominant pole, the discriminant of the quadratic function in the denominator $\Delta = \left[\frac{C_m C_{gd}(g_{mL} - g_{mG}) + C_{cf} C_3 g_{mG} + C_m C_{cf} g_{mG} g_{mL} r_{cf}}{C_m g_{mG} g_{mL}}\right]^2 - \frac{4(C_{gd}+C_2+C_{cf}) \times C_3}{g_{mG} g_{mL}}$ is less than 0 due to a smaller g_{mL}. Thus, p_2 and p_3 form a non-dominant complex pole pair located at $\omega_{2,3} = \sqrt{\frac{g_{mG} g_{mL}}{(C_{gd}+C_2) \times C_3}}$ with frequency peaking in magnitude due to a large Q-factor [4]. An optional C_{cf} of 500 fF is used here to reduce the peaking.

In the case of near zero output current (I_{out}:0–100 μA), g_{mL} is minimal. This would result in an unstable LDO in existing topologies [3] [4] as the complex pole magnitude peak rises above 0 dB near crossover. However, the feedback factor $f = \frac{1/g_{m\_M1}}{1/g_{m\_M1} + R_2}$ from the CD stage of the proposed LDO lowers DC loop gain and effectively suppresses the peak below 0 dB even with zero output current.

3 Simulation results

The proposed LDO has been simulated in TSMC 0.18 μm 1.8 V/3.3 V RFIC 1P6 M+ process with key technology data listed in Table 1. It regulates 1.2 to 1.8 V input supply to fixed 1 V output with 51 μA quiescent current and 100 mA maximum outputs current. No minimum output current is required, i.e., the LDO is stable at $I_{out} = 0$. Line regulation at output $I_{out} = 0$ and $I_{out} = 100\,mA$ are 0.223%/V and 0.728%/V, respectively. Load regulation is 10.7 ppm/mA at $V_{in} = 1.2$ V. Figure 4 shows the transient response at various load parasitic and process corners. Worst-case 0.5% error recovery time is less than 13 μs under full load transient (0–100 mA) of 1 μs rise and fall time. Power supply rejection (PSR) is −41 dB at 1 kHz, and the output noise is 6.3 $\mu V/\sqrt{Hz}$ and 640 $nV/\sqrt{Hz}$at 100 Hz and 10 kHz, respectively.

Table 1 TSMC 0.18 μm CMOS process technology (2 V nominal devices)

	1.8 V NMOS	1.8 V PMOS
V_{th0} (mV)	475	449
t_{ox} (nm)	4.08	4.08
C_{ox} (fF/μm^2)	8.46	8.46
$k' = \mu C_{ox}$ (μA/V^2)	340	70
Breakdown voltage (V)	1.8	1.8

To demonstrate the advantage of proposed work, a comparison with existing work is shown in Table 2. This work reduces $I_{out,\min}$ to zero [4] and compensation cap from 21 pF [5] to 4.5 pF, which contributes greatly to the area saving. A figure of merit adapted from [9], defined as $\text{FOM} = \frac{I_{\text{outmin}} + I_q}{I_{\text{outmax}}} \times \frac{C_{\text{onchip}}}{C_{\text{parasitic}}}$, takes both effects into account.

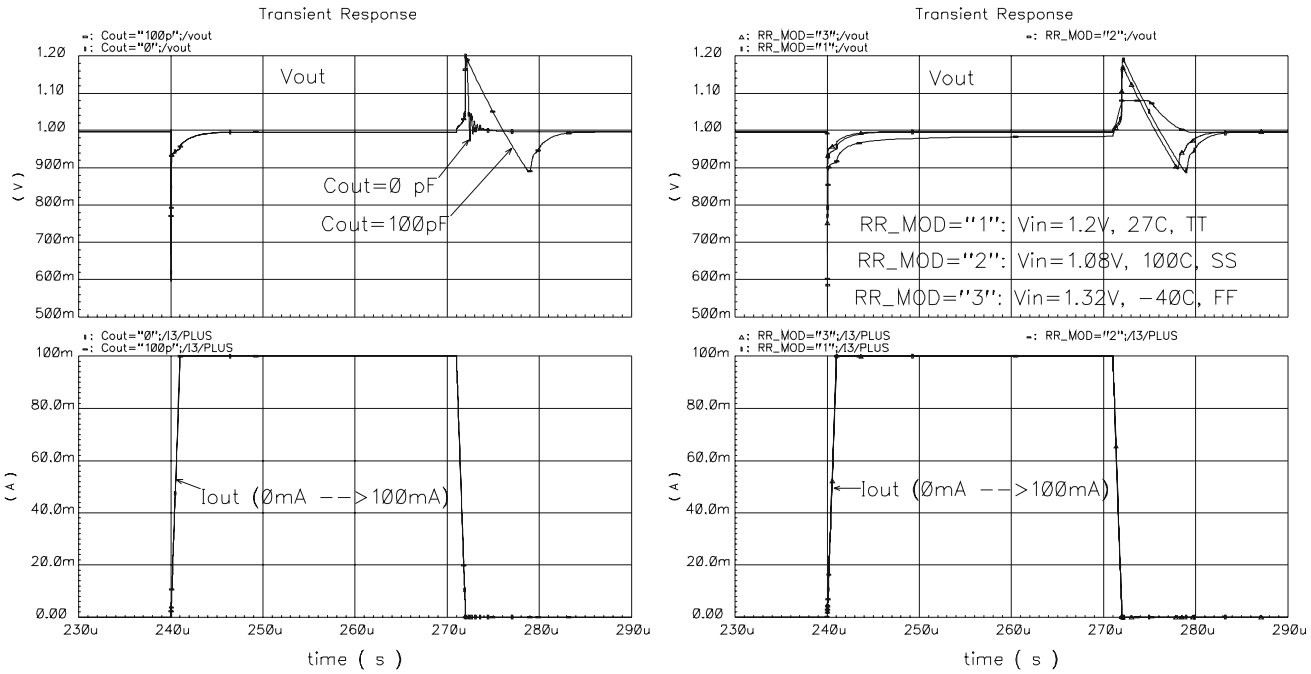

Fig. 4 Transient response of LDO under different output parasitic and corner conditions I_{out}: 20 mA/div., V_{out}: 100 mV/div., 10 μs/div

Table 2 Comparison with state-of-the-art capacitor-free LDO

	[4]	[5]	This work
Process	CMOS 0.35	CMOS 0.35	CMOS 0.18
Year	2007	2007	2009
V_{in} (V)	1.2–3.3	3–4.2	1.2–1.8
V_{out} (V)	1	2.8	1
Settling time (μs)	Not reported	15	13
$I_{out,\max}$ (mA)	100	50	100
$I_{out,\min}$ (μA)	100	0	0
Iq (μA)	100	65	51
On-chip cap (pF)	6	21	4.5
Area (mm^2)	0.125	0.120	0.020
Area/L_{min}^2	1.020	0.980	0.617
Current-area FOM	0.120	0.273	0.027

The smaller the FOM, the better current-area efficiency the LDO achieves.

4 Conclusion

A sleep-mode ready, current-area efficient capacitor-free LDO based on input current-differencing is presented. Compared with prior arts, it achieved sleep-mode efficiency and silicon area saving simultaneously.

Acknowledgments The authors would like to thank Texas Instruments (TI) for partially funding this research.

References

1. Shi, C., Walker, B. C., Zeisel, E., Hu, B., & McAllister, G. H. (2007). A highly integrated power management IC for advanced mobile applications. *IEEE Journal of Solid-State Circuits, 42*(8), 1723–1731.
2. Rincon-Mora, G. A. (2009). *Analog IC design with low-dropout regulator*. New York: McGraw-Hill.
3. Leung, K. N., & Mok, P. (2003). A capacitor-free CMOS low-dropout regulator with damping-factor control frequency compensation. *IEEE Journal of Solid-State Circuits, 38*(10), 1691–1702.
4. Lau, S. K., Mok, P. K. T., & Leung, K. N. (2007). A low-dropout regulator for SoC with Q-reduction. *IEEE Journal of Solid-State Circuits, 42*(3), 658–664.
5. Milliken, R., Silva-Martinez, J., & Sanchez-Sinencio, E. (2007). Full on-chip CMOS low-dropout voltage regulator. *IEEE Transactions on Circuits and Systems. I, Regular Papers, 54*(9), 1879–1890.
6. Sakimura, N., Sugibayashi, T., Nebashi, R., & Kasai, N. (2009). Nonvolatile magnetic flip-flop for standby-power-free SoCs. *IEEE Journal of Solid-State Circuits, 44*(8), 2244–2250.
7. Frederiksen, T., Davis, W., & Zobel, D. (1971). A new current-differencing single-supply operational amplifier. *IEEE Journal of Solid-State Circuits, 6*(6), 340–347.
8. Keskin, A. Ü. (2004). A four quadrant analog multiplier employing single CDBA. *Analog Integrated Circuits and Signal Processing, 40*(1), 99–101.
9. Hazucha, P., Karnik, T., Bloechel, B., Parsons, C., Finan, D., & Borkar, S. (2005). Area-efficient linear regulator with ultra-fast load regulation. *IEEE Journal of Solid-State Circuits, 40*(4), 933–940.

John Hu received the B.S. degree in electronics and information engineering from Beijing University of Aeronautics and Astronautics, Beijing, China, in 2006, and the M.S. degree in electrical and computer engineering from the Ohio State University in 2007, where he is now pursuing the Ph.D. degree. His research interest is power management integrated circuit design. He was an Ohio State University Fellow from 2006 to 2007 and has been a Texas Instruments Fellow since 2009. He interned with Battery Management Solutions and Low Power Wireless of Texas Instruments as an IC test engineer and IC design engineer in 2008 and 2009, respectively.

Wei Liu was born in Xi'an, China in 1976. He received his BSc. degree in 1998, MSc. degree in 2001 all in electrical engineering from Xi'an Jiaotong University, China. He was an ASIC design engineer from 2001 to 2003 in Zhongxing Corporation, China and an analog integrated circuit design engineer from 2003 to 2007 in Samsung Electronics, Korea. In September 2007, he joined the Department of Electrical and Computer Engineering at the Ohio State University as a Ph.D. student. His research areas include analog and mixed-signal integrated circuit design and integrated power electronics.

Mohammed Ismail received the B.S. and M.S. degrees in electronics and communications from Cairo University, Cairo, Egypt, and the Ph.D. degree in electrical engineering from the University of Manitoba, Winnipeg, MB, Canada. He has over 25 years experience of R&D in the fields of analog, RF, and mixed-signal integrated circuits. He has held several positions in both industry and academia and has served as a corporate consultant to nearly 30 companies in the United States, Europe, and the Far East. He is a professor of electrical and computer engineering and the founding director of the Analog Very Large Scale Integration (VLSI) Laboratory, the Ohio State University, Columbus and of the Radio and Mixed Signal Integrated Systems (RaMSiS) Group, Royal Institute of Technology (KTH), Stockholm, Sweden. His current research interests include fully integrated CMOS radios, BIST and digital self-calibration of RFICs, yield enhancement design and power management solutions. He has authored or coauthored intensively in the related area and has been awarded 11 patents. He has advised the research work of 49 Ph.D. and over 90 M.S. students. He has coedited and coauthored several books including a text on Analog VLSI Signal and Information Processing (McGraw-Hill, 1994). His last book is entitled Radio Design in Nanometer Technologies (Springer, 2007). He is the Founder and the Editor-in-Chief of the International Journal of Analog Integrated Circuits and Signal Processing. He is on the International Advisory Boards of several journals. He cofounded ANACAD-Egypt (now part of Mentor Graphics, Inc.) and Firstpass Technologies, Inc., a developer of CMOS radio and mixed-signal IPs for handheld wireless applications. Prof. Ismail has been the recipient of several awards including the US National Science Foundation Presidential Young Investigator Award, the US Semiconductor Research Corporation Inventor Recognition Awards in 1992 and 1993, The College of Engineering Lumley Research Award in 1992, 1999, 2002, and 2007, and a Fulbright/Nokia Fellowship Award in 1995. He was an Associate Editor for many IEEE Transactions, and was on the Board of Governors of the IEEE Circuits and Systems Society. He is the founder of the International Conference on Electronics, Circuits, and Systems (ICECS), the Circuit and Systems (CAS) flagship conference for Region 8.