Master-Slave Battery Charging System Using Parallel DC-DC Converters for Thermal Safety

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***Abstract*—Safety has become extremely important, even when the market is demanding faster charging of mobile batteries. Single-chip battery chargers cannot safely deliver the current needed because power density will exceed the package limit and create thermal hot spots. Therefore, a master-slave battery charging system using parallel DC-DC converters is presented. The master charger acts as a voltage or current source, and multiple slave chargers are turned on and off by the master as current sources. With it, the heat is spread out into multiple locations on the PCB, effectively eliminating thermal hot spots. With one slave, the constant-current (CC) phase charging time was reduced by 46%. With two slaves, thermal hot spots temperature were reduced by 15C. Designed as a switch-mode current source, the slave charger achieved 4% current accuracy (6-σ), and 92% peak efficiency from 5-9V input, 0.5-3A output range. It occupies 3.9 mm^2 in a 0.18 μm BCD process.**

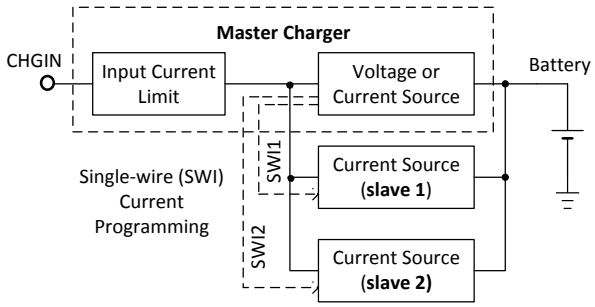

Fig. 1: Battery charging system using parallel DC-DC converter

I. Introduction

Fast and safe battery charging is a major challenge for smartphones and tablets applications, as the capacity of Li-Ion batteries continue to grow. Prior work on battery chargers focused on PWM-PFM mode transition [1], partial current sensing [2], and battery resistance monitoring [3] to improve efficiency and reduce charge time. As charge current increases further, the maximum current through a single die is limited by power density. Hence, a parallel charging scheme that can safely increase total charging current is proposed.

Compared with multiphase DC-DC converters [4], [5], clock synchronization and phase alignment [4] is not required, which reduces inter-chip PCB routing. Phase imbalance [5] is also avoided, since each slave regulates its own output current. Master-slave control [6] has been reported in parallel DC-DC converters to increase power capacity and achieve redundancy. This work distinguishes the role of slave as purely current regulation, thereby eliminating voltage regulation loops [1]–[3] and current sharing control [5], [6] to achieve low cost, smaller die area, and thermal safety.

II. Design Challenge

The charging of a typical Li-Ion battery goes through pre-qualification (PQ), constant-current (CC), constant-voltage (CV), and termination stages [7]. PQ current is limited to due to safety concerns, and termination current is programmable by users. To reduce charge time for a given capacity (Q), a larger CC current is the key. However, chip-scale package (CSP) on handset PCB is already limited by thermal constraints. Increasing CC current in a single chip would require a much larger die size or package, both of which is costly. Connecting multiple chargers in parallel [8] can temporarily solve the heat problem, but CV thresholds have to be set differently for all chargers connected, and the total silicon cost grows proportionally. Hence, a charging system that is simpler than multi-phase solutions [4], [5], but maximize CC current with minimum silicon cost is needed, all under a stringent thermal safety requirement.

III. System and Circuits

A. Block Diagram

Fig 1 shows the master-slave charging system using parallel DC-DC converters. The total input current is monitored by the master, and slave outputs are shorted to BAT. The master acts as a voltage or current source depending on the charging mode. Slaves are turned on and programmed through a single-wire (SWI) interface.

Fig 2 shows the implementation of both chargers. The master charger can be designed with current-mode [1], voltage-mode [2], or other methods of control [3]. The slave adopts hysteretic current-mode control partly due to the inherent current-limit from the topology. Slaves output current is sensed through a PMOS switch (QBAT) replica with auto-zero current sense amplifier to achieve the best accuracy. An RC integrator

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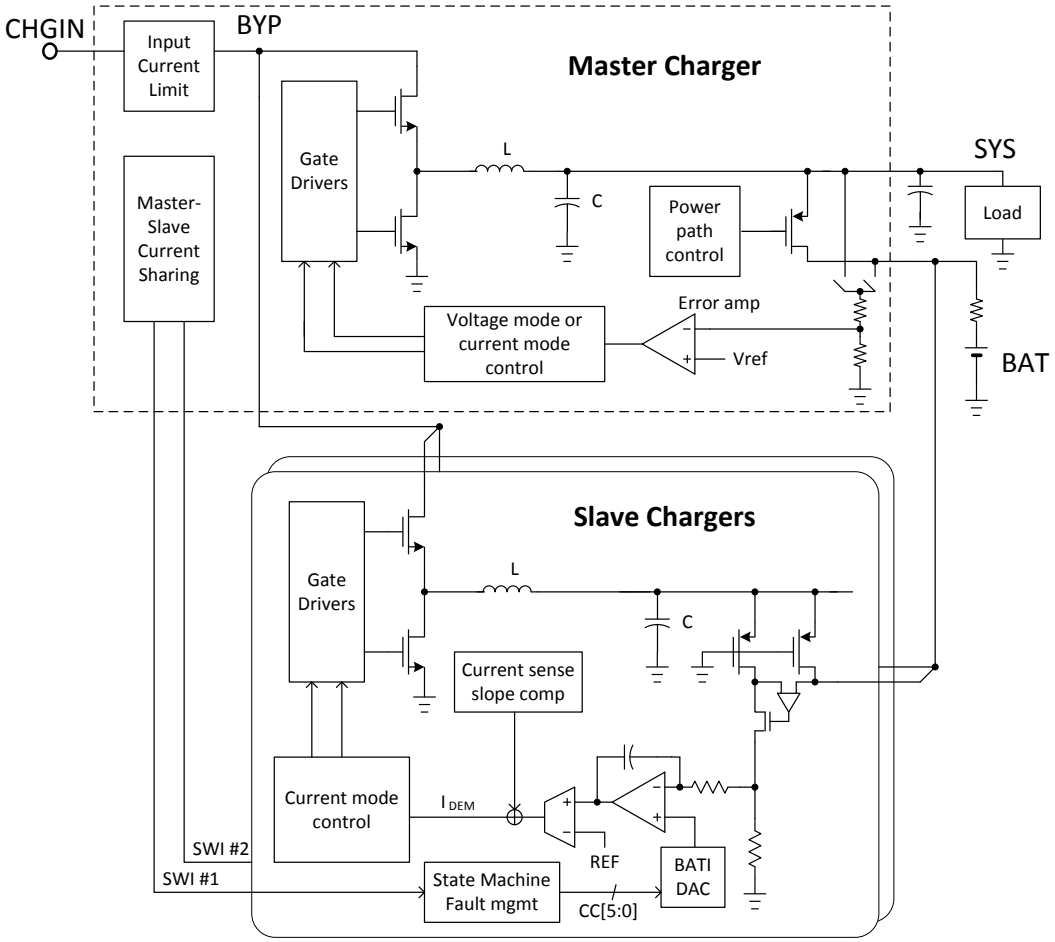


Fig. 2: Circuits and Block Diagram for master and slave chargers

sets the bandwidth of the BATI loop, and slope compensation is added to avoid sub-harmonic oscillation.

B. Safety Mechanism

For maximum safety, the master-slave charging system operates as follows. During the CC stage, the total current is split equally (or in a programmable ratio) among the master and all slaves. During CV, slaves remain on until the masters current drops to zero (or below a programmable threshold). Slaves are then turned off, and the master will finish the rest of CV stage. Due to the absence of voltage regulation, the slave charger employs multiple self-protection, such as BAT over-voltage (OV) and input-greater-than-BAT (INGTBAT) protection. If the battery is removed during charging, BAT pin voltage could overshoot above safety level. BATOV comparator with short de-bounce will turn off both high-side and low-side FETs immediately. Because slave converters only operate in CCM mode, INGTBAT is required, otherwise average inductor current will go negative, draining current from BAT to input.

TABLE I: Charge time comparison. Unit: minutes. (2800 mAh battery, 200mA termination)

	Master only	Master + 1 slave
CC phase	44	23.6
CC phase: Master + Slave	0	5.7
CV phase: master only	36.5	34.7
Total time	80.5	64

IV. Measurement Results

A. Bench

The master-slave charging profile is measured over a 4.4V, 2800mAh battery in Fig 3. Due to thermal limitation, the maximum current through a single die is 3A, and for a master and a slave is 5A (2.5A each). For single-chip 3A charging, CC and CV stages take 44 and 36.5 minutes, respectively. For master-slave charging, the CC stage is shortened to 23.6 minutes. The slave remains on in CV for 5.7 minutes, then it is turned off. The CV time in master-slave charging is slightly longer than that of a single chip because CC-CV transition

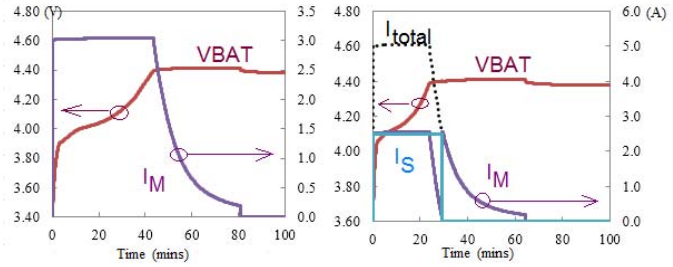


Fig. 3: Measured charging profile for 2800 mAh battery with similar thermal performance. Left: master 3A. Right: master 2.5A, slave 2.5A.

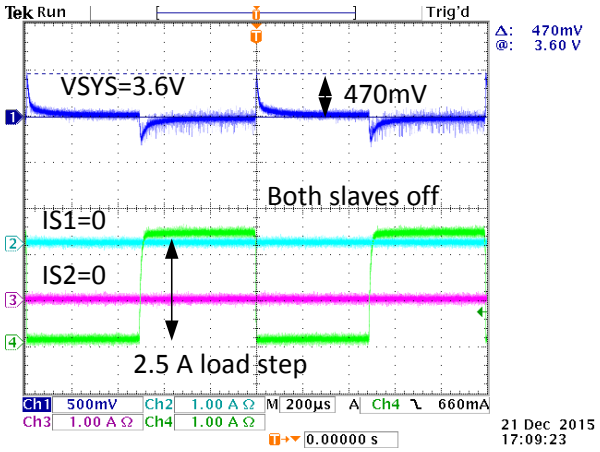


Fig. 4: Response to load transient on SYS. Master only. Slave 1 and 2 off.

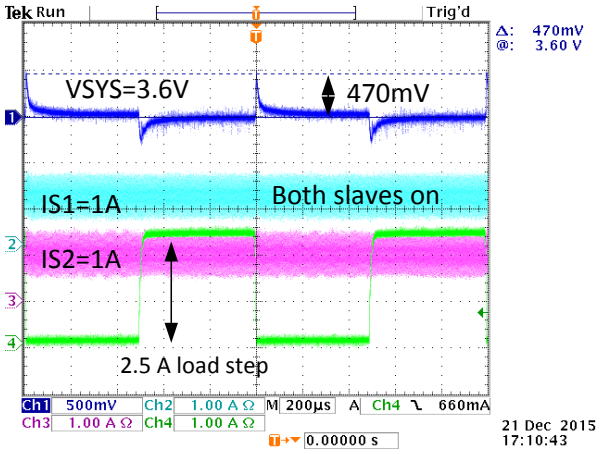
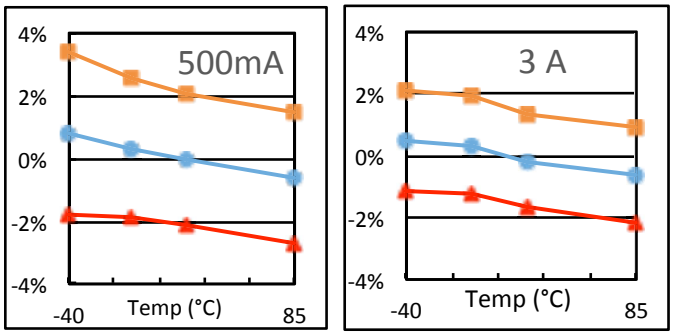


Fig. 5: Response to load transient on SYS. Master, Slave 1 and 2 on.

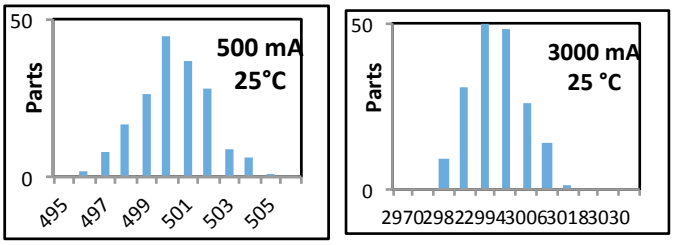
is earlier at higher current due to battery impedance [3]. The total charge time is also compared in Table I.



(a) I_{out}: 500mA (b) I_{out}: 3A

Fig. 6: Slave current accuracy (6-σ) across temperature

Load transient performance of the master-slave charging system is the same as that of the master alone. Fig. 4 illustrates the SYS load transient under 2.5A load step every 500us. The overshoot and undershoot are 470mV and 250mV, respectively, and they remain unchanged with or without slave charging.



(a) I_{out}: 500mA (b) I_{out}: 3A

Fig. 7: Slave current distribution across 150 units

B. ATE Characterization

The current accuracy of the master-slave charger system is determined by the master, as it monitors the total current through a sense resistor. However, if such a resistor is not available, the slave current accuracy becomes relevant. Fig. 6 show the slave current accuracy based on 150 units characterized from -40C to 85C. The 6-σ error is less than 4% at 500mA and 3A setting. This accuracy is achieved by trimming current sense resistor (CSR) (shown in Fig.2). The post-trim distribution of 500mA and 3A are shown in Fig. 7.

C. Thermal Safety

The thermal safety of the charger system is captured by a thermal camera in Fig. 8 Single-chip can only safely charge 3A due to its hot spot reaching $76°C$. With one slave, 5A total charging can be achieved with hot spots below $62.5°C$. With two slaves, thermal hot spots for 6A total charging are reduced by $15°C$ compared with one slave charging. The measured efficiency of the slave charger is shown in Fig. 9a. Peak efficiency of 95%, 92%, and 90% are achieved for 5V, 9V, and 12V input charging.

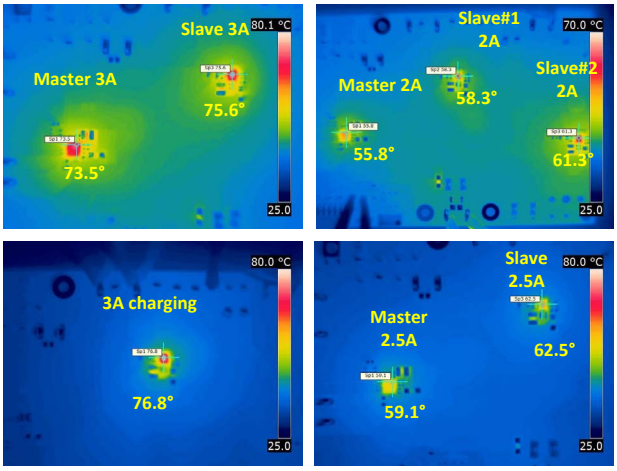
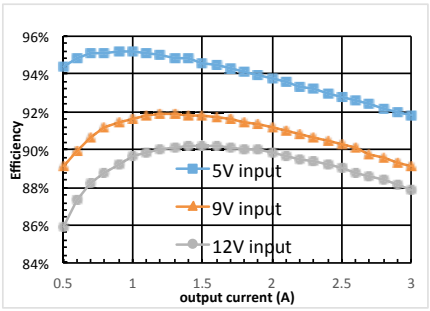
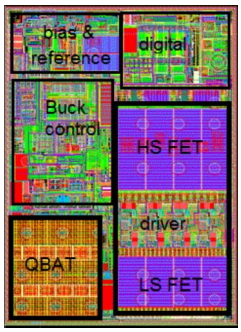


Fig. 8: Thermal profiles for CHGIN=5V, BAT=4.4V charging.



(a) Slave charger efficiency: V_{in}: 5V, 9V, 12V. V_{BATT}: 4.4V.



(b) Slave charger layout

Fig. 9: Slave charger efficiency and layout photo

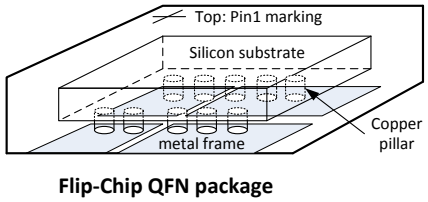


Fig. 10: Flip-Chip QFN Package used for slave charger

D. Package and Layout

Fig. 9b shows the slave charger chip layout, and Fig. 10 shows the Flip-chip QFN (FC-QFN) package used for slave charger to lower thermal impedance. Compared with wire-bond package [1], parasitic inductance is greatly reduced. Compared with chip-scale package (CSP) [7], QFN metal frames help with heat dissipation. Lastly, Table II compares master-slave charging with prior work on switch-mode battery chargers. It compares favorably in efficiency, power density, and charge time savings.

TABLE II: Comparison with Prior Work on Battery Chargers

	[1]	[2]	[3]	This Work
Technology	$0.35\mu m$ BiCMOS	$0.18\mu m$ CMOS	$0.25\mu m$ CMOS	$0.18\mu m$ BCD
Control method	current-mode PWM	charge-control PWM	voltage-mode PWM	current-mode hysteretic
f_{sw} (MHz)	0.6-2.4	2.2	0.5	2-4
V_{in} (V)	3.0-4.5	5-10	4.5-5.5	5-13
V_{out} (V)	1.8-2.7	2.1-4.2	2.1-4.2	3-4.7
I_{out} (A)	0.5	0.9	2	3
η_{max}	95%	86%	87%	92%
die (mm^2)	N/A	1.6	3	3.9
Time saved	N/A	N/A	40% CC	46% CC
Hot spot reduction	N/A	N/A	N/A	$-15°C$

V. Conclusion

A safe, master-slave battery charging system is proposed. As a result, CC time was reduced by 46%, and thermal hot spot temperature was reduced by $15°C$ for the same total charge current. System transient response is not affected by slave's operation. The slave charger achieved 4% current accuracy (6-σ) and peak efficiency of 92% in 9V to battery charging. The proposed system is well suited for advanced mobile handsets seeking to reduce charge time with better thermal performance.

VI. Acknowledgement

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