Increasing sleep-mode efficiency by reducing battery current using a DC-DC converter

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***Abstract*—Battery current is a key parameter that decides the runtime of a portable electronic system. For low power applications like IEEE 802.15.4 and Zigbee wireless network, the average battery current drain approximates the sleep mode current drain, since significantly more time is spent in sleep than in active usage. This paper proposes substituting a DC-DC converter for a low drop-out (LDO) regulator in the sleep mode power chain, such that the current drawn from the battery would be less than the actual current drained by the load. The battery current saving, and hence battery runtime extension, is estimated to be around 35% based on the analysis of a 65 nm CMOS IEEE 802.15.4/Zigbee low power wireless system-on-chip (SoC) model, whose parameters are extracted from state-of-the-art industrial products and experimental data from advanced nanometer processes.**

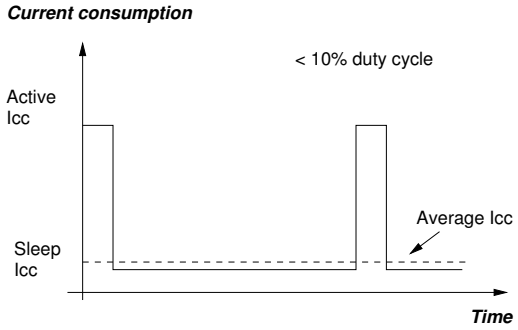

Fig. 1. Active and sleep mode current consumption [2]

I. Introduction

Short battery life is not only inconvenient for consumer electronics like laptops and cell phones, but also fatal to the commercial success of multi-year low power electronic devices like IEEE 802.15.4 and Zigbee wireless sensor networks for industrial, scientific, and medical (ISM) applications, due to the complexity and cost associated with replacing batteries.

Despite the innovations in battery technologies, increasing circuit efficiency remains the most effective way to prolong battery life. The bottleneck of power efficiency improvement, however, lies in the sleep mode [1]. For example, battery-operated IEEE 802.15.4/Zigbee sensor nodes will be in sleep mode 99.9% of the time, waking up periodically for a few milliseconds to check a sensor or poll the other radios. [2] Thus, the total power consumption will approach sleep mode power consumption, as depicted in Fig. 1, with duty cycle (wake up time per operating period) well below 10%.

However, reducing the current consumption of the chip, I_{cc} [1], during the sleep mode of a low power integrated circuit (IC) or System-on-Chip (SoC) is non-trivial. The sleep mode I_{cc} is usually made up of the biasing and quiescent current (I_q) of the key sub blocks that remains on during sleep, such as power-on-reset (POR), brown-out-detection (BoD), memory data retention, and sleep timer, as well as the leakage current of the rest of the circuits. It is challenging to reduce I_q of a circuit block without huge performance penalty, but it is even more challenging to control the leakage as the CMOS IC technology scales into the nanometer regimes, where leakage increases dramatically.

The reduction of standby leakage has been addressed by different techniques such as power gating [3], dynamic voltage scaling (DVS) [4], and body biasing [5]. Power gating and DVS use the power supply voltage, V_{dd}, as the primary knob for reducing leakage currents, by either cutting off, or gating, a circuit from its power supply, or lowering V_{dd} to reduce leakage. The penalty is mostly the area and design overhead. Body biasing adjusts the threshold voltage, V_{th} to reduce transistor sub-threshold leakage. However, reverse body biasing worsens short channel effects like drain induced barrier lowering (DIBL), and increases V_{th} variation across a die, which makes it less effective with technology scaling [5].

Motivated by the important role the power supply, V_{dd}, plays in standby leakage reduction and sleep mode efficiency boosting, this paper investigates the power chain structure within the widely used low power SoCs. A DC-DC converter based power chain is proposed to effectively reduces sleep mode battery current.

This paper is organized as follows: Section II presents the system power management requirements for a low power IEEE 802.15.4/Zigbee SoC. Section III studies the different power chain structures currently used and proposed a DC-DC converter based power chain topology for sleep mode. Section IV demonstrated the advantages of proposed power chain topology in battery current drain compared with existing structures, and Section V concluded the paper with future research directions.

[1]Notice that the total chip current (I_{cc}), more precisely the battery current (I_{batt}) decides the battery life, because the battery voltage remains relatively constant.

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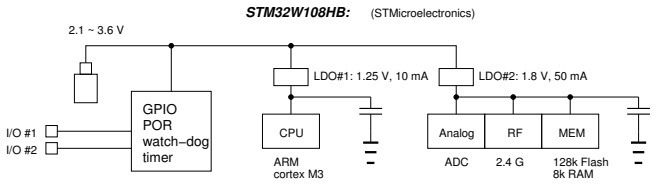

Fig. 2. Power chain example 1: STMicroelectronics STM32W108 2.4G wireless SoC [7]

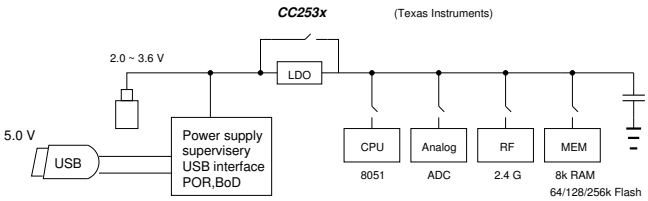

Fig. 3. Power Chain example 2: TI CC253x 2.4G SoC [8]

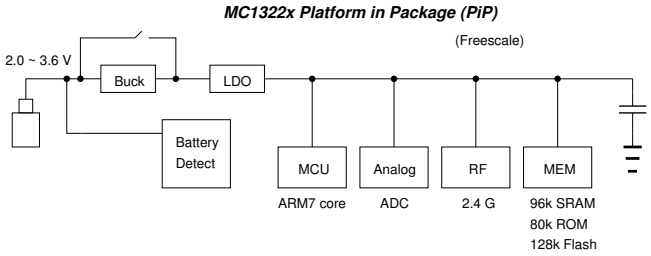

Fig. 4. Power chain example 3: Freescale MC1322x 2.4G PiP [9]

II. System Power Management Strategy within a Zigbee SoC

A. IEEE 802.15.4 and Zigbee overview

The IEEE 802.15.4 standard was charted for low data rate, low complexity, multi-year battery life Wireless Personal Area Network (WPAN) [6]. Zigbee is a suite of higher level communication protocols based on IEEE 802.15.4 standard to offer a complete network solution. Their applications could vary from smart metering, to home energy control and automation.

B. Zigbee SoC

To enable broad commercial adaptation, optimally designed IEEE 802.15.4/Zigbee-compliant SoC silicon device that could downscale the end-application system cost and design complexity is critical. Such an SoC typically integrates an IEEE 802.15.4/Zigbee-compliant RF transceiver for wireless communication, a CPU (or microcontroller), memory devices (RAM and ROM) for embedded processing, and ADCs for sensor interface, etc.

C. Power Mode Division

With emphasis on multi-year battery operation as well as short latency, i.e., short wake-up time, Zigbee SoCs are usually designed with different power modes. Power hungry blocks, such as the CPU and the RF transceiver, are switched off during sleep mode, while parts of the memory blocks could be set into retention to keeping critical data intact. Other blocks, such as oscillators, timer, and watchdog circuits, could be arranged to remain on or switched off depending on the SoC function required.

D. Power Management Circuit

In addition to power mode division, Zigbee SoC also has dedicated power manage circuits, such as linear regulators, which converts the battery voltage to the voltage levels required by different sub-blocks, and supports advanced power management scheme, such as dynamic voltage scaling (DVS), if available.

III. Power Chain Study

A power chain can be loosely defined in this paper as a power flowing path from the battery to a point of load. Each load circuit will have one or more power chains to the battery. Depending on the power mode, different chains can be selected and activated.

Several examples of the power chains within in state-of-the-art commercial products are shown in Fig. 2, 3, and 4 respectively. Fig. 2 shows a 2.4 GHz wireless SoC from STMicroelectronics built in ST's proprietary $0.18\mu m$ process [7]. Circuit blocks such as General Purpose Input-Output (GPIO) and Power-on-Reset (POR) are directly powered from the battery due to voltage level compatibility and the need for direct battery voltage access. Analog, RF, and memory circuits are powered off an internal 1.8 V LDO, which provides the standard supply voltage of a $0.18\mu m$ process and allows for maximum IP reuse. The CPU, on the other hand, operates off a 1.25 V LDO to reduce power consumption.

Fig. 3 shows a 2.4 GHz low power wireless SoC from Texas Instruments [8]. Unlike Fig. 2, both digital and analog sub-blocks are powered by a single 1.8 V LDO for simplicity. Notice that all sub-blocks can be disconnected from the supply rail during sleep mode to save on leakage, and the LDO can be by passed for direct battery operation.

Finally, Fig. 4 shows a 2.4 GHz low power wireless Platform in Package from Freescale Semiconductor [9]. It is similar to Fig. 3 expect that an optional Buck converter is added in series of an LDO to create the internal 1.8 V power supply rail. According to its datasheet [9], the converter will be activated during heavy load in active operations to save on battery current. During sleep mode, where the load current is low, the converter will be bypassed to avoid the Buck converter's operational overhead in power consumption.

In summary, the common theme for all three products is that the sleep mode power chain (the power chain to the load that remains on during sleep, e.g., Load 1 as in Fig. 5) consists of LDOs only, if not merely a wire. Even if a DC-DC converter is available in the structure, it is disabled during sleep mode. This paper proposes using DC-DC converters in sleep mode so that the battery current in sleep mode will also be reduced.

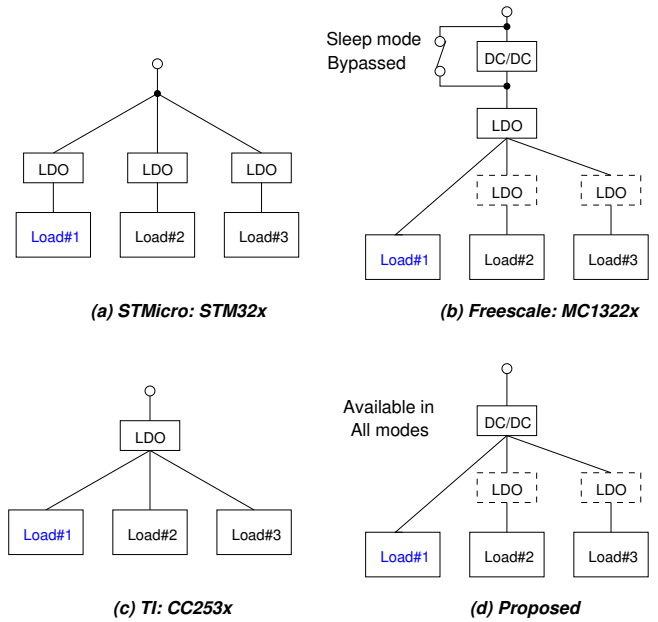

Fig. 5. Configuration of the sleep mode power chain: existing solutions and proposed.

IV. Power Saving from Proposed Structure

This section will quantify the power saving by replacing the conventional LDO-based power chain with the proposed DC-DC-based structure during a leakage-dominated sleep mode operation for a hypothetical IEEE 802.15.4/Zigbee wireless SoC in a digital 65 nm CMOS process. Even though the analysis is based on a specific genre of low power wireless SoCs, the findings are nevertheless general and can be applied to other standby-power-critical applications as well.

A. Sleep Mode Current Budget

The system is assumed to operate from a single-cell Li-Ion battery with nominal voltage of 3 V. During its sleep mode, 0.5 μA of "always-on" static power consumption is assumed for the essential functional blocks operated directed off the battery supply. Leakage reduction techniques such as power gating are assumed to have been applied such that the leakage from RF and analog is negligible due to the small number of transistors involved. Leakage from the CPU is assumed to be less of an impact than that of the memory, since V_{dd} of combinational logic circuits, which usually make up the majority of CPU, can be set very close to zero without any major concern [2], but a $V_{dd_{min}}$ is needed by a considerable portion of memory circuits like random-access memory (RAM) to retain their contents. To simplify the analysis, the sleep mode current budget will focus on the "always-on" and the leakage caused by data retention with $V_{dd_{min}}$ of 500 mV.

[2]In practice, sleep mode wake-up latency and current surge that leads to large IR drop is a concern. [10]

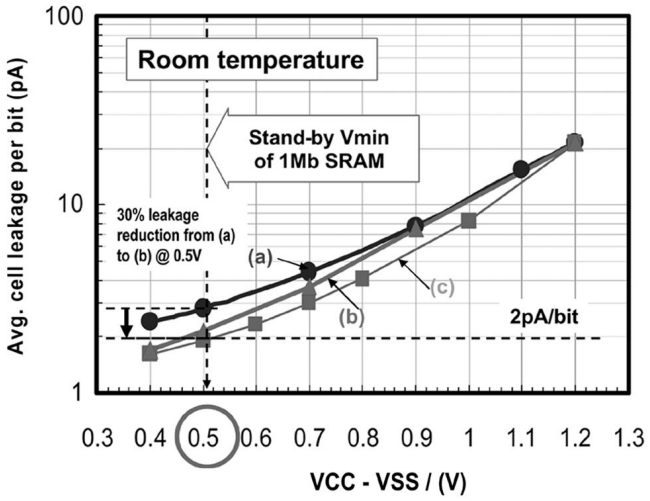

Fig. 6. Experimental data from 65 nm CMOS Ultra Low Power SRAM: Leakage reduction with V_{DD}. [12]

B. Leakage-Supply Modeling

The leakage current of a MOSFET is made up of gate tunneling, I_{gate}, gate induced junction leakage, I_{GIDL}, and the subthreshold current, I_{sub}, which often dominates and can be expressed as [11]:

$$I_{sub} = \frac{W}{L} I_t exp(\frac{V_{gs} - V_{th}}{nV_T})[1 - exp(-\frac{V_{DS}}{V_T})] \quad (1)$$

As we can see from equation 1, the I_{sub} decrease exponentially as the supply voltage V_{DD} is reduced. Decreasing V_{DD} would also reduce I_{gate} and I_{GIDL} as well [11]. To comprehensively model the leakage-supply relation, experimental data from a 65 nm ultra-low-power CMOS SRAM design [12], is used to construct an empirical formula.

As seen in Fig. 6 curve (a), the total leakage per bit decreases almost linearly with V_{DD} in the logarithm scale, which is in agreement with the exponential V_{DD}-relationship of I_{sub}, which is supposed be dominant. Though additional techniques like PMOS back gate bias (b) and virtual ground raise (c) would reduce the leakage further as reported in [12], this paper assumes a simple exponential I_{LEAK}-V_{DD} relation, i.e., assume

$$log(I_{LEAK}/bit) = k \cdot V_{DD} \quad (2)$$

Given the data pair $(20pA/bit, 1.2V), (2.8pA/bit, 0.5V)$ in [12], the parameter in equation 2 can be estimated as $\widehat{k} = (k_1 + k_2)/2 = 2.38$. Assume that 16 KB of SRAM is on-board the SoC for data retention, the total leakage current can be modeled as

$$I_{LEAK} = 8bit/B \times 16KB \times exp(2.38 \cdot V_{DD})pA/bit \quad (3)$$

The comparison is made between the conventional LDO based power chain and the proposed DC-DC converter, as seen in Fig. 7. The LDO is assumed to be ideal, thus

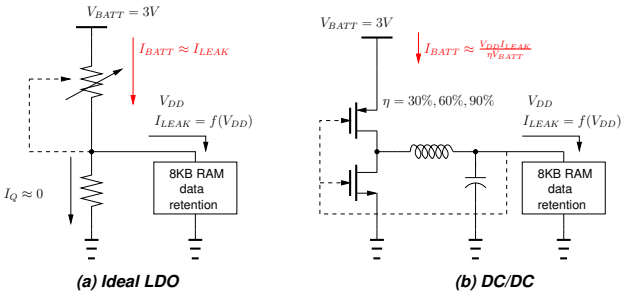

Fig. 7. Comparison between an LDO-based and a DC/DC based power chain in sleep mode

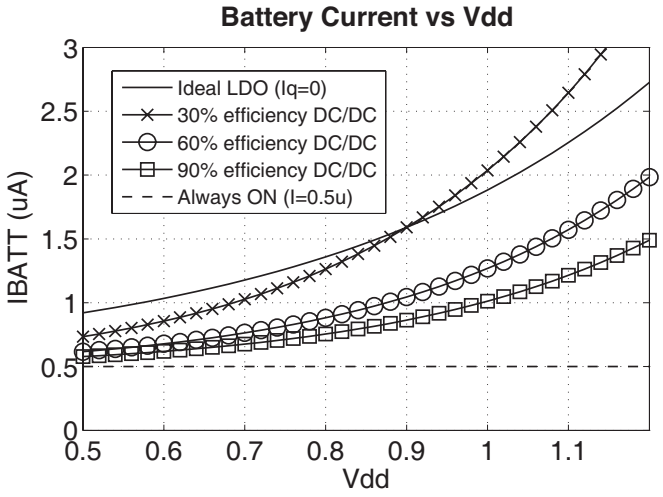

Fig. 8. Battery Current Reduction using DC/DC converter

TABLE I
BATTERY CURRENT (UNIT:μA) AT DIFFERENT RAM VOLTAGES (V_{DD})

V_{DD}	1.2 V	0.9 V	0.5 V
LDO	2.74	1.60	0.93
60% DC-DC	2.00	1.04	0.62
I_{BATT} saving	27%	35%	33%

$$I_{BATT\,LDO} = I_{LEAK} + I_{Q\,LDO} \approx I_{LEAK} \tag{4}$$

The DC/DC converter is assumed to have efficiency of η.

$$I_{BATT\,DCDC} = \frac{V_{DD} I_{LEAK}}{\eta \cdot V_{BATT}} \tag{5}$$

Fig. 8 shows the battery currents of the resulting system during sleep mode. A 30% efficient DC-DC converter would consume more battery current compared to the ideal LDO unless the RAM data retention voltage, V_{DD}, is lowered below 0.9 V. A 60% efficient DC-DC converter, on the other hand, would reduce the battery current by 20% to 30% across the entire V_{DD} range of interest (0.5 V to 1.2 V). Table I summarize the battery currents at three bench mark voltages.

V. CONCLUSION AND FUTURE WORK

This paper proposes using a DC-DC converter in the sleep mode power chain of low power electronic system to reduce battery current. Compared to the best case scenario of conventional LDO-based power chain structure, it reduces the battery current by as much as 35% based on the analysis of a leakage-dominated 65 nm CMOS IEEE 802.15.4/Zigbee wireless SoC model, whose parameters are extracted from state-of-the-art industrial products and experimental data [12].

This paper, however, does not detail the design of the ultra-light-load DC-DC converter with said efficiency, since integrated DC-DC converters with similar output power profile (1-100 μW) with above 80% efficiency using all-digital PFM control has already been reported [13]. Reseach in effective implementation of highly efficient sub-1V, 1-10 μA output DC-DC converter will be critical to fully claim the battery life extension suggested by this paper.

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