NAND-Based Ring Oscillator for Timing Applications

Ansari Almas Mohd Minnatullah

Department of Electronics Engineering VLSI Design & Technology,

Shah & Anchor Kutchhi Engineering College Mumbai, Maharashtra 400088, India

almas.18219@sakec.ac.in

Abstract— This paper discusses the generation and the design considerations of a NAND-based ring oscillator, especially in timing-related circuit designs. Ring oscillators, fundamental circuits for generating oscillations without an external clock source, rely on the cumulative delays of a loop of inverters or logic gates, such as NAND gates, to create a stable oscillating frequency. This survey investigates the design parameters, advantages, challenges, and potential improvements in NAND-based ring oscillators for precise timing applications.

I. INTRODUCTION

Ring oscillators, formed by chaining odd numbers of inverters or logic gates, are widely used in digital circuits to generate periodic signals. A NAND-based ring oscillator leverages NAND gates instead of basic inverters, providing advantages in flexibility and additional control inputs, crucial for applications in timing, clock generation, and frequency synthesis reference.[1] By carefully controlling the delay in each NAND gate, the oscillation frequency can be finely tuned, a valuable feature in time-sensitive circuits such as phase-locked loops (PLLs) and clock recovery systems

II. PRINCIPLE OF GENERATION

A ring oscillator functions by propagating a signal through a chain of gates, with the output redirected to the input, forming a self-sustaining loop. In a NAND-based configuration, as shown in **Fig. 1**, each stage has an extra control line, allowing for external modulation and greater flexibility in frequency control. The oscillation frequency foscf_{osc}fosc depends on the total delay TdelayT_{delay}Tdelay per gate

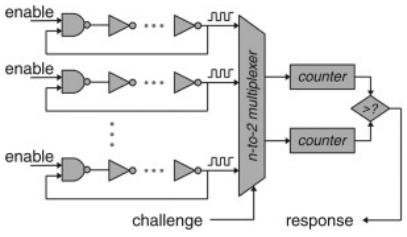

Fig. 1 Overview of NAND-Based Ring Oscillator for Timing Applications

III. IMPLEMENTATION

Two fundamental NAND-based ring oscillator designs have been presented:

1. **Standard NAND-Based Ring Oscillator**: The oscillation frequency foscf_{osc}fosc of a basic NAND-based ring oscillator is defined by the equation:where n is the number of stages and TdelayT_{delay}Tdelay is the propagation delay per stage.reference.[2] By arranging NAND gates in an odd-number loop, as depicted in **Fig. 2**, each gate inverts the previous signal, resulting in oscillations

$$f_{osc} = \frac{1}{2n \cdot T_{delay}}$$

2. **Current-Starved NAND-Based Ring Oscillator**:A current-starved NAND-based oscillator uses current-limiting transistors with each NAND gate, as illustrated in **Fig. 3**, allowing the oscillation frequency to vary with the control voltage. This enables fine-tuning of frequency and power consumption for timing-sensitive applications.reference.[3]

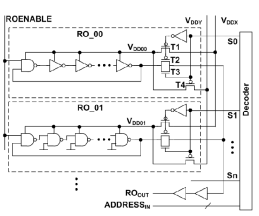

Fig. 2 Standard NAND-Based Ring Oscillator

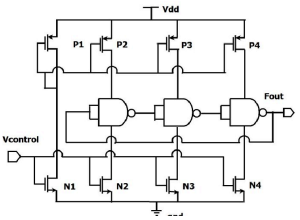

Fig.3 Current-Starved NAND-Based Ring Oscillator

To enhance the frequency stability of a NAND-based ring oscillator, improving the power supply rejection ratio (PSRR) is essential, as supply voltage variations can lead to frequency shifts. reference.[4] Utilizing decoupling capacitors close to the power pins of the oscillator can effectively stabilize the supply voltage, reducing frequency drift. To combat phase noise and frequency jitter from supply transients, adding capacitive bypass or filtering components near each NAND gate helps smooth power variations. Ensuring layout symmetry and optimized routing minimizes propagation delay variations, while using temperature-compensated resistors maintains consistent delay, reducing temperature sensitivity.

IV. ISSUES & IMPROVEMENTS

Challenges in NAND-based ring oscillators often involve maintaining frequency stability. Solutions include: Temperature Compensation: Using temperature-insensitive design techniques or incorporating temperature sensors to adjust for thermal drift. Voltage Regulation: Including a power management system to reduce the impact of supply variations. Noise Reduction: Shielding the oscillator circuit and using capacitive coupling to minimize noise interference, which can cause phase noise and jitter.

V. CONCLUSION & FUTURE SCOPE

NAND-based ring oscillators are versatile components in timing applications, with specific design adjustments making them suitable for precision-demanding systems. Future improvements may focus on integrating advanced compensation techniques to further enhance frequency stability, especially under variable environmental conditions.

VI. REFERENCES

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