

Wednesday, April 7, 2021

Met with team [15 min]

We decided to build an accumulator and planned when we were going to meet.

Saturday, April 10, 2021

Met with team [1 hour]

We started the design document. We determined what registers and instructions we needed and wrote out the instructions for them. We decided we would meet next to finish the design and start the assembly code.

Sunday, April 11, 2021

Met with team [1 hour 15 minutes]

We determined how each instruction was going to work and what types of addressing we would implement and started to plan for how our processor would run Euclid's algorithm. We planned to finish the design document in the next meeting.

Monday, April 12, 2021

Met with team [1hr 15 minutes]

We wrote the code fragments and Euclid's algorithm in assembly and went over the rest of the design document to finish it. We decided we would wait for feedback on our plan before we started implementing it. We also discussed setting up a compiler.

Monday, April 19, 2021

Worked on assembler [1hr]

I tried to determine how I was going to make the assembler. I decided to use java and hash maps to read instructions and convert them to machine code. Then I started making it.

Tuesday, April 20, 2021

Worked on assembler[2hr]

I wrote the assembler and it worked without too much issue.

Wednesday April 21, 2021

Worked on design document [2hr]

I wrote the machine code translation for the instruction fragments and made some other changes. We decided to change our instruction format to distinguish whether the instruction was a branch/jump or not based on the first bit of the op code so that we could have a shorter op code for the jumps and be able to jump a further distance.

Tuesday April 22, 2021

Worked on design document [1hr]

I wrote out the bottom-up testing plan. We decided that we wanted to test each component and then test them together in the groups that they will be sectioned into in the multicycle data-path.

Wednesday April 23, 2021

Worked on design document [2hr]

I wrote out the testing plan and example tests for each component. We just wrote pseudocode for now that we could later translate in to Verilog.

Sunday May 2, 2021

Worked on Verilog tests [30min]

I wrote the tests for the CRFile which was essentially loops comparing the output to the expected value for every combination of inputs.

Monday May 3, 2021

Met with group [1hr]

We discussed how we were going to implement the control signal and determined that we would write out the signals for each op code and store them in memory to be retrieved by the IR. In addition, we also planned for the next milestone and discussed our implementation plan for the data path.

Tuesday May 4, 2021

Worked on Verilog tests [30min]

I wrote the tests for SignExtender, PCALU, and started ALU/IR. The testing scheme followed the same convention as the CRFile previously mentioned.

Tuesday May 11, 2021

Worked on Testing plan, Verilog tests, and assembler [2hr]

I wrote the testing plan for the data-path, deciding to test one line of each instruction, then test some of the code fragments in our design document, and then test Euclid's algorithm. I also improved some of the Verilog tests. Some of them show up as a failure because the loop they are written in doesn't compare the edge cases but when looking at the result the test passed so we left them to display some tests as failing, knowing that they all actually passed. Finally, I added labels and sign extension to the assembler making it now fully functional for anything we may need to convert.

Wednesday May 12, 2021

Worked on subcomponents and testing [3hr]

I worked with Ian to add some mission functionality to our components and to add tests to validate that those changes worked. Additionally, we created a subcomponent for the registers and the ALU and began testing it.

Saturday May 15, 2021

Worked on testing subcomponents[2hr]

Ian and I finished testing our subcomponent and changing our plans on how to test the rest of the data-path. We decided we would just have 2 subcomponents because they were easier to test together.

Tuesday May 17, 2021

Planned out remaining work [2hr]

Worked on final testing planning and figured out how we needed to use memory to run instructions. We figured out that we use the .coe file and we planned how we were going to integrate the memory in to testing.

Wednesday May 18, 2021

Tested full data-path [2hr]

Worked with Ian to use hardcoded instructions to manually check each instruction and see if they could run both consecutively and individually without fail.

Thursday May 19, 2021

Finished data-path and testing Euclids [8hr]

Working as a group we figured out any bugs that we had in our data-path and wrote Euclid's algorithm into memory. We had some issues with the assembly code and the assembler, but eventually we got a working algorithm.