Work Log

Saturday April 10

- Met with team to begin document for initial design to complete milestone 1.
- Decided to use accumulator

Sunday April 11, 2021

- Met with team to continue work for design
- Came up with idea to have several “accumulator registers” that can be switched between to save work without including more temporary registers that continue to hold data

Monday April 12,2021

- Team meet to finish document
- Wanting to ask if we can change the size of instructions if they are j or other instructions
    - Will read opcode, if opcode first bit (most significant) is a 1 then it reads the full opcode and then reads 16 bits for an address to jump to
    - If opcode leads with 0, will read 10 bits for memory or immediate
- Made decision to just use 10 bit immediate and just sign extend them

Tuesday April 20, 2021

- Meeting for continuation of M2

  Added a table for a list of components and specifying each components signals in, out,

  and controls
- Going to use most significant bit of opcode to determine if J type

- All other instructions will start with 0 in most significant bit of instruction

  Placed all register information in a table to know their location in the register file easier

- in the document and have a convenient table following a convention

Wednesday April 21, 2021

- Talking with professor came up with design decision to use a separate cool register file for the accumulator registers and a separate register file
- Control signals will be used to determine whether we read/write to the Cr or the register file

Sunday April 26, 2021

- Drew up a rough draft for the datapath adding a couple of control signals for mux’s

Tuesday April 27, 2021

- Drew a cleaner and updated version of the datapath
- Made a small list of changes to make for a draft to upload
- Created a table including the control signals with their number of bits and description of their function
- Created a coolReg File to begin testing component
- Had errors when trying to get the schematic to synthesize due to directory issues and symbols

    - Fixed by making new project and adding them all to be in the same directory to compile together
    - Make sure all symbols/schematics are update when adding file

Sunday May 2, 2021

- Created sign extender

Monday May 3, 2021

- Created PC ALU
- Met with team to discuss more on testing and start working on control unit specs

Tuesday May 4, 2021

- Start Control unit table to summarize the control signals each signal will need
- Will complete table then make control unit for next milestone when all signals appropriate
- Also need to draw up new updated datapath to fix small issues
    - Concatenate for jumps, update to multicycle hopefully
- Fixed issues with Sign extender
    - Was copying the bit 1 spot then zero extending rest, had to look up concatenation
        - Will use the concatenation for jumping

        - PC[15:14] concatenate with left shift branch address/immediate

Monday May 12, 2021

- Finished control signal basis
    - Added control signals as datapath was drawn and deemed necessary

Tuesday May 13, 2021

- Designed Control Unit ready to test and if working implement to entire datapath
- Made decisions while creating control path
    - Instead of jal, have an instruction (SetPC) to set PC+2+immediate into the CR (so you can offset to a certain instruction if necessary but will mostly just be 0)
        - This will allow the PC current place to be written into the cool reg and then use regular Set to set the value into the $ra
            - Could probably just make SetPC to write into a chosen register instead, but this allows offsets so you can control where you return to if necessary
    - Instead of implementing Ori and Lui into the datapath, will use them as pseudo instructions.
        - Set 0 into Cr
        - Add upper 8 bits

- Shift left 8
- Add lower 8 bits