

Северо-кавказский федеральный университет
кафедра прикладной математики и математического моделирования

Лабораторная работа №2
(Вариант «Образец оформления»)
Дисциплина: Математические модели и методы синтеза СБИС
Тема: VHDL-реализация схем двоичной арифметики

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1. Постановка задачи (полное условие в соответствии с выбранным вариантом).

1. Разработать и реализовать на языке VHDL в среде проектирования Xilinx ISE 14.7 модель устройства, рассчитывающего значение арифметического выражения (в соответствии с вариантом). Синтезировать схему.

Внимание! Запрещено использовать готовые библиотечные IEEE-модули двоичной арифметики (т. е. необходимо создать свои модули для выполнения арифметических операций над двоичными числами). Разрядность входных и выходных сигналов — 32 бит.

2. Создать в среде проектирования Xilinx ISE 14.7 тестовый симулятор устройства, созданного в задании 1. Получить временные диаграммы симуляции схемы.

Арифметическое выражение варианта 000: $c = (a+b)^3 - 7a + b$

2. Подробная математическая (совокупность формул и поясняющего формулы текста) или информационной (словесное описание алгоритма) модели решения задачи.

Разобьем решение поставленной задачи на последовательность действий:

$$c = (a+b)^3 - 7a + b$$

- 1) $a_plus_b = a + b$
- 2) $a_plus_b_pow2 = a_plus_b * a_plus_b$
- 3) $a_plus_b_pow3 = a_plus_b * a_plus_b_pow2$
- 4) $a_mul_7 = a * 7$
- 5) $apbp3_minus_am7 = a_plus_b_pow3 - a_mul_7$
- 6) $c = apbp3_minus_am7 + b$

Последовательное выполнение данных действий приведет к правильному вычислению значения арифметического выражения.

Элементарные операции сложения и перемножения будем осуществлять по «школьному» алгоритму - «столбиком».

3. Тестовые наборы исходных данных и соответствующих им правильных результатов для проверки работоспособности программы.

Пусть $a=5$, $b=3$, тогда:

- 1) $a_plus_b = a + b = 5 + 3 = 8$
- 2) $a_plus_b_pow2 = a_plus_b * a_plus_b = 8 * 8 = 64$
- 3) $a_plus_b_pow3 = a_plus_b * a_plus_b_pow2 = 8 * 64 = 512$
- 4) $a_mul_7 = a * 7 = 5 * 7 = 35$
- 5) $apbp3_minus_am7 = a_plus_b_pow3 - a_mul_7 = 512 - 35 = 477$
- 6) $c = apbp3_minus_am7 + b = 477 + 3 = 480$

Ответ: $(5+3)^3 - 7*5 + 3 = 480$

4. Указание имен, типов и назначения всех переменных и сигналов, входящих в математическую или информационную модель.

a, b — `bit_vector(31 downto 0)` — входные значения сигналов

c — `bit_vector(31 downto 0)` — выходное значение (ответ)

a_plus_b , $a_plus_b_pow2$, $a_plus_b_pow3$, a_mul_7 , $apbp3_minus_am7$ - `bit_vector(31 downto 0)` — промежуточные сигналы (переменные).

5. Основной и вспомогательные (если есть) алгоритмы решения задачи (допустимо описание алгоритма на алгоритмическом языке, например, Pascal).

На языке программирования Pascal алгоритм решения поставленной задачи имеет вид:

```
program LR2_V000_Ionisyann;  
var a,b,c,  
    a_plus_b,a_plus_b_pow2,a_plus_b_pow3,a_mul_7,apbp3_minus_am7: LongInt;  
begin
```

```

writeln('a='); readln(a);
writeln('b='); readln(b);
a_plus_b:=a+b;
a_plus_b_pow2:=a_plus_b*a_plus_b;
a_plus_b_pow3:=a_plus_b*a_plus_b_pow2;
a_mul_7:=a*7;
apbp3_minus_am7:=a_plus_b_pow3-a_mul_7;
c:=apbp3_minus_am7+b;
writeln('Ответ: c=',c);
end.

```

6. Запись полных имен файлов, образующих проект с указанием назначения каждого файла (минимум указать имена и содержимое файлов с расширением .vhd (какие entity, procedure, function содержатся, что делают).

LR2_v000_Ionisyan.vhd – Реализация арифметического выражения в виде СБИС на языке VHDL

tb_LR2_v000_Ionisyan.vhd – отладочный модуль симуляции

LR2_V000_Ionisyan.xise – файл управления проектом.

bin_arith.vhd – вспомогательная библиотека компонент элементарной арифметики (созданная автором работы), включает в себя vhdл-описания:

- 1) full_adder - полный 1-битный сумматор;
- 2) bin_add – n-бит двоичный сумматор;
- 3) bin_sub – n-бит двоичный вычитатель;
- 4) bin_mul – n-бит двоичный перемножитель.

7. Полные исходные тексты VHDL-программ проекта (в каждом файле обязательно наличие информации о разработчике — ФИО, курс, группа, специальность, университет).

LR2_v000_Ionisyan.vhd – Реализация арифметического выражения в виде СБИС на языке VHDL

```

-----
-- Company: SKFU, 4PMI
-- Engineer: Ionisyan A.S.
-- Module Name: LR2_V000_Ionisyan
-- Project Name: LR2_var(000)
-----

entity LR2_V000_Ionisyan is
    Port ( a : in  bit_vector(31 downto 0);
          b : in  bit_vector(31 downto 0);
          c : out bit_vector(31 downto 0);
          clk : in  bit);
end LR2_V000_Ionisyan;

architecture Behavioral of LR2_V000_Ionisyan is
    component bin_add is
        Generic (n: integer);
        Port (op1,op2: in bit_vector(n-1 downto 0);
              res: out bit_vector(n-1 downto 0);
              clk: in bit);
    end component;

    component bin_sub is
        Generic (n: integer);
        Port (op1,op2: in bit_vector(n-1 downto 0);
              res: out bit_vector(n-1 downto 0);
              clk: in bit);
    end component;

    component bin_mul is
        Generic (n: integer);
        Port (op1,op2: in bit_vector(n-1 downto 0);
              res: out bit_vector(n-1 downto 0);

```



```

        clk : IN bit);
    END COMPONENT;

    COMPONENT LR2_V000_Ionisyan_good is
    PORT( a : in STD_LOGIC_VECTOR (31 downto 0);
          b : in STD_LOGIC_VECTOR (31 downto 0);
          c : out STD_LOGIC_VECTOR (31 downto 0);
          clk : in STD_LOGIC);
    END COMPONENT;

    --Inputs/Outputs
    signal a,b,c : bit_vector(31 downto 0);
    signal clk : bit := '0';

    signal a_good,b_good,c_good : std_logic_vector(31 downto 0);

    -- Clock period definitions
    constant clk_period : time := 100 ns;

BEGIN
    -- Instantiate the Unit Under Test (UUT)
    uut_lr2: LR2_V000_Ionisyan PORT MAP(a,b,c,clk);
    uut_good: LR2_V000_Ionisyan_good PORT MAP(a_good,b_good,c_good,to_stdulogic(clk));

    a<=bit_vector(to_unsigned(5,32));
    b<=bit_vector(to_unsigned(2,32));

    -- Clock process definitions
    clk_process :process
        variable a_tmp:integer:=0;
        variable b_tmp:integer:=0;
    begin
        clk <= '1';
        a_good<=conv_std_logic_vector(a_tmp,32);
        b_good<=conv_std_logic_vector(b_tmp,32);
        wait for clk_period/2;
        clk <= '0';
        a_tmp:=a_tmp+1;
        if a_tmp>15 then
            a_tmp:=0;
            b_tmp:=b_tmp+1;
            if b_tmp>15 then b_tmp:=0; end if;
        end if;
        wait for clk_period/2;
    end process;
END;
```

bin_arith.vhd – вспомогательная библиотека компонент элементарной арифметики

```

-- Company: SKFU, 4PMI
-- Engineer: Ionisyan A.S.
-- Module Name: LR2_V000_Ionisyan
-- Project Name: LR2_var(000)
-----
-- полный 1-битовый сумматор
-----

entity full_adder is
    Port (op1,op2,carry_in: in bit; res,carry_out: out bit; clk: in bit);
end full_adder;
architecture Behavioral of full_adder is
    signal p:bit;
begin
    process(clk)
    begin
        if (clk'event and clk = '1') then
            p<=(not(op1) and op2)or (op1 and not(op2));
            res<=(not(p) and carry_in)or(p and not(carry_in));
            carry_out<=(op1 and op2)or(p and carry_in);
        end if;
    end process;
end;
```

```

end process;
end Behavioral;

```

```

-----
-- n-бит двоичный сумматор
-----

```

```

entity bin_add is
Generic (n: integer);
Port (op1,op2: in bit_vector(n-1 downto 0);
      res: out bit_vector(n-1 downto 0);
      clk: in bit);
end bin_add;
architecture Behavioral of bin_add is
component full_adder
  Port (op1,op2,carry_in: in bit; res,carry_out: out bit; clk: in bit);
end component;
signal carry:bit_vector(n downto 0);
begin
  carry(0)<='0';
  gen: for i in 0 to n-1 generate
  begin
    adder: full_adder port map(op1(i),op2(i),carry(i),res(i),carry(i+1),clk);
  end generate;
end Behavioral;

```

```

-----
-- n-бит двоичный вычитатель
-----

```

```

entity bin_sub is
Generic (n: integer);
Port (op1,op2: in bit_vector(n-1 downto 0);
      res: out bit_vector(n-1 downto 0);
      clk: in bit);
end bin_sub;
architecture Behavioral of bin_sub is
component full_adder
  Port (op1,op2,carry_in: in bit; res,carry_out: out bit; clk: in bit);
end component;
signal carry:bit_vector(n downto 0);
begin
  carry(0)<='1';
  gen: for i in 0 to n-1 generate
  begin
    adder: full_adder port map(op1(i),not(op2(i)),carry(i),res(i),carry(i+1),clk);
  end generate;
end Behavioral;

```

```

-----
-- n-бит двоичный перемножитель (столбиком)
-----

```

```

entity bin_mul is
Generic (n: integer);
Port (op1,op2: in bit_vector(n-1 downto 0);
      res: out bit_vector(n-1 downto 0);
      clk: in bit);
end bin_mul;
architecture Behavioral of bin_mul is
component bin_add
generic(n:integer);
Port(op1,op2:in bit_vector(n-1 downto 0); res:out bit_vector(n-1 downto 0); clk: in
bit);
end component;
type T_tmp_sum is array(0 to n) of bit_vector(n-1 downto 0);
signal tmp_sum,tmp_op1: T_tmp_sum;
begin
  tmp_sum(0)<=(others=>'0');
  gen: for i in 0 to n-1 generate
  begin
    tmp_op1(i)(i-1 downto 0)<=(others=>'0');
    tmp_op1(i)(n-1 downto i)<=(others=>'0') when op2(i)='0' else op1(n-i-1 downto 0);
    adder: bin_add generic map(n) port map(tmp_sum(i),tmp_op1(i),tmp_sum(i+1),clk);
  end generate;
end Behavioral;

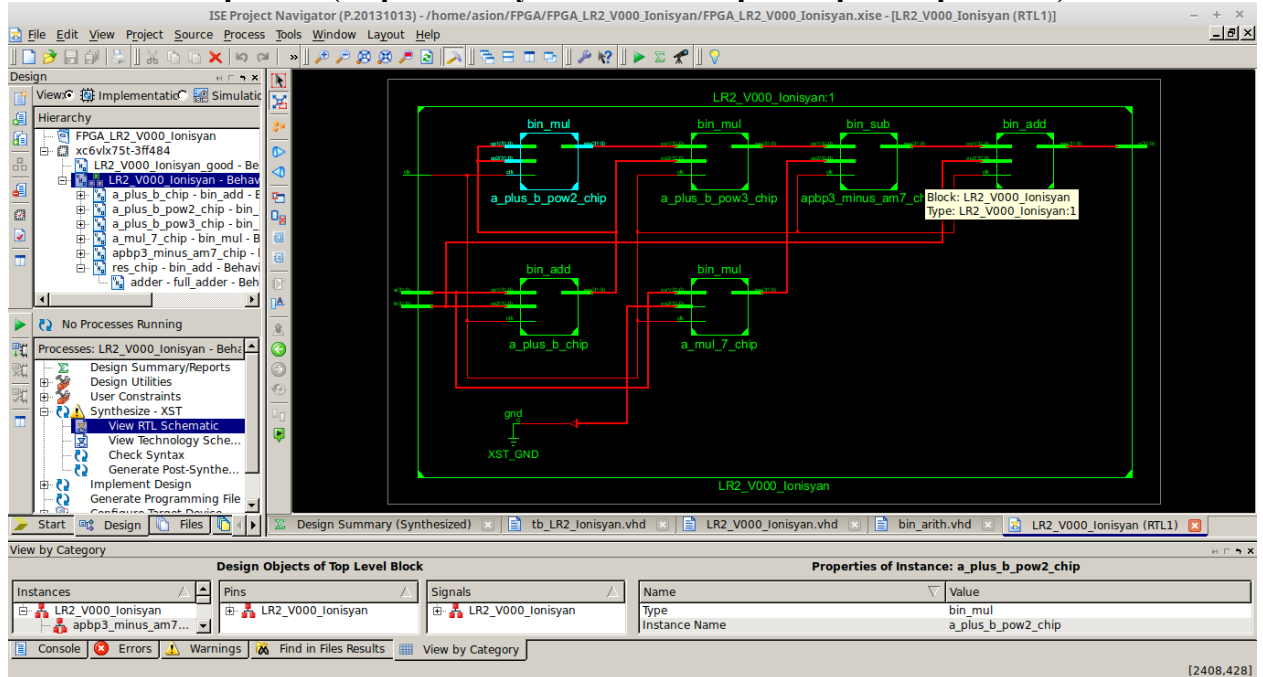
```

```

end generate;
res<=tmp_sum(n);
end Behavioral;

```

8. RTL-схема проекта (из раздела Synthesize-XST среды проектирования).



9. Содержимое файла .syf отчета синтеза и имплементации проекта.

```

Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.13 secs

```

```

-->
Parameter xsthdpdir set to xst

```

```

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.13 secs

```

```

-->
Reading design: LR2_V000_Ionisyman.prj

```

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```
=====
*                               Synthesis Options Summary                               *
=====

---- Source Parameters
Input File Name                  : "LR2_V000_Ionisyan.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters
Output File Name                 : "LR2_V000_Ionisyan"
Output Format                    : NGC
Target Device                   : xc6vlx75t-3-ff484

---- Source Options
Top Module Name                 : LR2_V000_Ionisyan
Automatic FSM Extraction        : YES
FSM Encoding Algorithm          : Auto
Safe Implementation             : No
FSM Style                       : LUT
RAM Extraction                  : Yes
RAM Style                       : Auto
ROM Extraction                  : Yes
Shift Register Extraction       : YES
ROM Style                       : Auto
Resource Sharing                : YES
Asynchronous To Synchronous   : NO
Shift Register Minimum Size     : 2
Use DSP Block                   : Auto
Automatic Register Balancing    : No

---- Target Options
LUT Combining                   : Auto
Reduce Control Sets             : Auto
Add IO Buffers                  : YES
Global Maximum Fanout           : 100000
Add Generic Clock Buffer (BUFG) : 32
Register Duplication            : YES
Optimize Instantiated Primitives : NO
Use Clock Enable                : Auto
Use Synchronous Set            : Auto
Use Synchronous Reset          : Auto
Pack IO Registers into IOBs     : Auto
Equivalent register Removal     : YES

---- General Options
Optimization Goal               : Speed
Optimization Effort             : 1
Power Reduction                 : NO
Keep Hierarchy                  : No
Netlist Hierarchy               : As_Optimized
RTL Output                      : Yes
Global Optimization             : AllClockNets
Read Cores                      : YES
Write Timing Constraints         : NO
Cross Clock Analysis            : NO
Hierarchy Separator             : /
Bus Delimiter                   : <>
Case Specifier                  : Maintain
Slice Utilization Ratio         : 100
BRAM Utilization Ratio          : 100
DSP48 Utilization Ratio         : 100
Auto BRAM Packing               : NO
Slice Utilization Ratio Delta   : 5

=====

=====
*                               HDL Parsing                               *
=====
```



```

=====
Parsing VHDL file "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd" into library
work
Parsing entity <full_adder>.
Parsing architecture <Behavioral> of entity <full_adder>.
Parsing entity <bin_add>.
Parsing architecture <Behavioral> of entity <bin_add>.
Parsing entity <bin_sub>.
Parsing architecture <Behavioral> of entity <bin_sub>.
WARNING:HDLCompiler:946 - "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd" Line
66: Actual for formal port op2 is neither a static name nor a globally static
expression
Parsing entity <bin_mul>.
Parsing architecture <Behavioral> of entity <bin_mul>.
Parsing VHDL file "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/LR2_V000_Ionisyan.vhd" into
library work
Parsing entity <LR2_V000_Ionisyan>.
Parsing architecture <Behavioral> of entity <lr2_v000_ionisyan>.
Parsing entity <LR2_V000_Ionisyan_good>.
Parsing architecture <Behavioral> of entity <lr2_v000_ionisyan_good>.

```

```

=====
*                               HDL Elaboration                               *
=====

```

```

Elaborating entity <LR2_V000_Ionisyan> (architecture <Behavioral>) from library
<work>.

```

```

Elaborating entity <bin_add> (architecture <Behavioral>) with generics from library
<work>.

```

```

Elaborating entity <full_adder> (architecture <Behavioral>) from library <work>.

```

```

Elaborating entity <bin_mul> (architecture <Behavioral>) with generics from library
<work>.

```

```

WARNING:HDLCompiler:746 - "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd" Line
90: Range is empty (null range)

```

```

WARNING:HDLCompiler:220 - "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd" Line
90: Assignment ignored

```

```

Elaborating entity <bin_sub> (architecture <Behavioral>) with generics from library
<work>.

```

```

=====
*                               HDL Synthesis                               *
=====

```

```

Synthesizing Unit <LR2_V000_Ionisyan>.
  Related source file is
"/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/LR2_V000_Ionisyan.vhd".

```

```

  Summary:
    no macro.
Unit <LR2_V000_Ionisyan> synthesized.

```

```

Synthesizing Unit <bin_add>.
  Related source file is "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd".
    n = 32

```

```

INFO:Xst:3210 - "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd" line 44:
Output port <carry_out> of the instance <gen[31].adder> is unconnected or connected to
loadless signal.

```

```

  Summary:
    no macro.
Unit <bin_add> synthesized.

```

```

Synthesizing Unit <full_adder>.
  Related source file is "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd".
  Found 1-bit register for signal <res>.
  Found 1-bit register for signal <carry_out>.
  Found 1-bit register for signal <p>.
  Summary:
    inferred    3 D-type flip-flop(s).

```

Unit <full_adder> synthesized.

Synthesizing Unit <bin_mul>.

Related source file is "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd".
n = 32

Summary:

inferred 32 Multiplexer(s).

Unit <bin_mul> synthesized.

Synthesizing Unit <bin_sub>.

Related source file is "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd".
n = 32

INFO:Xst:3210 - "/home/asion/FPGA/FPGA_LR2_V000_Ionisyan/bin_arith.vhd" line 66:

Output port <carry_out> of the instance <gen[31].adder> is unconnected or connected to loadless signal.

Summary:

no macro.

Unit <bin_sub> synthesized.

=====

HDL Synthesis Report

Macro Statistics

# Registers	: 9504
1-bit register	: 9504
# Multiplexers	: 96
1-bit 2-to-1 multiplexer	: 3
10-bit 2-to-1 multiplexer	: 3
11-bit 2-to-1 multiplexer	: 3
12-bit 2-to-1 multiplexer	: 3
13-bit 2-to-1 multiplexer	: 3
14-bit 2-to-1 multiplexer	: 3
15-bit 2-to-1 multiplexer	: 3
16-bit 2-to-1 multiplexer	: 3
17-bit 2-to-1 multiplexer	: 3
18-bit 2-to-1 multiplexer	: 3
19-bit 2-to-1 multiplexer	: 3
2-bit 2-to-1 multiplexer	: 3
20-bit 2-to-1 multiplexer	: 3
21-bit 2-to-1 multiplexer	: 3
22-bit 2-to-1 multiplexer	: 3
23-bit 2-to-1 multiplexer	: 3
24-bit 2-to-1 multiplexer	: 3
25-bit 2-to-1 multiplexer	: 3
26-bit 2-to-1 multiplexer	: 3
27-bit 2-to-1 multiplexer	: 3
28-bit 2-to-1 multiplexer	: 3
29-bit 2-to-1 multiplexer	: 3
3-bit 2-to-1 multiplexer	: 3
30-bit 2-to-1 multiplexer	: 3
31-bit 2-to-1 multiplexer	: 3
32-bit 2-to-1 multiplexer	: 3
4-bit 2-to-1 multiplexer	: 3
5-bit 2-to-1 multiplexer	: 3
6-bit 2-to-1 multiplexer	: 3
7-bit 2-to-1 multiplexer	: 3
8-bit 2-to-1 multiplexer	: 3
9-bit 2-to-1 multiplexer	: 3

=====

* Advanced HDL Synthesis *

=====

WARNING:Xst:1293 - FF/Latch <carry_out> has a constant value of 0 in block <gen[7].adder>. This FF/Latch will be trimmed during the optimization process.
WARNING:Xst:1293 - FF/Latch <carry_out> has a constant value of 0 in block <gen[6].adder>. This FF/Latch will be trimmed during the optimization process.
WARNING:Xst:1293 - FF/Latch <carry_out> has a constant value of 0 in block <gen[5].adder>. This FF/Latch will be trimmed during the optimization process.

[illegible]

[illegible]

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WARNING:Xst:1293 - FF/Latch <carry_out> has a constant value of 0 in block <gen[25].adder>. This FF/Latch will be trimmed during the optimization process.
 WARNING:Xst:1293 - FF/Latch <carry_out> has a constant value of 0 in block <gen[24].adder>. This FF/Latch will be trimmed during the optimization process.
 WARNING:Xst:1293 - FF/Latch <carry_out> has a constant value of 0 in block <gen[23].adder>. This FF/Latch will be trimmed during the optimization process.

=====
 Advanced HDL Synthesis Report

Macro Statistics

# Registers	: 9504
Flip-Flops	: 9504
# Multiplexers	: 96
1-bit 2-to-1 multiplexer	: 3
10-bit 2-to-1 multiplexer	: 3
11-bit 2-to-1 multiplexer	: 3
12-bit 2-to-1 multiplexer	: 3
13-bit 2-to-1 multiplexer	: 3
14-bit 2-to-1 multiplexer	: 3
15-bit 2-to-1 multiplexer	: 3
16-bit 2-to-1 multiplexer	: 3
17-bit 2-to-1 multiplexer	: 3
18-bit 2-to-1 multiplexer	: 3
19-bit 2-to-1 multiplexer	: 3
2-bit 2-to-1 multiplexer	: 3
20-bit 2-to-1 multiplexer	: 3
21-bit 2-to-1 multiplexer	: 3
22-bit 2-to-1 multiplexer	: 3
23-bit 2-to-1 multiplexer	: 3
24-bit 2-to-1 multiplexer	: 3
25-bit 2-to-1 multiplexer	: 3
26-bit 2-to-1 multiplexer	: 3
27-bit 2-to-1 multiplexer	: 3
28-bit 2-to-1 multiplexer	: 3
29-bit 2-to-1 multiplexer	: 3
3-bit 2-to-1 multiplexer	: 3
30-bit 2-to-1 multiplexer	: 3
31-bit 2-to-1 multiplexer	: 3
32-bit 2-to-1 multiplexer	: 3
4-bit 2-to-1 multiplexer	: 3
5-bit 2-to-1 multiplexer	: 3
6-bit 2-to-1 multiplexer	: 3
7-bit 2-to-1 multiplexer	: 3
8-bit 2-to-1 multiplexer	: 3
9-bit 2-to-1 multiplexer	: 3

=====

=====
 * Low Level Synthesis *

WARNING:Xst:2677 - Node <gen[31].adder/carry_out> of sequential type is unconnected in block <bin_add>.
 WARNING:Xst:2677 - Node <gen[31].adder/carry_out> of sequential type is unconnected in block <bin_sub>.

Optimizing unit <LR2_V000_Ionisyany> ...

Optimizing unit <bin_add> ...

Optimizing unit <bin_mul> ...

Optimizing unit <bin_sub> ...

WARNING:Xst:1710 - FF/Latch <a_mul_7_chip/gen[10].adder/gen[1].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyany>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <a_mul_7_chip/gen[10].adder/gen[2].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyany>. This FF/Latch will be trimmed during the optimization process.

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constant value of 0 in block <LR2_V000_Ionisyan>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<a_plus_b_pow2_chip/gen[14].adder/gen[4].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyan>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<a_plus_b_pow2_chip/gen[14].adder/gen[5].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyan>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<a_plus_b_pow2_chip/gen[14].adder/gen[6].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyan>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<a_plus_b_pow2_chip/gen[14].adder/gen[7].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyan>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<a_plus_b_pow2_chip/gen[14].adder/gen[8].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyan>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<a_plus_b_pow2_chip/gen[14].adder/gen[9].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyan>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch

<a_plus_b_pow2_chip/gen[14].adder/gen[10].adder/carry_out> (without init value) has a constant value of 0 in block <LR2_V000_Ionisyan>. This FF/Latch will be trimmed during the optimization process.

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block LR2_V000_Ionisyan, actual ratio is 23.

FlipFlop a_plus_b_chip/gen[1].adder/res has been replicated 1 time(s)

FlipFlop a_plus_b_chip/gen[2].adder/res has been replicated 1 time(s)

Final Macro Processing ...

Processing Unit <LR2_V000_Ionisyan> :

Found 3-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[30].adder/res>.

Found 5-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[29].adder/res>.

Found 7-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[28].adder/res>.

Found 9-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[27].adder/res>.

Found 11-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[26].adder/res>.

Found 13-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[25].adder/res>.

Found 15-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[24].adder/res>.

Found 17-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[23].adder/res>.

Found 19-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[22].adder/res>.

Found 21-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[21].adder/res>.

Found 23-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[20].adder/res>.

Found 25-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[19].adder/res>.

Found 27-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[18].adder/res>.

Found 29-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[17].adder/res>.

Found 31-bit shift register for signal

<a_plus_b_pow3_chip/gen[31].adder/gen[16].adder/res>.

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```

    Found 58-bit shift register for signal
<a_mul_7_chip/gen[31].adder/gen[4].adder/res>.
    Found 58-bit shift register for signal
<a_mul_7_chip/gen[31].adder/gen[3].adder/res>.
    Found 59-bit shift register for signal
<a_mul_7_chip/gen[31].adder/gen[2].adder/res>.
    Found 61-bit shift register for signal
<a_mul_7_chip/gen[31].adder/gen[1].adder/res>.
    Found 64-bit shift register for signal
<a_mul_7_chip/gen[31].adder/gen[0].adder/res>.
Unit <LR2_V000_Ionisyan> processed.

```

```

=====
Final Register Report

```

```

Macro Statistics

```

```

# Registers : 3445
Flip-Flops : 3445
# Shift Registers : 125
11-bit shift register : 2
13-bit shift register : 2
15-bit shift register : 2
17-bit shift register : 2
19-bit shift register : 2
2-bit shift register : 31
21-bit shift register : 2
23-bit shift register : 2
25-bit shift register : 2
27-bit shift register : 2
29-bit shift register : 2
3-bit shift register : 2
31-bit shift register : 2
33-bit shift register : 2
35-bit shift register : 2
37-bit shift register : 2
39-bit shift register : 2
41-bit shift register : 2
43-bit shift register : 2
45-bit shift register : 2
47-bit shift register : 2
49-bit shift register : 2
5-bit shift register : 2
51-bit shift register : 2
53-bit shift register : 2
55-bit shift register : 2
57-bit shift register : 2
58-bit shift register : 29
59-bit shift register : 3
61-bit shift register : 3
63-bit shift register : 1
64-bit shift register : 2
7-bit shift register : 2
9-bit shift register : 2

```

```

=====
* Partition Report *
=====

```

```

Partition Implementation Status
-----

```

```

    No Partitions were found in this design.
-----

```

```

=====
* Design Summary *
=====

```

Top Level Output File Name : LR2_V000_Ionisyan.ngc

Primitive and Black Box Usage:

```
-----
# BELS : 3379
# GND : 1
# INV : 1
# LUT2 : 1321
# LUT3 : 1038
# LUT4 : 162
# LUT5 : 855
# VCC : 1
# FlipFlops/Latches : 3570
# FD : 3445
# FDE : 125
# Shift Registers : 187
# SRLC16E : 47
# SRLC32E : 140
# Clock Buffers : 1
# BUFGP : 1
# IO Buffers : 96
# IBUF : 64
# OBUF : 32
```

Device utilization summary:

Selected Device : 6vlx75tff484-3

Slice Logic Utilization:

Number of Slice Registers:	3570	out of	93120	3%
Number of Slice LUTs:	3564	out of	46560	7%
Number used as Logic:	3377	out of	46560	7%
Number used as Memory:	187	out of	16720	1%
Number used as SRL:	187			

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	3632			
Number with an unused Flip Flop:	62	out of	3632	1%
Number with an unused LUT:	68	out of	3632	1%
Number of fully used LUT-FF pairs:	3502	out of	3632	96%
Number of unique control sets:	2			

IO Utilization:

Number of IOs:	97			
Number of bonded IOBs:	97	out of	240	40%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs:	1	out of	32	3%
---------------------------	---	--------	----	----

Partition Resource Summary:

No Partitions were found in this design.

=====

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

-----+-----+-----+

Clock Signal	Clock buffer(FF name)	Load	
--------------	-----------------------	------	--


```

-----+-----+-----+
clk                                     | BUFGP                               | 3757 |
-----+-----+-----+

```

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

Minimum period: 1.257ns (Maximum Frequency: 795.545MHz)
 Minimum input arrival time before clock: 0.565ns
 Maximum output required time after clock: 0.562ns
 Maximum combinational path delay: No path found

Timing Details:

All values displayed in nanoseconds (ns)

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 1.257ns (frequency: 795.545MHz)

Total number of paths / destination ports: 10721 / 3692

Delay: 1.257ns (Levels of Logic = 0)
 Source: a_plus_b_pow3_chip/gen[31].adder/gen[14].adder/Mshreg_res_0 (FF)
 Destination: a_plus_b_pow3_chip/gen[31].adder/gen[14].adder/Mshreg_res_1 (FF)
 Source Clock: clk rising
 Destination Clock: clk rising

Data Path: a_plus_b_pow3_chip/gen[31].adder/gen[14].adder/Mshreg_res_0 to
 a_plus_b_pow3_chip/gen[31].adder/gen[14].adder/Mshreg_res_1

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
SRLC32E:CLK->Q31	1	1.099	0.000	
a_plus_b_pow3_chip/gen[31].adder/gen[14].adder/Mshreg_res_0				
(a_plus_b_pow3_chip/gen[31].adder/gen[14].adder/Mshreg_res_0)				
SRLC32E:D		0.158		
a_plus_b_pow3_chip/gen[31].adder/gen[14].adder/Mshreg_res_1				
Total		1.257ns	(1.257ns logic, 0.000ns route)	(100.0% logic, 0.0% route)

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 341 / 278

Offset: 0.565ns (Levels of Logic = 2)
 Source: a<1> (PAD)
 Destination: a_plus_b_chip/gen[1].adder/carry_out (FF)
 Destination Clock: clk rising

Data Path: a<1> to a_plus_b_chip/gen[1].adder/carry_out

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	7	0.003	0.509	a_1_IBUF (a_1_IBUF)
LUT4:I0->O	1	0.053	0.000	a_plus_b_chip/gen[1].adder/op1_p_OR_3_o1
(a_plus_b_chip/gen[1].adder/op1_p_OR_3_o)				
FD:D		-0.012		a_plus_b_chip/gen[1].adder/carry_out
Total		0.565ns	(0.056ns logic, 0.509ns route)	(9.9% logic, 90.1% route)

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 32 / 32

Offset: 0.562ns (Levels of Logic = 1)
Source: res_chip/gen[31].adder/res (FF)
Destination: c<31> (PAD)
Source Clock: clk rising

Data Path: res_chip/gen[31].adder/res to c<31>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FD:C->Q (res_chip/gen[31].adder/res)	1	0.280	0.279	res_chip/gen[31].adder/res
OBUF:I->O		0.003		c_31_OBUF (c<31>)
Total		0.562ns	(0.283ns logic, 0.279ns route) (50.3% logic, 49.7% route)	

Cross Clock Domains Report:

Clock to Setup on destination clock clk

Source Clock	Dest:Rise	Dest:Fall	Src:Rise	Src:Fall
clk	1.257			

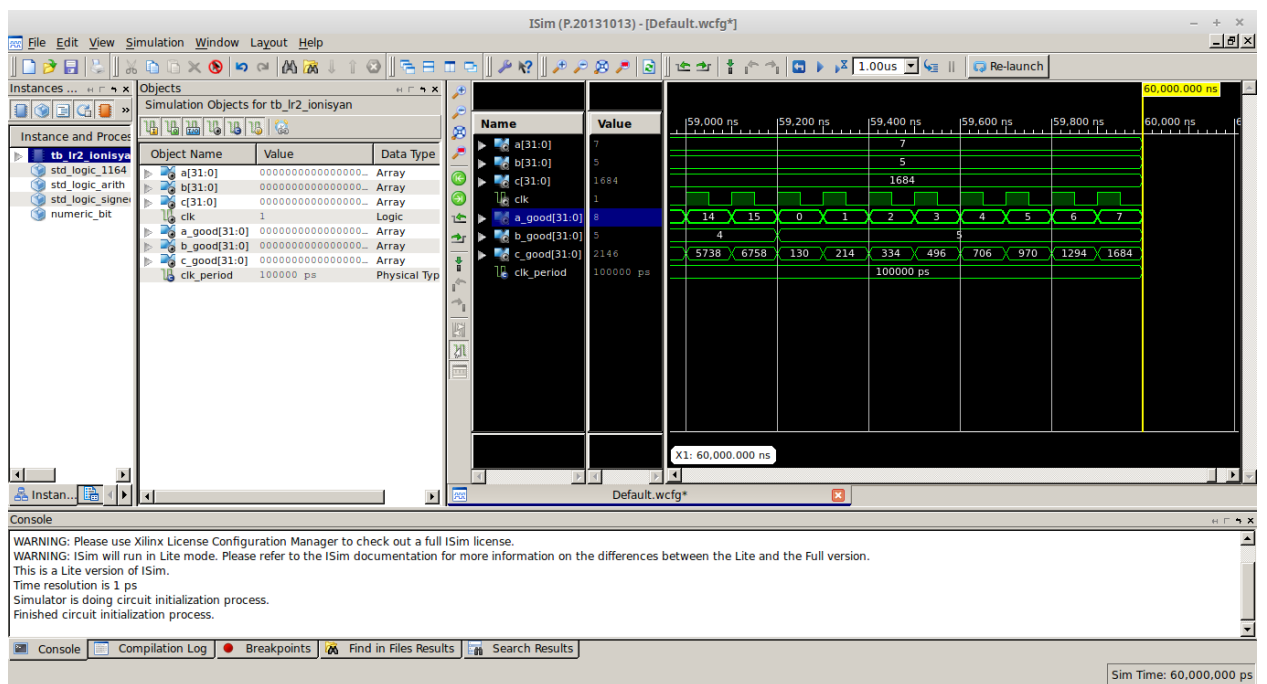
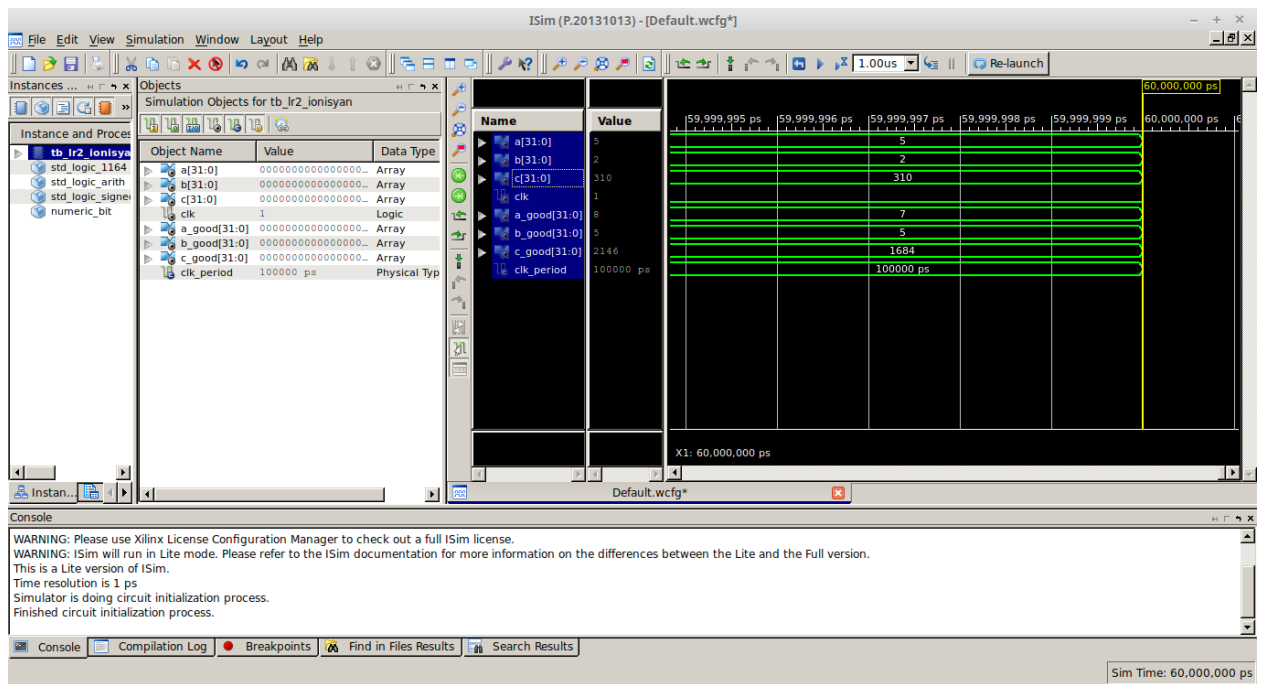
Total REAL time to Xst completion: 66.00 secs
Total CPU time to Xst completion: 61.35 secs

-->

Total memory usage is 480128 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 3573 (0 filtered)
Number of infos : 2 (0 filtered)

10. Энергопотребление схемы в Ваттах (содержимое таблиц XPower Analyzer среды проектирования).



13. Выводы о проделанной работе.

Мы разработали и реализовали в среде проектирования СБИС Xilinx ISE 14.7 принципиальную схему устройства рассчитывающую значения арифметической функции, синтезировали схему, проверили ее работоспособность на нескольких тестовых наборах входных данных. Существенным недостатком данной схемы является неоптимальная работа библиотеки элементарной арифметики, особенно реализация операции умножения, из-за чего схема не может быть использована в реальных приложениях.