Северо-кавказский федеральный университет
кафедра прикладной математики и математического моделирования

Лабораторная работа №3
(Вариант «Образец оформления»)
Дисциплина: Математические модели и методы синтеза СБИС
Тема: VHDL-реализация схем модулярной арифметики

Выполнил: преподаватель группы ПМИ-121
Ионисян А.С.

Ставрополь, 2016

1. Постановка задачи (полное условие в соответствии с выбранным вариантом).

1. Разработать и реализовать на языке VHDL в среде проектирования Xilinx ISE 14.7 модель устройства:

а) выполняющего перевод входных данных из двоичной системы счисления в систему остаточных классов

б) рассчитывающего значение арифметического выражения в системе остаточных классов (в соответствии с вариантом)

в) выполняющего перевод полученного результата из системы остаточных классов в двоичную систему счисления.

г) Синтезировать схему.

Разрешено использовать готовые библиотечные IEEE-модули двоичной арифметики. Разрядность входных и выходных сигналов — 32 бит.

2. Создать в среде проектирования Xilinx ISE 14.7 тестовый симулятор устройства, созданного в задании 1. Получить временные диаграммы симуляции схемы.

Арифметическое выражение варианта 000: $c=(a+b)^3-7a+b$

основания СОК: (173,229,181,233,239)

2. Подробная математическая (совокупность формул и поясняющего формулы текста) или информационной (словесное описание алгоритма) модели решения задачи.

Разобьем решение поставленной задачи на последовательность действий:

c=(a+b)^3-7a+b

```
0) перевод a,b из двоичной СС в СОК a_RNS, b_RNS
1) a_plus_b=a_RNS+b_RNS
2) a_plus_b_pow2=a_plus_b*a_plus_b
3) a_plus_b_pow3=a_plus_b*a_plus_b_pow2
4) a_mul_7=a_RNS*7
5) apbp3_minus_am7=a_plus_b_pow3-a_mul_7
6) c_RNS=apbp3_minus_am7+b_RNS
7) перевод c_RNS из СОК в двоичную систему счисления - c
```

Последовательное выполнение данных действий приведет к правильному вычислению значения арифметического выражения.

Для выполнения операций в СОК будем использовать математические модели и методы, описанные в статье «Алгоритмы и методы модулярной арифметики на основе интервальных характеристик чисел»(Ионисян А.С.). //Сборник научных трудов I-й международной конференции «Параллельная компьютерная алгебра и ее приложения в новых инфокоммуникационных системах». – Ставрополь.: Фабула, 2014 г. – С. 206-214.

3. Тестовые наборы исходных данных и соответствующих им правильных результатов для проверки работоспособности программы.

Пусть a=5, b=3, p1=173, p2=229, p3=181, p4=233, p5=239 тогда:

```
0) a_RNS=PSS_to_RNS(5)=(5,5,5,5,5); b_RNS=PSS_to_RNS(3)=(3,3,3,3,3)
1) a_plus_b=a_RNS+b_RNS=(5,5,5,5,5)+(3,3,3,3,3)=(8,8,8,8,8)
2) a_plus_b_pow2=a_plus_b*a_plus_b=(8,8,8,8,8)*(8,8,8,8,8)=(64,64,64,64,64)
3) a_plus_b_pow3=a_plus_b*a_plus_b_pow2=(8,8,8,8,8)*(64,64,64,64,64)=
=(512,512,512,512,512)=(166,54,150,46,34)
4) a_mul_7=a_RNS*7=(5,5,5,5,5)*(7,7,7,7,7)=(35,35,35,35,35)
5) apbp3_minus_am7=a_plus_b_pow3-a_mul_7=(166,54,150,46,34)-(35,35,35,35,35)=
=(131,19,115,11,238)
6) c_RNS=apbp3_minus_am7+b_RNS=(131,19,115,11,238)+(3,3,3,3,3)=
=(133,22,118,14,2)
7) c=RNS_to_PSS(133,22,118,14,2)=480
```

Ответ: $(5+3)^3-7*5+3=480$

4. Указание имен, типов и назначения всех переменных и сигналов, входящих в математическую или информационную модель.
a,b — t_bin_data — входные значения сигналов 32-битовое целое
c — t_bin_data — выходное значение (ответ) 32-битовое целое
a_RNS, b_RNS, c_RNS, a_plus_b, a_plus_b_pow2, a_plus_b_pow3, a_mul_7, apbp3_minus_am7 - T_RNS_vector — промежуточные сигналы (переменные) — типа вектора из чисел заданной СОК.

5. Основной и вспомогательные (если есть) алгоритмы решения задачи (допустимо описание алгоритма на алгоритмическом языке, например, Pascal).
На языке программирования Pascal алгоритм решения поставленной задачи имеет вид:

```
program LR2_V000_Ionisyan;
var a,b,c:LongInt;
 a_RNS,b_RNS,c_RNS: T_RNS_vector;
 a_plus_b,a_plus_b_pow2,a_plus_b_pow3,a_mul_7,apbp3_minus_am7: T_RNS_vector;
begin
   writeln('a='); readln(a);
   writeln('b='); readln(b);
   a_RNS:=PSS_to_RNS(a);
   b_RNS:=PSS_to_RNS(b);
   a_plus_b:=RNS_add(a,b);
   a_plus_b_pow2:=RNS_mul(a_plus_b,a_plus_b);
   a_plus_b_pow3:=RNS_mul(a_plus_b,a_plus_b_pow2);
   a_mul_7:=RNS_mul(a_RNS,PSS_to_RNS(7));
   apbp3_minus_am7:=RNS_sub(a_plus_b_pow3,a_mul_7);
   c_RNS:=RNS_add(apbp3_minus_am7,b_RNS);
   c:=RNS_to_PSS(c_RNS);
   writeln('Ответ: c=',c);
end.
```

6. Запись полных имен файлов, образующих проект с указанием назначения каждого файла (минимум указать имена и содержимое файлов с расширением .vhd (какие entity, procedure, function содержатся, что делают).
LR3_v000_Ionisyan.vhd – Реализация арифметического выражения в виде СБИС на языке VHDL
tb_LR3_v000_Ionisyan.vhd – отладочный модуль симуляции
LR3_V000_Ionisyan.xise – файл управления проектом.
RNS_defs_pkg.vhd – вспомогательная библиотека подпрограмм работы с числами в СОК (созданная автором курса) – практически полный комплект операций над числами в СОК (до 54 оснований, каждое из которых – простое 8-битное число).
ALU_RNS_mods.vhd – entity компонент работы с сигналами в СОК (операции сложения, умножения, смены знака, нахождения обратного числа, сравнения чисел в СОК)
RNS_conv_mods.vhd – entity компонент работы с сигналами в СОК (операции перевода СОК<--->ОПСС<--->ПСС)

7. Полные исходные тексты VHDL-программ проекта (в каждом файле обязательно наличие информации о разработчике — ФИО, курс, группа, специальность, университет).

LR3_v000_Ionisyan.vhd – Реализация арифметического выражения в виде СБИС на языке VHDL

```
----------------------------------------------------------------------------------
-- Company: SKFU, 4PMI
-- Engineer: prepod, Ionisyan A.S.
-- Project Name: LR3_var(000)
-- formula: c=(a+b)^3-7a+b
```

```
-- a,b,c - 32bit BSS numbers
-- RNS primes is (173,229,181,233,239)
----------------------------------------------------------------------------------
library IEEE;
USE ieee.std_logic_1164.ALL;
USE work.RNS_defs_pkg.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity LR3_V000_Ionisyan is
    Port ( a : in  T_bin_data;
           b : in  T_bin_data;
           c : out  T_bin_data;
           clk : in  std_logic);
end LR3_V000_Ionisyan;

architecture Behavioral of LR3_V000_Ionisyan is
   COMPONENT PSS_RNS_module
    Port (clock: std_logic; A: in T_bin_data; result: out T_RNS_vector);
    END COMPONENT;

   component RNS_PSS_module
   Port (clock: std_logic; A: in T_RNS_vector; result: out T_bin_data);
   end component;

   component RNS_ALU_neg is
      Port (clock: std_logic; A: in T_RNS_vector; result: out T_RNS_vector);
   end component;

   component RNS_ALU_inv is
      Port (clock: std_logic; A: in T_RNS_vector; result: out T_RNS_vector);
   end component;

   component RNS_ALU_add is
      Port (clock: std_logic; op1, op2: in T_RNS_vector; result: out T_RNS_vector);
   end component;

   component RNS_ALU_mul is
      Port (clock: std_logic; op1, op2: in T_RNS_vector; result: out T_RNS_vector);
   end component;

   component RNS_ALU_cmp_equ
      Port (clock: std_logic; op1, op2: in T_RNS_vector; result: out STD_LOGIC);
   end component;

   component RNS_ALU_cmp_g
      Port (clock: std_logic; op1, op2: in T_RNS_vector; result: out STD_LOGIC);
   end component;

   signal a_RNS,b_RNS,c_RNS:T_RNS_vector;
   signal a_plus_b,a_plus_b_pow2,a_plus_b_pow3: T_RNS_vector;
   signal apbp3_minus_am7,neg_a_mul_7,a_mul_7,seven_RNS:T_RNS_vector;
   signal seven:T_bin_data;

begin

--c=(a+b)^3-7a+b
--0) a_RNS=PSS_to_SOK(a); b_RNS=PSS_to_SOK(b)
a_to_aRNS_chip: PSS_RNS_module port map(clk,a,a_RNS);
b_to_bRNS_chip: PSS_RNS_module port map(clk,b,b_RNS);
--1) a_plus_b=a_RNS+b_RNS
a_plus_b_chip: RNS_ALU_add port map(clk,a_RNS,b_RNS,a_plus_b);
--2) a_plus_b_pow2=a_plus_b*a_plus_b
a_plus_b_pow2_chip: RNS_ALU_mul port map(clk,a_plus_b,a_plus_b,a_plus_b_pow2);
--3) a_plus_b_pow3=a_plus_b*a_plus_b_pow2
a_plus_b_pow3_chip: RNS_ALU_mul port map(clk,a_plus_b_pow2,a_plus_b,a_plus_b_pow3);
--4) a_mul_7=a_RNS*7
seven<="00000000000000000000000000000111";
seven_to_RNS_chip: PSS_RNS_module port map(clk,seven,seven_RNS);
a_mul_7_chip: RNS_ALU_mul port map(clk,a_RNS,seven_RNS,a_mul_7);
--5) apbp3_minus_am7=a_plus_b_pow3-a_mul_7
```

```
neg_apbp3_minus_am7_chip: RNS_ALU_neg port map(clk,a_mul_7,neg_a_mul_7);
apbp3_minus_am7_chip: RNS_ALU_add port
map(clk,a_plus_b_pow3,neg_a_mul_7,apbp3_minus_am7);
--6) c_RNS=apbp3_minus_am7+b
cRNS_chip: RNS_ALU_add port map(clk,apbp3_minus_am7,b_RNS,c_RNS);
--7) c=RNS_to_PSS(c_RNS);
cRNS_to_c_chip: RNS_PSS_module port map(clk,c_RNS,c);
end Behavioral;
```

tb_LR3_v000_Ionisyan.vhd – отладочный модуль симуляции

```
----------------------------------------------------------------------------------
-- Company: SKFU, 4PMI
-- Engineer: prepod, Ionisyan A.S.
-- Project Name: LR3_var(000) testbench
-- formula: c=(a+b)^3-7a+b
-- a,b,c - 32bit BSS numbers
-- RNS primes is (173,229,181,233,239)
----------------------------------------------------------------------------------
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE work.RNS_defs_pkg.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

ENTITY tb_LR3_V000_Ionisyan IS
END tb_LR3_V000_Ionisyan;

ARCHITECTURE behavior OF tb_LR3_V000_Ionisyan IS

component LR3_V000_Ionisyan is
    Port ( a : in  T_bin_data;
           b : in  T_bin_data;
           c : out  T_bin_data;
           clk : in  std_logic);
end component;


   --Inputs
   signal clock : std_logic := '0';
   signal a,b : T_bin_data := (others => '0');
      --Outputs
   signal c : T_bin_data := (others => '0');
   -- Clock period definitions
   constant clock_period : time := 10 ns;

BEGIN

      -- Instantiate the Unit Under Test (UUT)
   LR3_v000_Ionisyan_chip: LR3_V000_Ionisyan PORT MAP (a,b,c,clock);

   -- Clock process definitions
   clk_process :process
   begin
             clock <= '0';
             wait for clock_period/2;
             clock <= '1';
             wait for clock_period/2;
   end process;

   -- Stimulus process
   stim_proc: process
   begin
      wait for (clock_period*9)/10;
      A<="00000000000000000000000000000101";
      B<="00000000000000000000000000000011";
      wait for clock_period/10;
   end process;
END;
```

RNS_defs_pkg.vhd – вспомогательная библиотека подпрограмм работы с числами в СОК

```
----------------------------------------------------------------------------------
-- Company: SKFU, 4PMI
-- Engineer: prepod, Ionisyan A.S.
-- a,b,c - 32bit BSS numbers
-- RNS primes is (173,229,181,233,239)
----------------------------------------------------------------------------------

--Copyright 2015 Andrey S. Ionisyan
--Licensed under the Apache License, Version 2.0 (the "License");
--you may not use this file except in compliance with the License.
--You may obtain a copy of the License at
--    http://www.apache.org/licenses/LICENSE-2.0
--Unless required by applicable law or agreed to in writing, software
--distributed under the License is distributed on an "AS IS" BASIS,
--WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
--See the License for the specific language governing permissions and
--limitations under the License.

-- модуль определений типов данных, констант, хранимых в ROM
-- и вспомогательных подпрограмм
-----------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

package RNS_defs_pkg is

--8-битовое целое
subtype uint_8bit is natural range 0 to 255;
--9-битовое целое (используется при обработке результатов 8-бит+8-бит)
subtype uint_9bit is natural range 0 to 511;
--множество всех 8-битных чисел от 0 до 255
type T_uint_8bit_set is array(0 to 255) of uint_8bit;
--множество всех 8-битных чисел от 0 до 511
--используется при табличной выборке результатов операций 8-бит+8-бит
type T_uint_9bit_set is array(0 to 511) of uint_8bit;

--число СОК-регистров микропроцессора
constant RNS_regs_num: natural range 1 to 16 := 8;
--число двоичных регистров микропроцессора
constant bin_regs_num: natural range 1 to 16 := 8;

--число бит в двоичных числах, подаваемых на вход микропроцессора и снимаеых с его
выхода
--(ширина шины данных микропроцессора)
constant bin_data_width: natural range 1 to 256 := 32;
--тип шины двоичных данных (для передачи шины в подпрограммы и модули)
subtype T_bin_data is unsigned(bin_data_width-1 downto 0);

--тип массивов для хранененния вспомогательных величин, например остатков СОК,
--для каждого разряда обрабатываемого двоичного числа.
--используется, например, для описания таблицы значений степеней числа 2, переведенных
в СОК
type T_bin_data_width_set is array(0 to bin_data_width-1) of uint_8bit;

--тип для хранения дерева (используется в быстрых алгоритмах бинарного сдваивания)
--если корень имеет индекс i, то левое поддерево имеет индекс 2*i, правое поддерево
2*i+1
type T_tree_array is array(1 to 2*bin_data_width-1)of uint_8bit;

-----------------------------------------------------------
--8-битные константы СОК, хранимые в ПЗУ
-----------------------------------------------------------
--максимально допустимое число оснований СОК (54 -это числов всех простых 8-битных
чисел)
constant RNS_P_num_max: natural range 1 to 54 := 54;
type T_RNS_vector_max is array(1 to RNS_P_num_max) of uint_8bit;
```

```
--подпрограмма генерации всех простых числе от 2 до RNS_P_num_max-го простого числа
function gen_primes_8bit return T_RNS_vector_max;
--работает достаточно долго, поэтому имеет смысл заполнить массив простых чисел
константами
--если нужна именно генерация, то раскомментировать gen_primes_8bit
constant primes_8bit: T_RNS_vector_max --:= gen_primes_8bit;
 := ( 2,3,5,7,11,13,17,19,23,29,31,37,41,43,47,53,59,61,67,71,73,79,83,89,97,101,
      103,107,109,113,127,131,137,139,149,151,157,163,167,173,179,181,191,193,197,
      199,211,223,227,229,233,239,241,251 );

--число реально используемых оснований СОК
constant RNS_P_num: natural range 1 to RNS_P_num_max := 5;
type T_RNS_vector is array(1 to RNS_P_num) of uint_8bit;
--в массиве RNS_primes_order хранятся номера оснований из главного массива
primes_8bit[]
--так, 3-му основанию соответствует 3-е простое число 5, 7- му -> 17, 8-му -> 19.
constant RNS_primes_order: T_RNS_vector := (40,50,42,51,52);
--так как постоянно вести индексную адресацию неудобно, то используется массив
RNS_primes[],
--в котором хранятся уже не индексы оснований, а конкретные числа.
function gen_RNS_primes return T_RNS_vector;
constant RNS_primes: T_RNS_vector := gen_RNS_primes;

------------------------------------------------------------
--для быстрого расчета остатков от деления используются таблицы
--размером [число оснований СОК x 512], где вторая размерность 512,
--так как результат сложения, после которого обычно нужно вычислить остаток,
--может превышать 255.
type T_RNS_table_9bit is array(1 to RNS_P_num) of T_uint_9bit_set;

--функция генерации и массив ПЗУ для хранения остатков от деления
--всех 9-битных чисел на все возможные основания СОК.
--первый индекс - номер основания,
--второй индекс - число для которого нужно найти остаток
function gen_RNS_rems_P return T_RNS_table_9bit;
constant RNS_rems_P: T_RNS_table_9bit := gen_RNS_rems_P;

--функция генерации и массив ПЗУ для хранения остатков от деления
--всех 9-битных чисел на значение функции Эйлера от оснований СОК.
--первый индекс - номер основания,
--второй индекс - число для которого нужно найти остаток
function gen_RNS_rems_phi return T_RNS_table_9bit;
constant RNS_rems_phi: T_RNS_table_9bit := gen_RNS_rems_phi;

--таблица значений степеней числа 2, в СОК.
type T_RNS_bin_pows_table is array(1 to RNS_P_num) of T_bin_data_width_set;
function gen_RNS_bin_pows return T_RNS_bin_pows_table;
constant RNS_bin_pows: T_RNS_bin_pows_table := gen_RNS_bin_pows;

--подпрограмма быстрого вычисления степени m числа n. Результат - остаток от деления
на q.
function GF_pow(n,m,q:natural) return natural;
--подпрограмм вычисления первообразного корня поля Галуа по модулю q.
function GF_primitive(q:natural) return natural;

--подпрограмма расчета и массив для хранения всех первообразных корней
--полей Галуа для всех 8-битных простых чисел.
function gen_primitives_8bit return T_RNS_vector_max;
--так как расчет идет медленно, то таблица заполнена заранее вычисленными числами
--однако, можно раскомментировать функцию gen_primitives_8bit
constant primitives_8bit: T_RNS_vector_max --:= gen_primitives_8bit;
 := ( 1, 2, 2, 3, 2, 2, 3, 2, 5, 2, 3, 2, 6, 3, 5, 2, 2, 2, 2,
      7, 5, 3, 2, 3, 5, 2, 5, 2, 6, 3, 3, 2, 3, 2, 2, 6, 5, 2,
      5, 2, 2, 2, 19, 5, 2, 3, 2, 3, 2, 6, 3, 7, 7, 6 );

--так как в проекте используется подмножество простых чисел-оснований СОК,
--то заполняется таблица RNS-primitives - реально используемые первообразные корни
function gen_RNS_primitives return T_RNS_vector;
constant RNS_primitives: T_RNS_vector := gen_RNS_primitives;
```

```
--тип массивов-просмотровых таблиц СОК
type T_RNS_table is array(1 to RNS_P_num) of T_uint_8bit_set;

--просмотровая таблица быстрого нахождения обратного индекса (дискретное
потенцирование)
--первый индекс - номер основания,
--второй индекс - индекс числа (дискретный логарифм) по которому нужно восстановить
число
function gen_RNS_inv_idx_table return T_RNS_table;
constant RNS_inv_idx_table: T_RNS_table := gen_RNS_inv_idx_table;

--просмотровая таблица быстрого нахождения индекса (дискретное логарифмирование)
--первый индекс - номер основания,
--второй индекс - число для которого нужно найти его индекс (дискретный логарифм)
function gen_RNS_idx_table return T_RNS_table;
constant RNS_idx_table: T_RNS_table := gen_RNS_idx_table;

--модулярный сумматор
--j - номер основания
--op1 - первое слагаемое
--op2 - второе слагаемое
function add_mod_8bit(j,op1,op2:uint_8bit) return uint_8bit;

--модулярный умножитель
--j - номер основания
--op1 - первый множитель
--op2 - второй множитель
function mul_mod_8bit(j,op1,op2:uint_8bit) return uint_8bit;

--расчет обратного по умножению элемента поля Галуа по модулю q
--работа основана на теории индексов
-- A^(-1) := inv_idx( q -idx(A) ); q=RNS_primes(j);
-- 0^(-1) :=0; (чтобы не глючило)
function inv_mod_8bit(j,A:uint_8bit) return uint_8bit;

--модулярный формальный делитель (корректно работает только при делении нацело)
--j - номер основания
--op1 - делимое
--op2 - делитель (если op2=0, то возвращается в ответе 0)
function fdiv_mod_8bit(j,op1,op2:uint_8bit) return uint_8bit;

--масштабирование на первое основание СОК
function scale_p1_8bit(A:T_RNS_vector) return T_RNS_vector;

--функция быстрого сложения содержимого массива чисел
--методом бинарного сдваивания (результат берется по модулю RNS_primes(j) )
function add_tree_method(j:uint_8bit; A: T_bin_data_width_set) return uint_8bit;

--функция быстрого перемножения содержимого массива чисел
--методом бинарного сдваиванияр (результат берется по модулю RNS_primes(j) )
function mul_tree_method(j:uint_8bit; A: T_bin_data_width_set) return uint_8bit;

--функция быстрого вычисления скалярного произведения содержимого двух массивов чисел
--методом бинарного сдваиванияр (результат берется по модулю RNS_primes(j) )
function scalar_tree_method(j:uint_8bit; op1,op2: T_bin_data_width_set) return
uint_8bit;

--расчет остатка от деления сверхдлинного двоичного числа на простое основание
--каждый бит переводимого числа умножается на соответствующую степень
--двойки, остаток от деления на простое число от которой заранее известен.
--найденные произведения складываются методом бинарного сдваивания
--j - номер основания из таблицы RNS_primes[]
--A - двоичное число
function calc_rem_P(j:uint_8bit; A: T_bin_data) return uint_8bit;

--перевод числа из двоичной системы счисления в СОК
function RNS_conv_PSS_RNS(A: T_bin_data) return T_RNS_vector;

--перевод числа из СОК в ОПСС
--A=(a1,a2,..,a(p_num)) = opss1+opss2*p1+opss3*p1*p2+...+opss(p_num)*p1*p2*..*p(p_num-
1)
```

```
function RNS_conv_RNS_OPSS(A: T_RNS_vector) return T_RNS_vector;

--перевод числа из ОПСС в СОК
function RNS_conv_OPSS_RNS(A: T_RNS_vector) return T_RNS_vector;

--перевод числа из ОПСС в двоичную систему счисления
function RNS_conv_OPSS_PSS(A: T_RNS_vector) return T_bin_data;

--перевод числа из СОК в двоичную систему счисления
function RNS_conv_RNS_PSS(A: T_RNS_vector) return T_bin_data;

--перевод числа из двоичной системы счисления в ОПСС
function RNS_conv_PSS_OPSS(A: T_bin_data) return T_RNS_vector;

--функция проверки чисел в СОК op1 и op2 на равенство
--result - логический результат (1 - равны, 0 не равны)
function RNS_is_equ(op1,op2:T_RNS_vector) return std_logic;

--функция проверки чисел в СОК op1 и op2 на "op1>op2"
--result - логический результат (1 - op1>op2, 0 иначе)
function RNS_cmp_g(op1,op2:T_RNS_vector) return std_logic;

--функция беззнакового сложения двоичного и 8-битного двоичного чисел
--(в проекте не используется, так как хорошо работает перегруженная "стандартная +")
--function bin_add_int8bit(A: T_bin_data; B:uint_8bit) return T_bin_data;

--функция беззнакового умножения двоичного и 8-битного двоичного чисел
--(перегруженная "стандартная *" глючит)
function bin_mul_uint8bit(A: T_bin_data; B:uint_8bit) return T_bin_data;

end;

-----------------------------------------------------------------
--реализации подпрограмм на языке VHDL
-----------------------------------------------------------------
package body RNS_defs_pkg is

--при отказе от unsigned в пользу std_logic vector
--subtype T_bin_data is std_logic_vector(bin_data_width-1 downto 0);
----сумматор двоичного числа и 8-битного двоичного числа
----(используется, например, при переводе чисел из ОПСС в ПСС)
--function bin_add_int8bit(A: T_bin_data; B:uint_8bit) return T_bin_data is
--variable res: T_bin_data;
--variable B_stdlgc: std_logic_vector(7 downto 0);
--variable i: natural;
--variable carry: std_logic;
--begin
--   res:=A; B_stdlgc:=conv_std_logic_vector(B,8); carry:='0';
--   for i in 0 to 7 loop
--      res(i) := (A(i) xor B_stdlgc(i)) xor carry;
--      carry:= (A(i) and B_stdlgc(i)) or ((A(i) or B_stdlgc(i)) and carry);
--   end loop;
--   for i in 8 to bin_data_width-1 loop
--      res(i) := A(i) xor carry;
--      carry := carry and A(i);
--   end loop;
--   return res;
--end;
--
----умножитель двоичного числа на 8-битное двоичное число
----(используется, например, при переводе чисел из ОПСС в ПСС)
function bin_mul_uint8bit(A: T_bin_data; B:uint_8bit) return T_bin_data is
variable res: T_bin_data;
variable B_stdlgc: unsigned(7 downto 0);
variable i: natural;
begin
   res:=conv_unsigned(0,bin_data_width);
   if B/=0 then
      B_stdlgc:=conv_unsigned(B,8);
      for i in bin_data_width-1 downto 0 loop
         res:=res+res;
```

```
         if A(i)='1' then
            res:=res+B_stdlgc;
         end if;
      end loop;
   end if;
   return res;
end;
--------------------------------------------------------------------------

--генерация всех 8-битных простых чисел от 2 до RNS_P_num_max-го
function gen_primes_8bit return T_RNS_vector_max is
variable i,j,k:natural;
variable is_prime:boolean;
variable p: T_RNS_vector_max;
begin
     p(1):=2;
     i:=2;
     for k in 1 to RNS_p_num_max loop
          is_prime:=false;
          while not(is_prime) loop
               i:=i+1; is_prime:=true;
               for j in 1 to k loop
                   if (i mod p(j))=0 then is_prime:=false; end if;
               end loop;
          end loop;
          if (i<=255)and(k<RNS_p_num_max) then p(k+1):=i; end if;
     end loop;
     return p;
end;

--заполнение массива RNS_primes простыми числами
--согласно индексов, хранимых в массиве RNS_primes_order
function gen_RNS_primes return T_RNS_vector is
variable i: natural;
variable tmp: T_RNS_vector;
begin
   for i in 1 to RNS_p_num loop
      tmp(i) := primes_8bit(RNS_primes_order(i));
   end loop;
   return tmp;
end;

--расчет содержимого массива RNS_rems_P[] - остатков от деления 9-битных чисел на
основания СОК
--первый индекс - номер основания
--второй индекс - число, для которого нужно найти остаток от деления
--(используется в модулярном сумматоре )
function gen_RNS_rems_P return T_RNS_table_9bit is
variable i,k:natural;
variable tmp: T_RNS_table_9bit;
begin
   for i in 1 to RNS_P_num loop
      tmp(i)(0):=0;
      for k in 1 to 511 loop
         tmp(i)(k):=k mod RNS_primes(i);
      end loop;
   end loop;
   return tmp;
end;

--расчет содержимого массива RNS_rems_phi[] - остатков от деления 9-битных чисел
--на функцию Эйлера от оснований СОК
--первый индекс - номер основания
--второй индекс - число, для которого нужно найти остаток от деления
--(используется в модулярном умножителе)
function gen_RNS_rems_phi return T_RNS_table_9bit is
variable i,k:natural;
variable tmp: T_RNS_table_9bit;
begin
   for i in 1 to RNS_P_num loop
      tmp(i)(0):=0;
```

```
      for k in 1 to 511 loop
         tmp(i)(k):=k mod (RNS_primes(i)-1);
      end loop;
   end loop;
   return tmp;
end;

--расчет значений степеней числа 2 в СОК
--(используется при переводе двоичных чисел в СОК)
function gen_RNS_bin_pows return T_RNS_bin_pows_table is
variable tmp_table: T_RNS_bin_pows_table;
variable i,k,new_pow: natural;
begin
   for i in 1 to RNS_P_num loop
      tmp_table(i)(0):=1;
      for k in 1 to bin_data_width-1 loop
         new_pow:=tmp_table(i)(k-1)*2;
         tmp_table(i)(k):=RNS_rems_P(i)(new_pow);
      end loop;
   end loop;
   return tmp_table;
end;

--быстрое модулярное возведение числа n в степень m
--результат берется по модулю q
function GF_pow(n,m,q:natural) return natural is
variable res,h,hm:natural;
begin
  res:=1; h:=n; hm:=m;
  while (hm>0) loop
     if (hm mod 2)=0 then h:=(h*h) mod q; hm:=hm/2;
                     else res:=(res*h) mod q; hm:=hm-1;
     end if;
  end loop;
  return res;
end;

--расчет значения первообразного корня поля Галуа по простому основанию q
function GF_primitive(q:natural) return natural is
variable i,j,flag:natural;
begin
   flag:=0;
   for i in 1 to q-1 loop
      for j in 1 to q-1 loop
         if GF_pow(i,j,q)=1 then flag:=flag+1; end if;
      end loop;
      if flag=1 then return i; else flag:=0; end if;
   end loop;
end;

--вычисление первообразных корней для всех 8-битных простых чисел
function gen_primitives_8bit return T_RNS_vector_max is
variable i:natural;
variable tmp: T_RNS_vector_max;
begin
   for i in 1 to RNS_p_num_max loop
      tmp(i) := GF_primitive(primes_8bit(i));
   end loop;
   return tmp;
end;

--заполнение массива RNS_primitives первообразными корнями
--согласно индексов, хранимых в массиве RNS_primes_order
function gen_RNS_primitives return T_RNS_vector is
variable i: natural;
variable tmp: T_RNS_vector;
begin
   for i in 1 to RNS_p_num loop
      tmp(i) := primitives_8bit(RNS_primes_order(i));
   end loop;
   return tmp;
```

```
end;

--расчет просмотровой таблицы дискретного потенцирования
--(по индексу восстанавливается число)
function gen_RNS_inv_idx_table return T_RNS_table is
variable tmp_inv: T_RNS_table;
variable i,k:natural;
begin
   for i in 1 to RNS_p_num loop
      for k in 0 to 255 loop
         tmp_inv(i)(k) := GF_pow(RNS_primitives(i),k,RNS_primes(i));
      end loop;
   end loop;
   return tmp_inv;
end;

--расчет просмотровой таблицы дискретного логарифимирования (индексы)
--(для заданного числа находится его индекс)
function gen_RNS_idx_table return T_RNS_table is
variable tmp_idx: T_RNS_table;
variable i,k:natural;
begin
   for i in 1 to RNS_p_num loop
      for k in 255 downto 0 loop
         tmp_idx(i)(RNS_inv_idx_table(i)(k)):=k;
      end loop;
   end loop;
   return tmp_idx;
end;

--модулярный сумматор
function add_mod_8bit(j,op1,op2:uint_8bit) return uint_8bit is
variable res_9bit: uint_9bit;
begin
   res_9bit := op1 + op2;
   return RNS_rems_P(j)(res_9bit);
end;

--модулярный умножитель
--работа основана на теории индексов
-- op1*op2 := inv_idx( idx(op1) + idx(op2) );
function mul_mod_8bit(j,op1,op2:uint_8bit) return uint_8bit is
variable op1_idx,op2_idx,sum_idx: uint_8bit;
variable res_9bit: uint_9bit;
begin
   if op1=0 then return 0;
   else if op2=0 then return 0;
   else
      op1_idx := RNS_idx_table(j)(op1);
      op2_idx := RNS_idx_table(j)(op2);
      res_9bit := op1_idx + op2_idx;
      sum_idx := RNS_rems_phi(j)(res_9bit);
      return RNS_inv_idx_table(j)(sum_idx);
   end if;
   end if;
end;

--расчет обратного по умножению элемента поля Галуа по модулю q
--работа основана на теории индексов
-- A^(-1) := inv_idx( phi(q) -idx(A) );
-- 0^(-1) :=0; (чтобы не глючило)
function inv_mod_8bit(j,A:uint_8bit) return uint_8bit is
variable A_idx, neg_A_idx: uint_8bit;
begin
   if A=0 then return 0;
         else
      A_idx := RNS_idx_table(j)(A);
      neg_A_idx := (RNS_primes(j)-1)-A_idx;
      return RNS_inv_idx_table(j)(neg_A_idx);
   end if;
end;
```

```
--модулярный формальный делитель (корректно работает только при делении нацело)
--j - номер основания
--op1 - делимое
--op2 - делитель (если op2=0, то возвращается в ответе 0)
function fdiv_mod_8bit(j,op1,op2:uint_8bit) return uint_8bit is
variable op2_inv: uint_8bit;
begin
   op2_inv:=inv_mod_8bit(j,op2);
   return mul_mod_8bit(j,op1,op2_inv);
end;

--масштабирование на первое основание СОК
function scale_p1_8bit(A:T_RNS_vector) return T_RNS_vector is
variable A_opss, tmp: T_RNS_vector;
begin
   A_opss:=RNS_conv_RNS_OPSS(A);
   for i in 1 to RNS_P_num -1 loop
      tmp(i):=A_opss(i+1);
   end loop;
   tmp(RNS_P_num):=0;
   return RNS_conv_OPSS_RNS(tmp);
end;

--функция быстрого сложения содержимого массива чисел методом бинарного сдваивания
--результат берется по модулю RNS_primes(j)
function add_tree_method(j:uint_8bit; A: T_bin_data_width_set) return uint_8bit is
variable tree_array: T_tree_array;
variable i: uint_8bit;
begin
   for i in 0 to bin_data_width-1 loop
      tree_array(bin_data_width+i):=A(i);
   end loop;
   for i in bin_data_width-1 downto 1 loop
      tree_array(i) := add_mod_8bit(j,tree_array(2*i), tree_array(2*i+1));
   end loop;
   return tree_array(1);
end;

--функция быстрого перемножения массива чисел методом бинарного сдваивания
--результат берется по модулю RNS_primes(j)
function mul_tree_method(j:uint_8bit; A: T_bin_data_width_set) return uint_8bit is
variable tree_array: T_tree_array;
variable i: uint_8bit;
begin
   for i in 0 to bin_data_width-1 loop
      tree_array(bin_data_width+i):=A(i);
   end loop;
   for i in bin_data_width-1 downto 1 loop
      tree_array(i) := mul_mod_8bit(j,tree_array(2*i), tree_array(2*i+1));
   end loop;
   return tree_array(1);
end;

--функция быстрого вычисления скалярного произведения содержимого двух массивов чисел
--методом бинарного сдваивания (результат берется по модулю RNS_primes(j) )
function scalar_tree_method(j:uint_8bit; op1,op2: T_bin_data_width_set) return
uint_8bit is
variable tree_array: T_tree_array;
variable i: uint_8bit;
begin
   for i in 0 to bin_data_width-1 loop
      tree_array(bin_data_width+i):=mul_mod_8bit(j,op1(i),op2(i));
   end loop;
   for i in bin_data_width-1 downto 1 loop
      tree_array(i) := add_mod_8bit(j,tree_array(2*i), tree_array(2*i+1));
   end loop;
   return tree_array(1);
end;

--расчет остатка от деления сверхдлинного двоичного числа на простое основание
```

```
--каждый бит переводимого числа умножается на соответствующую степень
--двойки, остаток от деления на простое число от которой заранее известен.
--найденные произведения складываются методом бинарного сдваивания
--j - номер основания из таблицы RNS_primes[]
--A - двоичное число
function calc_rem_P(j:uint_8bit; A:T_bin_data) return uint_8bit is
variable tmp: T_bin_data_width_set;
variable k: uint_8bit;
begin
   for k in 0 to bin_data_width-1 loop
      if A(k)='1' then tmp(k):=RNS_bin_pows(j)(k); else tmp(k):=0; end if;
   end loop;
   return add_tree_method(j,tmp);
end;

--перевод числа из двоичной системы счисления в СОК
-----------------------------------------------------------------------
function RNS_conv_PSS_RNS(A: T_bin_data) return T_RNS_vector is
variable result: T_RNS_vector;
variable i: uint_8bit;
begin
   for i in 1 to RNS_P_num loop
      result(i) := calc_rem_P(i,A);
   end loop;
   return result;
end;

--перевод числа из СОК в ОПСС
--A=(a1,a2,..,a(p_num)) = opss1+opss2*p1+opss3*p1*p2+...+opss(p_num)*p1*p2*..*p(p_num-
1)
function RNS_conv_RNS_OPSS(A: T_RNS_vector) return T_RNS_vector is
variable tmp_res: T_RNS_vector;
variable i,digit: uint_8bit;
variable tmp_add,tmp_neg,tmp_inv: uint_8bit;
begin
   for i in 1 to RNS_P_num loop
      digit := A(i);
      for j in 2 to i loop
         tmp_neg := RNS_primes(i) - RNS_rems_P(i)(tmp_res(j-1));
         tmp_add := add_mod_8bit(i,digit,tmp_neg);
         tmp_inv := inv_mod_8bit(i,RNS_primes(j-1));
         digit := mul_mod_8bit(i,tmp_add,tmp_inv);
      end loop;
      tmp_res(i) := digit;
   end loop;
   return tmp_res;
end;

--функция перевода числа из ОПСС в СОК
function RNS_conv_OPSS_RNS(A: T_RNS_vector) return T_RNS_vector is
variable i,j,tmp_res,tmp_rem,tmp_mul: uint_8bit;
variable result: T_RNS_vector;
begin
      for i in 1 to RNS_P_num loop
         tmp_res := 0;
         for j in RNS_P_num downto 1 loop
            tmp_rem := RNS_rems_P(i)(RNS_primes(j));
            tmp_mul := mul_mod_8bit(i,tmp_res,tmp_rem);
            tmp_res := add_mod_8bit(i,tmp_mul,A(j));
         end loop;
         result(i) := tmp_res;
      end loop;
      return result;
end;

--перевод числа из ОПСС в двоичную систему счисления
function RNS_conv_OPSS_PSS(A: T_RNS_vector) return T_bin_data is
variable tmp_res: T_bin_data;
begin
   tmp_res:=conv_unsigned(0,bin_data_width);
   for i in RNS_P_num downto 1 loop
```

```
      tmp_res := conv_unsigned(A(i),8) + bin_mul_uint8bit(tmp_res,RNS_primes(i));
   end loop;
   return tmp_res;
end;

--перевод числа из СОК в двоичную систему счисления
function RNS_conv_RNS_PSS(A: T_RNS_vector) return T_bin_data is
variable OPSS_res: T_RNS_vector;
begin
   OPSS_res := RNS_conv_RNS_OPSS(A);
   return RNS_conv_OPSS_PSS(OPSS_res);
end;

--перевод числа из двоичной системы счисления в ОПСС
function RNS_conv_PSS_OPSS(A: T_bin_data) return T_RNS_vector is
variable RNS_res: T_RNS_vector;
begin
   RNS_res := RNS_conv_PSS_RNS(A);
   return RNS_conv_RNS_OPSS(RNS_res);
end;

--функция проверки чисел в СОК op1 и op2 на равенство
--result - логический результат (1 - равны, 0 не равны)
function RNS_is_equ(op1,op2:T_RNS_vector) return std_logic is
variable flag:std_logic;
variable i:uint_8bit;
begin
   flag:='1';
   for i in 1 to RNS_P_num loop
      if op1(i) /= op2(i) then flag := '0'; end if;
   end loop;
   return flag;
end;

--функция проверки чисел в СОК op1 и op2 на "op1>op2"
--result - логический результат (1 - op1>op2, 0 иначе)
function RNS_cmp_g(op1,op2:T_RNS_vector) return std_logic is
variable flag1,flag2:std_logic;
variable op1_opss, op2_opss: T_RNS_vector;
begin
   op1_opss:=RNS_conv_RNS_OPSS(op1);
   op2_opss:=RNS_conv_RNS_OPSS(op2);
   flag1:='0'; flag2:='0';
   for i in RNS_P_num downto 1 loop
      if (flag2='0')and(op1_opss(i)>op2_opss(i)) then flag1:='1'; end if;
      if (flag1='0')and(op2_opss(i)>op1_opss(i)) then flag2:='1'; end if;
   end loop;
   return flag1;
end;

end;
```

ALU_RNS_mods.vhd – entity компонент работы с сигналами в СОК (операции сложения, умножения, смены знака, нахождения обратного числа, сравнения чисел в СОК)

```
----------------------------------------------------------------------------------
-- Company: SKFU, 4PMI
-- Engineer: prepod, Ionisyan A.S.
-- Project Name: LR3_var(000)
-- formula: c=(a+b)^3-7a+b
-- a,b,c - 32bit BSS numbers
-- RNS primes is (173,229,181,233,239)
----------------------------------------------------------------------------------
--Copyright 2015 Andrey S. Ionisyan
--Licensed under the Apache License, Version 2.0 (the "License");
--you may not use this file except in compliance with the License.
--You may obtain a copy of the License at
--    http://www.apache.org/licenses/LICENSE-2.0
--Unless required by applicable law or agreed to in writing, software
--distributed under the License is distributed on an "AS IS" BASIS,
```

```
--WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
--See the License for the specific language governing permissions and
--limitations under the License.
----------------------------------------------------------------------
--компонент нахождения обратного относительно сложения элемента
--A - число в СОК
--result - обратный относительно сложения элемент
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.all;
USE work.RNS_defs_pkg.all;

entity RNS_ALU_neg is
   Port (clock: std_logic; A: in T_RNS_vector; result: out T_RNS_vector);
end RNS_ALU_neg;

architecture Spartan3e500 of RNS_ALU_neg is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      for i in 1 to RNS_P_num loop
         if A(i)=0 then result(i)<=0;
                   else result(i)<=RNS_primes(i)-A(i);
         end if;
      end loop;
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

----------------------------------------------------------------------
--компонент нахождения обратного относительно умножения элемента
--A - число в СОК
--result - обратный относительно умножения элемент
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.all;
USE work.RNS_defs_pkg.all;

entity RNS_ALU_inv is
   Port (clock: std_logic; A: in T_RNS_vector; result: out T_RNS_vector);
end RNS_ALU_inv;

architecture Spartan3e500 of RNS_ALU_inv is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      for i in 1 to RNS_P_num loop
         result(i) <= inv_mod_8bit(i,A(i));
      end loop;
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

----------------------------------------------------------------------
--компонент сложения чисел в СОК
--op1 - первое слагаемое
--op2 - второе слагаемое
--result - сумма
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE work.RNS_defs_pkg.all;

entity RNS_ALU_add is
   Port(clock: in std_logic;
        op1, op2: in T_RNS_vector; result: out T_RNS_vector);
end RNS_ALU_add;
```

```
architecture Spartan3e500 of RNS_ALU_add is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      for i in 1 to RNS_P_num loop
         result(i) <= add_mod_8bit(i,op1(i),op2(i));
      end loop;
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

----------------------------------------------------------------------
--компонент перемножения чисел в СОК
--op1 - первый множитель
--op2 - второй множитель
--result - произведение
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
USE work.RNS_defs_pkg.all;
entity RNS_ALU_mul is
   Port (clock: in std_logic;
         op1, op2: in T_RNS_vector; result: out T_RNS_vector);
end RNS_ALU_mul;

architecture Spartan3e500 of RNS_ALU_mul is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      for i in 1 to RNS_P_num loop
         result(i) <= mul_mod_8bit(i,op1(i),op2(i));
      end loop;
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

----------------------------------------------------------------------
--компонент проверки чисел в СОК на равенство
--op1 - операнд слева
--op2 - операнд справа
--result - логический (1 - равны, 0 не равны) результат
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE work.RNS_defs_pkg.all;

entity RNS_ALU_cmp_equ is
   Port (clock: std_logic; op1, op2: in T_RNS_vector; result: out std_logic);
end RNS_ALU_cmp_equ;

architecture Spartan3e500 of RNS_ALU_cmp_equ is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      result <= RNS_is_equ(op1,op2);
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

----------------------------------------------------------------------
--компонент сравнения чисел в СОК
--числа переводятся в ОПСС и производится покомпонентное сравнение
```

```
--op1 - операнд слева
--op2 - операнд справа
--result - логический результат (1 - op1>op2, 0 иначе)
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE work.RNS_defs_pkg.all;

entity RNS_ALU_cmp_g is
   Port (clock: std_logic; op1, op2: in T_RNS_vector; result: out std_logic);
end RNS_ALU_cmp_g;

architecture Spartan3e500 of RNS_ALU_cmp_g is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      result<=RNS_cmp_g(op1,op2);
   end if;
   end process;
end Spartan3e500;
```

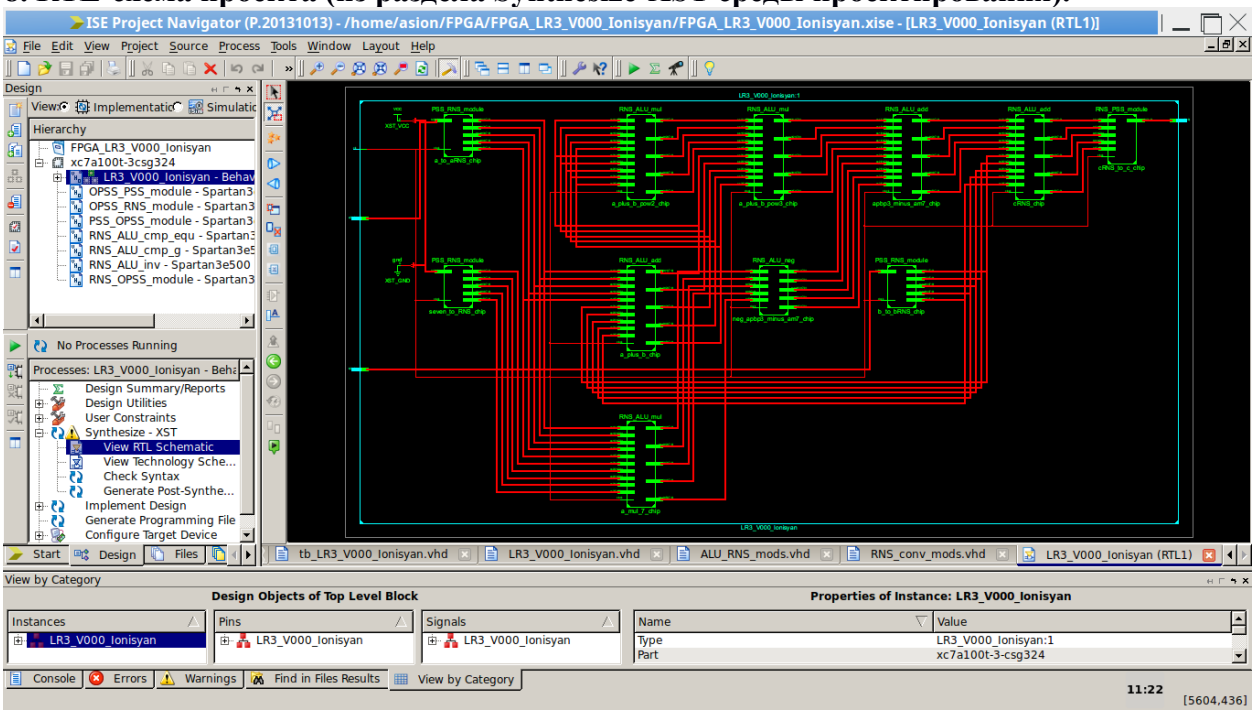
RNS_conv_mods.vhd – entity компонент работы с сигналами в СОК (операции перевода СОК<--->ОПСС<--->ПСС)

```
----------------------------------------------------------------------------------
-- Company: SKFU, 4PMI
-- Engineer: prepod, Ionisyan A.S.
-- Project Name: LR3_var(000)
-- formula: c=(a+b)^3-7a+b
-- a,b,c - 32bit BSS numbers
-- RNS primes is (173,229,181,233,239)
----------------------------------------------------------------------------------
--Copyright 2015 Andrey S. Ionisyan
--Licensed under the Apache License, Version 2.0 (the "License");
--you may not use this file except in compliance with the License.
--You may obtain a copy of the License at
--    http://www.apache.org/licenses/LICENSE-2.0
--Unless required by applicable law or agreed to in writing, software
--distributed under the License is distributed on an "AS IS" BASIS,
--WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
--See the License for the specific language governing permissions and
--limitations under the License.
----------------------------------------------------------------------
--компонент перевода числа из позиционной (двоичной) системы счисления
--в систему остаточных классов
----------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE work.RNS_defs_pkg.all;
entity PSS_RNS_module is
   Port (clock: std_logic; A: in T_bin_data; result: out T_RNS_vector);
end PSS_RNS_module;

architecture Spartan3e500 of PSS_RNS_module is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      result <= RNS_conv_PSS_RNS(A);
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

----------------------------------------------------------------------
--компонент перевода числа из СОК в обобщенную позиционную систему счисления
--A=(a1,a2,..,a(p_num)) = opss1+opss2*p1+opss3*p1*p2+...+opss(p_num)*p1*p2*..*p(p_num-
1)
----------------------------------------------------------------------
library IEEE;
```

```
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
USE work.RNS_defs_pkg.all;
entity RNS_OPSS_module is
   Port (clock: std_logic; A: in T_RNS_vector; result: out T_RNS_vector);
end RNS_OPSS_module;

architecture Spartan3e500 of RNS_OPSS_module is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      result <= RNS_conv_RNS_OPSS(A);
    end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
USE work.RNS_defs_pkg.all;
entity OPSS_RNS_module is
   Port (clock: std_logic; A: in T_RNS_vector; result: out T_RNS_vector);
end OPSS_RNS_module;

architecture Spartan3e500 of OPSS_RNS_module is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      result <= RNS_conv_OPSS_RNS(A);
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
USE work.RNS_defs_pkg.all;
entity OPSS_PSS_module is
   Port (clock: std_logic; A: in T_RNS_vector; result: out T_bin_data);
end OPSS_PSS_module;

architecture Spartan3e500 of OPSS_PSS_module is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      result <= RNS_conv_OPSS_PSS(A);
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
USE work.RNS_defs_pkg.all;
entity RNS_PSS_module is
   Port (clock: std_logic; A: in T_RNS_vector; result: out T_bin_data);
end RNS_PSS_module;

architecture Spartan3e500 of RNS_PSS_module is
begin
   process(clock)
```

```
   begin
   if (clock'event and clock = '1') then
      result <= RNS_conv_RNS_PSS(A);
   end if;
   end process;
end Spartan3e500;
----------------------------------------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE work.RNS_defs_pkg.all;
entity PSS_OPSS_module is
   Port (clock: std_logic; A: in T_bin_data; result: out T_RNS_vector);
end PSS_OPSS_module;

architecture Spartan3e500 of PSS_OPSS_module is
begin
   process(clock)
   begin
   if (clock'event and clock = '1') then
      result <= RNS_conv_PSS_OPSS(A);
   end if;
   end process;
end Spartan3e500;
```

8. RTL-схема проекта (из раздела Synthesize-XST среды проектирования).



9. Содержимое файла .syr отчета синтеза и имплементации проекта.

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs
```

```
-->
Reading design: LR3_V000_Ionisyan.prj

TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
  5) Advanced HDL Synthesis
       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "LR3_V000_Ionisyan.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "LR3_V000_Ionisyan"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : LR3_V000_Ionisyan
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
```

```
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Parsing VHDL file "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/RNS_defs_pkg.vhd" into
library work
Parsing package <RNS_defs_pkg>.
Parsing package body <RNS_defs_pkg>.
WARNING:HDLCompiler:443 - "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/RNS_defs_pkg.vhd"
Line 380: Function gf_primitive does not always return a value.
Parsing VHDL file "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/RNS_conv_mods.vhd" into
library work
Parsing entity <PSS_RNS_module>.
Parsing architecture <Spartan3e500> of entity <pss_rns_module>.
Parsing entity <RNS_OPSS_module>.
Parsing architecture <Spartan3e500> of entity <rns_opss_module>.
Parsing entity <OPSS_RNS_module>.
Parsing architecture <Spartan3e500> of entity <opss_rns_module>.
Parsing entity <OPSS_PSS_module>.
Parsing architecture <Spartan3e500> of entity <opss_pss_module>.
Parsing entity <RNS_PSS_module>.
Parsing architecture <Spartan3e500> of entity <rns_pss_module>.
Parsing entity <PSS_OPSS_module>.
Parsing architecture <Spartan3e500> of entity <pss_opss_module>.
Parsing VHDL file "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/ALU_RNS_mods.vhd" into
library work
Parsing entity <RNS_ALU_neg>.
Parsing architecture <Spartan3e500> of entity <rns_alu_neg>.
Parsing entity <RNS_ALU_inv>.
Parsing architecture <Spartan3e500> of entity <rns_alu_inv>.
Parsing entity <RNS_ALU_add>.
Parsing architecture <Spartan3e500> of entity <rns_alu_add>.
Parsing entity <RNS_ALU_mul>.
Parsing architecture <Spartan3e500> of entity <rns_alu_mul>.
Parsing entity <RNS_ALU_cmp_equ>.
Parsing architecture <Spartan3e500> of entity <rns_alu_cmp_equ>.
Parsing entity <RNS_ALU_cmp_g>.
Parsing architecture <Spartan3e500> of entity <rns_alu_cmp_g>.
Parsing VHDL file "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/LR3_V000_Ionisyan.vhd" into
library work
Parsing entity <LR3_V000_Ionisyan>.
Parsing architecture <Behavioral> of entity <lr3_v000_ionisyan>.

=========================================================================
*                           HDL Elaboration                             *
=========================================================================

Elaborating entity <LR3_V000_Ionisyan> (architecture <Behavioral>) from library
<work>.

Elaborating entity <PSS_RNS_module> (architecture <Spartan3e500>) from library <work>.
```

```
Elaborating entity <RNS_ALU_add> (architecture <Spartan3e500>) from library <work>.

Elaborating entity <RNS_ALU_mul> (architecture <Spartan3e500>) from library <work>.

Elaborating entity <RNS_ALU_neg> (architecture <Spartan3e500>) from library <work>.

Elaborating entity <RNS_PSS_module> (architecture <Spartan3e500>) from library <work>.
WARNING:HDLCompiler:746 - "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/RNS_defs_pkg.vhd"
Line 590: Range is empty (null range)

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <LR3_V000_Ionisyan>.
    Related source file is
"/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/LR3_V000_Ionisyan.vhd".
    Summary:
      no macro.
Unit <LR3_V000_Ionisyan> synthesized.

Synthesizing Unit <PSS_RNS_module>.
    Related source file is
"/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/RNS_conv_mods.vhd".
    Found 8-bit register for signal <result<2>>.
    Found 8-bit register for signal <result<3>>.
    Found 8-bit register for signal <result<4>>.
    Found 8-bit register for signal <result<5>>.
    Found 8-bit register for signal <result<1>>.
    Found 7-bit adder for signal <n0886> created at line 447.
    Found 5-bit adder for signal <n0889> created at line 447.
    Found 8-bit adder for signal <n0892> created at line 447.
    Found 7-bit adder for signal <n0895> created at line 447.
    Found 8-bit adder for signal <n0898> created at line 447.
    Found 7-bit adder for signal <n0901> created at line 447.
    Found 8-bit adder for signal <n0904> created at line 447.
    Found 9-bit adder for signal <n0907> created at line 447.
    Found 8-bit adder for signal <n0910> created at line 447.
    Found 8-bit adder for signal <n0913> created at line 447.
    Found 9-bit adder for signal <n0916> created at line 447.
    Found 9-bit adder for signal <n0919> created at line 447.
    Found 9-bit adder for signal <n0922> created at line 447.
    Found 7-bit adder for signal <n0925> created at line 447.
    Found 5-bit adder for signal <n0928> created at line 447.
    Found 3-bit adder for signal <n0931> created at line 447.
    Found 8-bit adder for signal <n0934> created at line 447.
    Found 9-bit adder for signal <n0937> created at line 447.
    Found 9-bit adder for signal <n0940> created at line 447.
    Found 9-bit adder for signal <n0943> created at line 447.
    Found 9-bit adder for signal <n0946> created at line 447.
    Found 9-bit adder for signal <n0949> created at line 447.
    Found 9-bit adder for signal <n0952> created at line 447.
    Found 6-bit adder for signal <n0955> created at line 447.
    Found 9-bit adder for signal <n0958> created at line 447.
    Found 9-bit adder for signal <n0961> created at line 447.
    Found 9-bit adder for signal <n0964> created at line 447.
    Found 9-bit adder for signal <n0967> created at line 447.
    Found 9-bit adder for signal <n0970> created at line 447.
    Found 9-bit adder for signal <n0973> created at line 447.
    Found 9-bit adder for signal <n0976> created at line 447.
    Found 9-bit adder for signal <n0979> created at line 447.
    Found 8-bit adder for signal <n0982> created at line 447.
    Found 9-bit adder for signal <n0985> created at line 447.
    Found 9-bit adder for signal <n0988> created at line 447.
    Found 9-bit adder for signal <n0991> created at line 447.
    Found 9-bit adder for signal <n0994> created at line 447.
    Found 9-bit adder for signal <n0997> created at line 447.
    Found 8-bit adder for signal <n1000> created at line 447.
    Found 8-bit adder for signal <n1003> created at line 447.
    Found 9-bit adder for signal <n1006> created at line 447.
    Found 9-bit adder for signal <n1009> created at line 447.
```

```
Found 7-bit adder for signal <n1012> created at line 447.
Found 9-bit adder for signal <n1015> created at line 447.
Found 9-bit adder for signal <n1018> created at line 447.
Found 9-bit adder for signal <n1021> created at line 447.
Found 9-bit adder for signal <n1024> created at line 447.
Found 9-bit adder for signal <n1027> created at line 447.
Found 9-bit adder for signal <n1030> created at line 447.
Found 9-bit adder for signal <n1033> created at line 447.
Found 9-bit adder for signal <n1036> created at line 447.
Found 9-bit adder for signal <n1039> created at line 447.
Found 9-bit adder for signal <n1042> created at line 447.
Found 9-bit adder for signal <n1045> created at line 447.
Found 9-bit adder for signal <n1048> created at line 447.
Found 9-bit adder for signal <n1051> created at line 447.
Found 9-bit adder for signal <n1054> created at line 447.
Found 8-bit adder for signal <n1057> created at line 447.
Found 9-bit adder for signal <n1060> created at line 447.
Found 8-bit adder for signal <n1063> created at line 447.
Found 9-bit adder for signal <n1066> created at line 447.
Found 9-bit adder for signal <n1069> created at line 447.
Found 8-bit adder for signal <n1072> created at line 447.
Found 8-bit adder for signal <n1075> created at line 447.
Found 6-bit adder for signal <n1078> created at line 447.
Found 8-bit adder for signal <n1081> created at line 447.
Found 8-bit adder for signal <n1084> created at line 447.
Found 8-bit adder for signal <n1087> created at line 447.
Found 9-bit adder for signal <n1090> created at line 447.
Found 9-bit adder for signal <n1093> created at line 447.
Found 9-bit adder for signal <n1096> created at line 447.
Found 9-bit adder for signal <n1099> created at line 447.
Found 9-bit adder for signal <n1102> created at line 447.
Found 9-bit adder for signal <n1105> created at line 447.
Found 9-bit adder for signal <n1108> created at line 447.
Found 9-bit adder for signal <n1111> created at line 447.
Found 9-bit adder for signal <n1114> created at line 447.
Found 9-bit adder for signal <n1117> created at line 447.
Found 9-bit adder for signal <n1120> created at line 447.
Found 9-bit adder for signal <n1123> created at line 447.
Found 9-bit adder for signal <n1126> created at line 447.
Found 9-bit adder for signal <n1129> created at line 447.
Found 9-bit adder for signal <n1132> created at line 447.
Found 4-bit adder for signal <n1135> created at line 447.
Found 8-bit adder for signal <n1138> created at line 447.
Found 9-bit adder for signal <n1141> created at line 447.
Found 8-bit adder for signal <n1144> created at line 447.
Found 9-bit adder for signal <n1147> created at line 447.
Found 9-bit adder for signal <n1150> created at line 447.
Found 7-bit adder for signal <n1153> created at line 447.
Found 8-bit adder for signal <n1156> created at line 447.
Found 9-bit adder for signal <n1159> created at line 447.
Found 9-bit adder for signal <n1162> created at line 447.
Found 9-bit adder for signal <n1165> created at line 447.
Found 7-bit adder for signal <n1168> created at line 447.
Found 9-bit adder for signal <n1171> created at line 447.
Found 9-bit adder for signal <n1174> created at line 447.
Found 9-bit adder for signal <n1177> created at line 447.
Found 9-bit adder for signal <n1180> created at line 447.
Found 9-bit adder for signal <n1183> created at line 447.
Found 9-bit adder for signal <n1186> created at line 447.
Found 9-bit adder for signal <n1189> created at line 447.
Found 9-bit adder for signal <n1192> created at line 447.
Found 9-bit adder for signal <n1195> created at line 447.
Found 9-bit adder for signal <n1198> created at line 447.
Found 9-bit adder for signal <n1201> created at line 447.
Found 9-bit adder for signal <n1204> created at line 447.
Found 9-bit adder for signal <n1207> created at line 447.
Found 9-bit adder for signal <n1210> created at line 447.
Found 9-bit adder for signal <n1213> created at line 447.
Found 9-bit adder for signal <n1216> created at line 447.
Found 8-bit adder for signal <n1219> created at line 447.
Found 9-bit adder for signal <n1222> created at line 447.
```

```
Found 9-bit adder for signal <n1225> created at line 447.
Found 9-bit adder for signal <n1228> created at line 447.
Found 9-bit adder for signal <n1231> created at line 447.
Found 8-bit adder for signal <n1234> created at line 447.
Found 9-bit adder for signal <n1237> created at line 447.
Found 8-bit adder for signal <n1240> created at line 447.
Found 9-bit adder for signal <n1243> created at line 447.
Found 7-bit adder for signal <n1246> created at line 447.
Found 9-bit adder for signal <n1249> created at line 447.
Found 9-bit adder for signal <n1252> created at line 447.
Found 9-bit adder for signal <n1255> created at line 447.
Found 9-bit adder for signal <n1258> created at line 447.
Found 9-bit adder for signal <n1261> created at line 447.
Found 9-bit adder for signal <n1264> created at line 447.
Found 9-bit adder for signal <n1267> created at line 447.
Found 9-bit adder for signal <n1270> created at line 447.
Found 9-bit adder for signal <n1273> created at line 447.
Found 9-bit adder for signal <n1276> created at line 447.
Found 9-bit adder for signal <n1279> created at line 447.
Found 9-bit adder for signal <n1282> created at line 447.
Found 9-bit adder for signal <n1285> created at line 447.
Found 9-bit adder for signal <n1288> created at line 447.
Found 128x7-bit Read Only RAM for signal <BUS_0001_PWR_7_o_wide_mux_32_OUT>
Found 32x5-bit Read Only RAM for signal <BUS_0002_PWR_7_o_wide_mux_34_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0003_GND_7_o_wide_mux_36_OUT>
Found 128x7-bit Read Only RAM for signal <BUS_0004_PWR_7_o_wide_mux_38_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0005_GND_7_o_wide_mux_40_OUT>
Found 128x7-bit Read Only RAM for signal <BUS_0006_PWR_7_o_wide_mux_42_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0007_GND_7_o_wide_mux_44_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0008_PWR_7_o_wide_mux_46_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0009_GND_7_o_wide_mux_48_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0010_GND_7_o_wide_mux_50_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0011_PWR_7_o_wide_mux_52_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0012_PWR_7_o_wide_mux_54_OUT>
Found 128x7-bit Read Only RAM for signal <BUS_0014_PWR_7_o_wide_mux_58_OUT>
Found 32x5-bit Read Only RAM for signal <BUS_0015_PWR_7_o_wide_mux_60_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0017_GND_7_o_wide_mux_64_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0018_PWR_7_o_wide_mux_66_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0019_PWR_7_o_wide_mux_68_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0020_PWR_7_o_wide_mux_70_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0021_PWR_7_o_wide_mux_72_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0022_PWR_7_o_wide_mux_74_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0023_PWR_7_o_wide_mux_76_OUT>
Found 64x6-bit Read Only RAM for signal <BUS_0024_PWR_7_o_wide_mux_78_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0025_PWR_7_o_wide_mux_80_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0026_PWR_7_o_wide_mux_82_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0027_PWR_7_o_wide_mux_84_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0028_PWR_7_o_wide_mux_86_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0029_PWR_7_o_wide_mux_88_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0030_PWR_7_o_wide_mux_90_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0031_PWR_7_o_wide_mux_92_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0032_GND_7_o_wide_mux_125_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0033_GND_7_o_wide_mux_127_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0034_GND_7_o_wide_mux_129_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0035_GND_7_o_wide_mux_131_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0036_GND_7_o_wide_mux_133_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0037_GND_7_o_wide_mux_135_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0038_GND_7_o_wide_mux_137_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0039_GND_7_o_wide_mux_139_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0040_GND_7_o_wide_mux_141_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0041_GND_7_o_wide_mux_143_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0042_GND_7_o_wide_mux_145_OUT>
Found 128x7-bit Read Only RAM for signal <BUS_0043_PWR_7_o_wide_mux_147_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0048_GND_7_o_wide_mux_157_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0049_GND_7_o_wide_mux_159_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0050_GND_7_o_wide_mux_161_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0051_GND_7_o_wide_mux_163_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0052_GND_7_o_wide_mux_165_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0053_GND_7_o_wide_mux_167_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0054_GND_7_o_wide_mux_169_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0056_GND_7_o_wide_mux_173_OUT>
```

```
Found 512x8-bit Read Only RAM for signal <BUS_0057_GND_7_o_wide_mux_175_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0058_GND_7_o_wide_mux_177_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0059_GND_7_o_wide_mux_179_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0060_GND_7_o_wide_mux_181_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0061_GND_7_o_wide_mux_183_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0062_GND_7_o_wide_mux_185_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0063_GND_7_o_wide_mux_218_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0064_PWR_7_o_wide_mux_220_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0065_GND_7_o_wide_mux_222_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0066_PWR_7_o_wide_mux_224_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0067_PWR_7_o_wide_mux_226_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0068_GND_7_o_wide_mux_228_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0069_GND_7_o_wide_mux_230_OUT>
Found 64x6-bit Read Only RAM for signal <BUS_0070_PWR_7_o_wide_mux_232_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0071_GND_7_o_wide_mux_234_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0072_GND_7_o_wide_mux_236_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0073_GND_7_o_wide_mux_238_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0074_PWR_7_o_wide_mux_240_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0079_PWR_7_o_wide_mux_250_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0080_PWR_7_o_wide_mux_252_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0081_PWR_7_o_wide_mux_254_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0082_PWR_7_o_wide_mux_256_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0083_PWR_7_o_wide_mux_258_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0084_PWR_7_o_wide_mux_260_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0085_PWR_7_o_wide_mux_262_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0087_PWR_7_o_wide_mux_266_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0088_PWR_7_o_wide_mux_268_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0089_PWR_7_o_wide_mux_270_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0090_PWR_7_o_wide_mux_272_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0091_PWR_7_o_wide_mux_274_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0092_PWR_7_o_wide_mux_276_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0093_PWR_7_o_wide_mux_278_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0095_GND_7_o_wide_mux_312_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0096_GND_7_o_wide_mux_314_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0097_GND_7_o_wide_mux_316_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0098_GND_7_o_wide_mux_318_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0099_GND_7_o_wide_mux_320_OUT>
Found 128x7-bit Read Only RAM for signal <BUS_0100_PWR_7_o_wide_mux_322_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0101_GND_7_o_wide_mux_324_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0102_GND_7_o_wide_mux_326_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0103_GND_7_o_wide_mux_328_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0104_GND_7_o_wide_mux_330_OUT>
Found 128x7-bit Read Only RAM for signal <BUS_0105_PWR_7_o_wide_mux_332_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0110_GND_7_o_wide_mux_342_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0111_GND_7_o_wide_mux_344_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0112_GND_7_o_wide_mux_346_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0113_GND_7_o_wide_mux_348_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0114_GND_7_o_wide_mux_350_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0115_GND_7_o_wide_mux_352_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0116_GND_7_o_wide_mux_354_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0118_GND_7_o_wide_mux_358_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0119_GND_7_o_wide_mux_360_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0120_GND_7_o_wide_mux_362_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0121_GND_7_o_wide_mux_364_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0122_GND_7_o_wide_mux_366_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0123_GND_7_o_wide_mux_368_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0124_GND_7_o_wide_mux_370_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0125_GND_7_o_wide_mux_403_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0126_GND_7_o_wide_mux_405_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0127_GND_7_o_wide_mux_407_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0128_GND_7_o_wide_mux_409_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0129_GND_7_o_wide_mux_411_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0130_GND_7_o_wide_mux_413_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0131_GND_7_o_wide_mux_415_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0132_GND_7_o_wide_mux_417_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0133_GND_7_o_wide_mux_419_OUT>
Found 256x8-bit Read Only RAM for signal <BUS_0134_GND_7_o_wide_mux_421_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0135_GND_7_o_wide_mux_423_OUT>
Found 128x7-bit Read Only RAM for signal <BUS_0136_PWR_7_o_wide_mux_425_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0141_GND_7_o_wide_mux_435_OUT>
Found 512x8-bit Read Only RAM for signal <BUS_0142_GND_7_o_wide_mux_437_OUT>
```

```
    Found 512x8-bit Read Only RAM for signal <BUS_0143_GND_7_o_wide_mux_439_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0144_GND_7_o_wide_mux_441_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0145_GND_7_o_wide_mux_443_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0146_GND_7_o_wide_mux_445_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0147_GND_7_o_wide_mux_447_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0149_GND_7_o_wide_mux_451_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0150_GND_7_o_wide_mux_453_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0151_GND_7_o_wide_mux_455_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0152_GND_7_o_wide_mux_457_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0153_GND_7_o_wide_mux_459_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0154_GND_7_o_wide_mux_461_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0155_GND_7_o_wide_mux_463_OUT>
    Found 512x40-bit Read Only RAM for signal <_n1801>
    Summary:
      inferred 133 RAM(s).
      inferred 135 Adder/Subtractor(s).
      inferred  40 D-type flip-flop(s).
Unit <PSS_RNS_module> synthesized.

Synthesizing Unit <RNS_ALU_add>.
    Related source file is "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/ALU_RNS_mods.vhd".
    Found 8-bit register for signal <result<2>>.
    Found 8-bit register for signal <result<3>>.
    Found 8-bit register for signal <result<4>>.
    Found 8-bit register for signal <result<5>>.
    Found 8-bit register for signal <result<1>>.
    Found 9-bit adder for signal <n0042> created at line 447.
    Found 9-bit adder for signal <n0045> created at line 447.
    Found 9-bit adder for signal <n0048> created at line 447.
    Found 9-bit adder for signal <n0051> created at line 447.
    Found 9-bit adder for signal <n0054> created at line 447.
    Found 512x8-bit Read Only RAM for signal <BUS_0001_PWR_8_o_wide_mux_1_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0002_GND_8_o_wide_mux_3_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0003_PWR_8_o_wide_mux_5_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0004_GND_8_o_wide_mux_7_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0005_GND_8_o_wide_mux_9_OUT>
    Summary:
      inferred   5 RAM(s).
      inferred   5 Adder/Subtractor(s).
      inferred  40 D-type flip-flop(s).
Unit <RNS_ALU_add> synthesized.

Synthesizing Unit <RNS_ALU_mul>.
    Related source file is "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/ALU_RNS_mods.vhd".
    Found 8-bit register for signal <result<2>>.
    Found 8-bit register for signal <result<3>>.
    Found 8-bit register for signal <result<4>>.
    Found 8-bit register for signal <result<5>>.
    Found 8-bit register for signal <result<1>>.
    Found 9-bit adder for signal <n0102> created at line 463.
    Found 9-bit adder for signal <n0105> created at line 463.
    Found 9-bit adder for signal <n0108> created at line 463.
    Found 9-bit adder for signal <n0111> created at line 463.
    Found 9-bit adder for signal <n0114> created at line 463.
    Found 256x8-bit Read Only RAM for signal <op1[1][7]_GND_9_o_wide_mux_2_OUT>
    Found 256x8-bit Read Only RAM for signal <op2[1][7]_GND_9_o_wide_mux_3_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0001_GND_9_o_wide_mux_6_OUT>
    Found 256x8-bit Read Only RAM for signal <op1[2][7]_GND_9_o_wide_mux_19_OUT>
    Found 256x8-bit Read Only RAM for signal <op2[2][7]_GND_9_o_wide_mux_20_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0002_GND_9_o_wide_mux_23_OUT>
    Found 256x8-bit Read Only RAM for signal <op1[3][7]_GND_9_o_wide_mux_36_OUT>
    Found 256x8-bit Read Only RAM for signal <op2[3][7]_GND_9_o_wide_mux_37_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0003_PWR_9_o_wide_mux_40_OUT>
    Found 256x8-bit Read Only RAM for signal <op1[4][7]_GND_9_o_wide_mux_53_OUT>
    Found 256x8-bit Read Only RAM for signal <op2[4][7]_GND_9_o_wide_mux_54_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0004_PWR_9_o_wide_mux_57_OUT>
    Found 256x8-bit Read Only RAM for signal <op1[5][7]_GND_9_o_wide_mux_70_OUT>
    Found 256x8-bit Read Only RAM for signal <op2[5][7]_GND_9_o_wide_mux_71_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0005_PWR_9_o_wide_mux_74_OUT>
    Found 512x8-bit Read Only RAM for signal <_n0667>
    Found 512x8-bit Read Only RAM for signal <_n1180>
```

```
    Found 512x8-bit Read Only RAM for signal <_n1693>
    Found 512x8-bit Read Only RAM for signal <_n2206>
    Found 512x8-bit Read Only RAM for signal <_n2719>
    Summary:
      inferred  20 RAM(s).
      inferred   5 Adder/Subtractor(s).
      inferred  40 D-type flip-flop(s).
Unit <RNS_ALU_mul> synthesized.

Synthesizing Unit <RNS_ALU_neg>.
    Related source file is "/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/ALU_RNS_mods.vhd".
    Found 8-bit register for signal <result<2>>.
    Found 8-bit register for signal <result<3>>.
    Found 8-bit register for signal <result<4>>.
    Found 8-bit register for signal <result<5>>.
    Found 8-bit register for signal <result<1>>.
    Found 8-bit subtractor for signal <GND_10_o_GND_10_o_sub_2_OUT<7:0>> created at
line 39.
    Found 8-bit subtractor for signal <GND_10_o_GND_10_o_sub_5_OUT<7:0>> created at
line 39.
    Found 8-bit subtractor for signal <GND_10_o_GND_10_o_sub_8_OUT<7:0>> created at
line 39.
    Found 8-bit subtractor for signal <GND_10_o_GND_10_o_sub_11_OUT<7:0>> created at
line 39.
    Found 8-bit subtractor for signal <GND_10_o_GND_10_o_sub_14_OUT<7:0>> created at
line 39.
    Summary:
      inferred   5 Adder/Subtractor(s).
      inferred  40 D-type flip-flop(s).
Unit <RNS_ALU_neg> synthesized.

Synthesizing Unit <RNS_PSS_module>.
    Related source file is
"/home/asion/FPGA/FPGA_LR3_V000_Ionisyan/RNS_conv_mods.vhd".
    Found 32-bit register for signal <result>.
    Found 9-bit adder for signal <n0976> created at line 447.
    Found 9-bit adder for signal <n0978> created at line 463.
    Found 9-bit adder for signal <n0981> created at line 447.
    Found 9-bit adder for signal <n0983> created at line 463.
    Found 9-bit adder for signal <n0986> created at line 447.
    Found 9-bit adder for signal <n0990> created at line 447.
    Found 9-bit adder for signal <n0992> created at line 463.
    Found 9-bit adder for signal <n0995> created at line 447.
    Found 9-bit adder for signal <n0997> created at line 463.
    Found 9-bit adder for signal <n1000> created at line 447.
    Found 9-bit adder for signal <n1002> created at line 463.
    Found 9-bit adder for signal <n1005> created at line 447.
    Found 9-bit adder for signal <n1007> created at line 463.
    Found 9-bit adder for signal <n1010> created at line 447.
    Found 9-bit adder for signal <n1012> created at line 463.
    Found 9-bit adder for signal <n1015> created at line 447.
    Found 9-bit adder for signal <n1017> created at line 463.
    Found 9-bit adder for signal <n1020> created at line 447.
    Found 9-bit adder for signal <n1022> created at line 463.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_214_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_217_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_220_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_223_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_226_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_229_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_232_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_234_OUT> created at line 624.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_237_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_240_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_243_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_246_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_249_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_252_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_255_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_258_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_261_OUT> created at line 273.
```

```
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_264_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_267_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_270_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_273_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_276_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_279_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_282_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_285_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_288_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_291_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_294_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_297_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_300_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_303_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_306_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_309_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_312_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_315_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_318_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_321_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_324_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_327_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_329_OUT> created at line 624.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_332_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_335_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_338_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_341_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_344_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_347_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_350_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_353_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_356_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_359_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_362_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_365_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_368_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_371_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_374_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_377_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_380_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_383_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_386_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_389_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_392_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_395_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_398_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_401_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_404_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_407_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_410_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_413_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_416_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_419_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_422_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_424_OUT> created at line 624.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_427_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_430_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_433_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_436_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_439_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_442_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_445_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_448_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_451_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_454_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_457_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_460_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_463_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_466_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_469_OUT> created at line 273.
Found 32-bit adder for signal <GND_11_o_GND_11_o_add_472_OUT> created at line 273.
```

```
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_475_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_478_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_481_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_484_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_487_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_490_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_493_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_496_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_499_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_502_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_505_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_508_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_511_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_514_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_517_OUT> created at line 273.
    Found 32-bit adder for signal <GND_11_o_GND_11_o_add_519_OUT> created at line 624.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_2_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_16_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_30_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_43_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_57_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_71_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_85_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_99_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_113_OUT<7:0>> created at
line 591.
    Found 8-bit subtractor for signal <GND_11_o_GND_11_o_sub_127_OUT<7:0>> created at
line 591.
    Found 512x8-bit Read Only RAM for signal <BUS_0001_GND_11_o_wide_mux_3_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0001_GND_11_o_wide_mux_5_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0002_GND_11_o_wide_mux_8_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0003_PWR_12_o_wide_mux_17_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0003_GND_11_o_wide_mux_19_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0004_PWR_12_o_wide_mux_22_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0005_PWR_12_o_wide_mux_31_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0006_PWR_12_o_wide_mux_36_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0007_GND_11_o_wide_mux_44_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0007_GND_11_o_wide_mux_46_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0008_PWR_12_o_wide_mux_49_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0009_GND_11_o_wide_mux_58_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0009_GND_11_o_wide_mux_60_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0010_PWR_12_o_wide_mux_63_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0011_GND_11_o_wide_mux_72_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0011_GND_11_o_wide_mux_74_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0012_PWR_12_o_wide_mux_77_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0013_GND_11_o_wide_mux_86_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0013_GND_11_o_wide_mux_88_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0014_PWR_12_o_wide_mux_91_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0015_GND_11_o_wide_mux_100_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0015_GND_11_o_wide_mux_102_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0016_PWR_12_o_wide_mux_105_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0017_GND_11_o_wide_mux_114_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0017_GND_11_o_wide_mux_116_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0018_PWR_12_o_wide_mux_119_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0012_GND_11_o_wide_mux_125_OUT>
    Found 512x8-bit Read Only RAM for signal <BUS_0019_GND_11_o_wide_mux_128_OUT>
    Found 256x8-bit Read Only RAM for signal <BUS_0019_GND_11_o_wide_mux_130_OUT>
    Found 256x32-bit Read Only RAM for signal <_n2126>
    Found 512x8-bit Read Only RAM for signal <_n2639>
    Found 512x8-bit Read Only RAM for signal <_n3152>
    Found 512x8-bit Read Only RAM for signal <_n3665>
    Found 512x8-bit Read Only RAM for signal <_n4178>
    Found 256x24-bit Read Only RAM for signal <_n4435>
```

```
    Found 256x8-bit Read Only RAM for signal <_n4692>
    Found 512x8-bit Read Only RAM for signal <_n5205>
    Found 512x8-bit Read Only RAM for signal <_n5718>
    Found 512x8-bit Read Only RAM for signal <_n6231>
    Found 256x16-bit Read Only RAM for signal <_n6488>
    Found 512x8-bit Read Only RAM for signal <_n7001>
    Found 512x8-bit Read Only RAM for signal <_n7514>
    Found 512x8-bit Read Only RAM for signal <_n8027>
    Found 256x8-bit Read Only RAM for signal <_n8284>
    Summary:
      inferred  44 RAM(s).
      inferred 133 Adder/Subtractor(s).
      inferred  32 D-type flip-flop(s).
      inferred 117 Multiplexer(s).
Unit <RNS_PSS_module> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 518
 128x7-bit single-port Read Only RAM                   : 24
 256x16-bit single-port Read Only RAM                  : 1
 256x24-bit single-port Read Only RAM                  : 1
 256x32-bit single-port Read Only RAM                  : 1
 256x8-bit single-port Read Only RAM                   : 132
 32x5-bit single-port Read Only RAM                    : 6
 512x40-bit single-port Read Only RAM                  : 3
 512x8-bit single-port Read Only RAM                   : 344
 64x6-bit single-port Read Only RAM                    : 6
# Adders/Subtractors                                   : 573
 3-bit adder                                           : 3
 32-bit adder                                          : 104
 4-bit adder                                           : 3
 5-bit adder                                           : 6
 6-bit adder                                           : 6
 7-bit adder                                           : 24
 8-bit adder                                           : 66
 8-bit subtractor                                      : 15
 9-bit adder                                           : 346
# Registers                                            : 51
 32-bit register                                       : 1
 8-bit register                                        : 50
# Multiplexers                                         : 117
 1-bit 2-to-1 multiplexer                              : 8
 32-bit 2-to-1 multiplexer                             : 100
 8-bit 2-to-1 multiplexer                              : 9

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


Synthesizing (advanced) Unit <PSS_RNS_module>.
INFO:Xst:3226 - The RAM <Mram_BUS_0124_GND_7_o_wide_mux_370_OUT> will be implemented
as a BLOCK RAM, absorbing the following register(s): <result_4>
    -----------------------------------------------------------------------
    | ram_type           | Block                                |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     mode           | write-first                          |          |
    |     clkA           | connected to signal <clock>          | rise     |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1210>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to signal <result<4>>      |          |
    -----------------------------------------------------------------------
    | optimization       | speed                                |          |
```

```
    ----------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0031_PWR_7_o_wide_mux_92_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_1>
    ----------------------------------------------------------------------
    | ram_type           | Block                                 |          |
    ----------------------------------------------------------------------
    | Port A                                                     |          |
    |     aspect ratio   | 512-word x 8-bit                      |          |
    |     mode           | write-first                           |          |
    |     clkA           | connected to signal <clock>           | rise     |
    |     weA            | connected to signal <GND>             | high     |
    |     addrA          | connected to signal <n0976>           |          |
    |     diA            | connected to signal <GND>             |          |
    |     doA            | connected to signal <result<1>>       |          |
    ----------------------------------------------------------------------
    | optimization       | speed                                 |          |
    ----------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0062_GND_7_o_wide_mux_185_OUT> will be implemented
as a BLOCK RAM, absorbing the following register(s): <result_2>
    ----------------------------------------------------------------------
    | ram_type           | Block                                 |          |
    ----------------------------------------------------------------------
    | Port A                                                     |          |
    |     aspect ratio   | 512-word x 8-bit                      |          |
    |     mode           | write-first                           |          |
    |     clkA           | connected to signal <clock>           | rise     |
    |     weA            | connected to signal <GND>             | high     |
    |     addrA          | connected to signal <n1054>           |          |
    |     diA            | connected to signal <GND>             |          |
    |     doA            | connected to signal <result<2>>       |          |
    ----------------------------------------------------------------------
    | optimization       | speed                                 |          |
    ----------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0093_PWR_7_o_wide_mux_278_OUT> will be implemented
as a BLOCK RAM, absorbing the following register(s): <result_3>
    ----------------------------------------------------------------------
    | ram_type           | Block                                 |          |
    ----------------------------------------------------------------------
    | Port A                                                     |          |
    |     aspect ratio   | 512-word x 8-bit                      |          |
    |     mode           | write-first                           |          |
    |     clkA           | connected to signal <clock>           | rise     |
    |     weA            | connected to signal <GND>             | high     |
    |     addrA          | connected to signal <n1132>           |          |
    |     diA            | connected to signal <GND>             |          |
    |     doA            | connected to signal <result<3>>       |          |
    ----------------------------------------------------------------------
    | optimization       | speed                                 |          |
    ----------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0155_GND_7_o_wide_mux_463_OUT> will be implemented
as a BLOCK RAM, absorbing the following register(s): <result_5>
    ----------------------------------------------------------------------
    | ram_type           | Block                                 |          |
    ----------------------------------------------------------------------
    | Port A                                                     |          |
    |     aspect ratio   | 512-word x 8-bit                      |          |
    |     mode           | write-first                           |          |
    |     clkA           | connected to signal <clock>           | rise     |
    |     weA            | connected to signal <GND>             | high     |
    |     addrA          | connected to signal <n1288>           |          |
    |     diA            | connected to signal <GND>             |          |
    |     doA            | connected to signal <result<5>>       |          |
    ----------------------------------------------------------------------
    | optimization       | speed                                 |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0095_GND_7_o_wide_mux_312_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
```

```
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1138>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0015_PWR_7_o_wide_mux_60_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 32-word x 5-bit                      |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0928>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0014_PWR_7_o_wide_mux_58_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 128-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0925>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n1801> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 512-word x 40-bit                    |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0922>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0012_PWR_7_o_wide_mux_54_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0919>          |          |
```

```
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0043_PWR_7_o_wide_mux_147_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 128-word x 7-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1012>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0074_PWR_7_o_wide_mux_240_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1090>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0105_PWR_7_o_wide_mux_332_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 128-word x 7-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1168>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0136_PWR_7_o_wide_mux_425_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 128-word x 7-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1246>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0011_PWR_7_o_wide_mux_52_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
```

resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0916>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0042_GND_7_o_wide_mux_145_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1009>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0073_GND_7_o_wide_mux_238_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1087>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0104_GND_7_o_wide_mux_330_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1165>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0135_GND_7_o_wide_mux_423_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	

```
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1243>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0010_GND_7_o_wide_mux_50_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0913>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0041_GND_7_o_wide_mux_143_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1006>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0072_GND_7_o_wide_mux_236_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1084>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0103_GND_7_o_wide_mux_328_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1162>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0134_GND_7_o_wide_mux_421_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
```

of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1240>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0009_GND_7_o_wide_mux_48_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0910>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0040_GND_7_o_wide_mux_141_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1003>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0071_GND_7_o_wide_mux_234_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1081>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0102_GND_7_o_wide_mux_326_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	

```
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1159>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0133_GND_7_o_wide_mux_419_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1237>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0008_PWR_7_o_wide_mux_46_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n0907>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0039_GND_7_o_wide_mux_139_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 256-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1000>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0070_PWR_7_o_wide_mux_232_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 64-word x 6-bit                     |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1078>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
```

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0101_GND_7_o_wide_mux_324_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1156>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0132_GND_7_o_wide_mux_417_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1234>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0007_GND_7_o_wide_mux_44_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0904>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0038_GND_7_o_wide_mux_137_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0997>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0069_GND_7_o_wide_mux_230_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

```
    | ram_type           | Distributed                          |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1075>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0100_PWR_7_o_wide_mux_322_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 128-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1153>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0131_GND_7_o_wide_mux_415_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1231>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0006_PWR_7_o_wide_mux_42_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 128-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0901>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0037_GND_7_o_wide_mux_135_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0994>          |          |
    |     diA            | connected to signal <GND>            |          |
```

```
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0068_GND_7_o_wide_mux_228_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1072>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0099_GND_7_o_wide_mux_320_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1150>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0130_GND_7_o_wide_mux_413_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1228>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0005_GND_7_o_wide_mux_40_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0898>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0036_GND_7_o_wide_mux_133_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
```

resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0991>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0067_PWR_7_o_wide_mux_226_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1069>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0098_GND_7_o_wide_mux_318_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1147>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0129_GND_7_o_wide_mux_411_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1225>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0004_PWR_7_o_wide_mux_38_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	128-word x 7-bit	

```
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0895>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0035_GND_7_o_wide_mux_131_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0988>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0066_PWR_7_o_wide_mux_224_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1066>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0097_GND_7_o_wide_mux_316_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1144>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0128_GND_7_o_wide_mux_409_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1222>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0003_GND_7_o_wide_mux_36_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
```

of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0892>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0034_GND_7_o_wide_mux_129_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0985>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0065_GND_7_o_wide_mux_222_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1063>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0096_GND_7_o_wide_mux_314_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1141>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0127_GND_7_o_wide_mux_407_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	

```
    | Port A                                                                 |
    |     aspect ratio   | 256-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1219>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0002_PWR_7_o_wide_mux_34_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 32-word x 5-bit                     |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n0889>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0033_GND_7_o_wide_mux_127_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 256-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n0982>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0064_PWR_7_o_wide_mux_220_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1060>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0126_GND_7_o_wide_mux_405_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1216>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
```

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0001_PWR_7_o_wide_mux_32_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	128-word x 7-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0886>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0032_GND_7_o_wide_mux_125_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0979>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0063_GND_7_o_wide_mux_218_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1057>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0125_GND_7_o_wide_mux_403_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1213>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0110_GND_7_o_wide_mux_342_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

```
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1171>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0024_PWR_7_o_wide_mux_78_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 64-word x 6-bit                      |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0955>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0023_PWR_7_o_wide_mux_76_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0952>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0054_GND_7_o_wide_mux_169_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1033>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0085_PWR_7_o_wide_mux_262_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1111>          |          |
    |     diA            | connected to signal <GND>            |          |
```

```
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0116_GND_7_o_wide_mux_354_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1189>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0147_GND_7_o_wide_mux_447_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1267>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0022_PWR_7_o_wide_mux_74_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0949>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0053_GND_7_o_wide_mux_167_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1030>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0084_PWR_7_o_wide_mux_260_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
```

resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1108>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0115_GND_7_o_wide_mux_352_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1186>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0146_GND_7_o_wide_mux_445_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1264>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0021_PWR_7_o_wide_mux_72_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0946>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0052_GND_7_o_wide_mux_165_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	

```
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1027>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0083_PWR_7_o_wide_mux_258_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1105>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0114_GND_7_o_wide_mux_350_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1183>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0145_GND_7_o_wide_mux_443_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1261>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0020_PWR_7_o_wide_mux_70_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0943>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0051_GND_7_o_wide_mux_163_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
```

of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1024>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0082_PWR_7_o_wide_mux_256_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1102>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0113_GND_7_o_wide_mux_348_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1180>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0144_GND_7_o_wide_mux_441_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1258>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0019_PWR_7_o_wide_mux_68_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	

```
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                  |          |
    |     weA            | connected to signal <GND>         | high     |
    |     addrA          | connected to signal <n0940>       |          |
    |     diA            | connected to signal <GND>         |          |
    |     doA            | connected to internal node        |          |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0050_GND_7_o_wide_mux_161_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                       |          |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                  |          |
    |     weA            | connected to signal <GND>         | high     |
    |     addrA          | connected to signal <n1021>       |          |
    |     diA            | connected to signal <GND>         |          |
    |     doA            | connected to internal node        |          |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0081_PWR_7_o_wide_mux_254_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                       |          |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                  |          |
    |     weA            | connected to signal <GND>         | high     |
    |     addrA          | connected to signal <n1099>       |          |
    |     diA            | connected to signal <GND>         |          |
    |     doA            | connected to internal node        |          |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0112_GND_7_o_wide_mux_346_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                       |          |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                  |          |
    |     weA            | connected to signal <GND>         | high     |
    |     addrA          | connected to signal <n1177>       |          |
    |     diA            | connected to signal <GND>         |          |
    |     doA            | connected to internal node        |          |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0143_GND_7_o_wide_mux_439_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                       |          |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                  |          |
    |     weA            | connected to signal <GND>         | high     |
    |     addrA          | connected to signal <n1255>       |          |
    |     diA            | connected to signal <GND>         |          |
    |     doA            | connected to internal node        |          |
    ------------------------------------------------------------------------
```

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0018_PWR_7_o_wide_mux_66_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0937>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0049_GND_7_o_wide_mux_159_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1018>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0080_PWR_7_o_wide_mux_252_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1096>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0111_GND_7_o_wide_mux_344_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1174>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0142_GND_7_o_wide_mux_437_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

```
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1252>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0017_GND_7_o_wide_mux_64_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0934>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0048_GND_7_o_wide_mux_157_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1015>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0079_PWR_7_o_wide_mux_250_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1093>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0141_GND_7_o_wide_mux_435_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1249>          |          |
    |     diA            | connected to signal <GND>            |          |
```

```
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0118_GND_7_o_wide_mux_358_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1192>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0028_PWR_7_o_wide_mux_86_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0967>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0059_GND_7_o_wide_mux_179_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1045>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0090_PWR_7_o_wide_mux_272_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1123>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0121_GND_7_o_wide_mux_364_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
```

resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1201>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0152_GND_7_o_wide_mux_457_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1279>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0027_PWR_7_o_wide_mux_84_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0964>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0058_GND_7_o_wide_mux_177_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1042>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0089_PWR_7_o_wide_mux_270_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	

```
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1120>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0120_GND_7_o_wide_mux_362_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1198>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0151_GND_7_o_wide_mux_455_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1276>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0026_PWR_7_o_wide_mux_82_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0961>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0057_GND_7_o_wide_mux_175_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1039>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0088_PWR_7_o_wide_mux_268_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
```

of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1117>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0119_GND_7_o_wide_mux_360_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1195>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0150_GND_7_o_wide_mux_453_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1273>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0025_PWR_7_o_wide_mux_80_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0958>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0056_GND_7_o_wide_mux_173_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	

```
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1036>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0087_PWR_7_o_wide_mux_266_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1114>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0149_GND_7_o_wide_mux_451_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1270>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0122_GND_7_o_wide_mux_366_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n1204>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0030_PWR_7_o_wide_mux_90_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ------------------------------------------------------------------------
    | ram_type           | Distributed                         |           |
    ------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 512-word x 8-bit                    |           |
    |     weA            | connected to signal <GND>           | high      |
    |     addrA          | connected to signal <n0973>         |           |
    |     diA            | connected to signal <GND>           |           |
    |     doA            | connected to internal node          |           |
    ------------------------------------------------------------------------
```

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0061_GND_7_o_wide_mux_183_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1051>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0092_PWR_7_o_wide_mux_276_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1129>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0123_GND_7_o_wide_mux_368_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1207>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0154_GND_7_o_wide_mux_461_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1285>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0029_PWR_7_o_wide_mux_88_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

```
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                    |          |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0970>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0060_GND_7_o_wide_mux_181_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                    |          |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1048>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0091_PWR_7_o_wide_mux_274_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                    |          |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1126>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0153_GND_7_o_wide_mux_459_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                    |          |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1282>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
Unit <PSS_RNS_module> synthesized (advanced).

Synthesizing (advanced) Unit <RNS_ALU_add>.
INFO:Xst:3226 - The RAM <Mram_BUS_0001_PWR_8_o_wide_mux_1_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_1>
    -----------------------------------------------------------------------
    | ram_type           | Block                                |          |
    -----------------------------------------------------------------------
    | Port A                                                    |          |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     mode           | write-first                          |          |
    |     clkA           | connected to signal <clock>          | rise     |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n0042>          |          |
```

```
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to signal <result<1>>    |          |
    ---------------------------------------------------------------------
    | optimization       | speed                              |          |
    ---------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0002_GND_8_o_wide_mux_3_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_2>
    ---------------------------------------------------------------------
    | ram_type           | Block                              |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     mode           | write-first                        |          |
    |     clkA           | connected to signal <clock>        | rise     |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0045>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to signal <result<2>>    |          |
    ---------------------------------------------------------------------
    | optimization       | speed                              |          |
    ---------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0004_GND_8_o_wide_mux_7_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_4>
    ---------------------------------------------------------------------
    | ram_type           | Block                              |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     mode           | write-first                        |          |
    |     clkA           | connected to signal <clock>        | rise     |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0051>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to signal <result<4>>    |          |
    ---------------------------------------------------------------------
    | optimization       | speed                              |          |
    ---------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0003_PWR_8_o_wide_mux_5_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_3>
    ---------------------------------------------------------------------
    | ram_type           | Block                              |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     mode           | write-first                        |          |
    |     clkA           | connected to signal <clock>        | rise     |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0048>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to signal <result<3>>    |          |
    ---------------------------------------------------------------------
    | optimization       | speed                              |          |
    ---------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0005_GND_8_o_wide_mux_9_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_5>
    ---------------------------------------------------------------------
    | ram_type           | Block                              |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     mode           | write-first                        |          |
    |     clkA           | connected to signal <clock>        | rise     |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0054>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to signal <result<5>>    |          |
    ---------------------------------------------------------------------
    | optimization       | speed                              |          |
    ---------------------------------------------------------------------
Unit <RNS_ALU_add> synthesized (advanced).
```

```
Synthesizing (advanced) Unit <RNS_ALU_mul>.
INFO:Xst:3226 - The RAM <Mram_BUS_0001_GND_9_o_wide_mux_6_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_1>
    ---------------------------------------------------------------------
    | ram_type           | Block                                  |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                       |          |
    |     mode           | write-first                            |          |
    |     clkA           | connected to signal <clock>            | rise     |
    |     weA            | connected to signal <GND>              | high     |
    |     addrA          | connected to signal <_n0667>           |          |
    |     diA            | connected to signal <GND>              |          |
    |     doA            | connected to signal <result<1>>        |          |
    |     dorstA         | connected to signal <GND_9_o_op1[1][7]_equal_1_o_0> | high
|
    | reset value        | 00000000                                        |
    ---------------------------------------------------------------------
    | optimization       | speed                                  |          |
    ---------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0002_GND_9_o_wide_mux_23_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_2>
    ---------------------------------------------------------------------
    | ram_type           | Block                                  |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                       |          |
    |     mode           | write-first                            |          |
    |     clkA           | connected to signal <clock>            | rise     |
    |     weA            | connected to signal <GND>              | high     |
    |     addrA          | connected to signal <_n1180>           |          |
    |     diA            | connected to signal <GND>              |          |
    |     doA            | connected to signal <result<2>>        |          |
    |     dorstA         | connected to signal <GND_9_o_op1[2][7]_equal_18_o_0> | high
|
    | reset value        | 00000000                                        |
    ---------------------------------------------------------------------
    | optimization       | speed                                  |          |
    ---------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0004_PWR_9_o_wide_mux_57_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_4>
    ---------------------------------------------------------------------
    | ram_type           | Block                                  |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                       |          |
    |     mode           | write-first                            |          |
    |     clkA           | connected to signal <clock>            | rise     |
    |     weA            | connected to signal <GND>              | high     |
    |     addrA          | connected to signal <_n2206>           |          |
    |     diA            | connected to signal <GND>              |          |
    |     doA            | connected to signal <result<4>>        |          |
    |     dorstA         | connected to signal <GND_9_o_op1[4][7]_equal_52_o_0> | high
|
    | reset value        | 00000000                                        |
    ---------------------------------------------------------------------
    | optimization       | speed                                  |          |
    ---------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0003_PWR_9_o_wide_mux_40_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_3>
    ---------------------------------------------------------------------
    | ram_type           | Block                                  |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                       |          |
    |     mode           | write-first                            |          |
    |     clkA           | connected to signal <clock>            | rise     |
    |     weA            | connected to signal <GND>              | high     |
    |     addrA          | connected to signal <_n1693>           |          |
    |     diA            | connected to signal <GND>              |          |
    |     doA            | connected to signal <result<3>>        |          |
```

```
    |     dorstA         | connected to signal <GND_9_o_op1[3][7]_equal_35_o_0> | high
|
    | reset value        | 00000000                                            |
    --------------------------------------------------------------------------
    | optimization       | speed                                 |           |
    --------------------------------------------------------------------------
INFO:Xst:3226 - The RAM <Mram_BUS_0005_PWR_9_o_wide_mux_74_OUT> will be implemented as
a BLOCK RAM, absorbing the following register(s): <result_5>
    --------------------------------------------------------------------------
    | ram_type           | Block                                 |           |
    --------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 256-word x 8-bit                      |           |
    |     mode           | write-first                           |           |
    |     clkA           | connected to signal <clock>           | rise      |
    |     weA            | connected to signal <GND>             | high      |
    |     addrA          | connected to signal <_n2719>          |           |
    |     diA            | connected to signal <GND>             |           |
    |     doA            | connected to signal <result<5>>       |           |
    |     dorstA         | connected to signal <GND_9_o_op1[5][7]_equal_69_o_0> | high
|
    | reset value        | 00000000                                            |
    --------------------------------------------------------------------------
    | optimization       | speed                                 |           |
    --------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op1[1][7]_GND_9_o_wide_mux_2_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    --------------------------------------------------------------------------
    | ram_type           | Distributed                           |           |
    --------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 256-word x 8-bit                      |           |
    |     weA            | connected to signal <GND>             | high      |
    |     addrA          | connected to signal <op1<1>>          |           |
    |     diA            | connected to signal <GND>             |           |
    |     doA            | connected to internal node            |           |
    --------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op1[2][7]_GND_9_o_wide_mux_19_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    --------------------------------------------------------------------------
    | ram_type           | Distributed                           |           |
    --------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 256-word x 8-bit                      |           |
    |     weA            | connected to signal <GND>             | high      |
    |     addrA          | connected to signal <op1<2>>          |           |
    |     diA            | connected to signal <GND>             |           |
    |     doA            | connected to internal node            |           |
    --------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op1[3][7]_GND_9_o_wide_mux_36_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    --------------------------------------------------------------------------
    | ram_type           | Distributed                           |           |
    --------------------------------------------------------------------------
    | Port A                                                                 |
    |     aspect ratio   | 256-word x 8-bit                      |           |
    |     weA            | connected to signal <GND>             | high      |
    |     addrA          | connected to signal <op1<3>>          |           |
    |     diA            | connected to signal <GND>             |           |
```

```
    |     doA            | connected to internal node         |          |
    --------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op1[4][7]_GND_9_o_wide_mux_53_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    --------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    --------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <op1<4>>       |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    --------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op1[5][7]_GND_9_o_wide_mux_70_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    --------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    --------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <op1<5>>       |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    --------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op2[1][7]_GND_9_o_wide_mux_3_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    --------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    --------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <op2<1>>       |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    --------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op2[2][7]_GND_9_o_wide_mux_20_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    --------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    --------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <op2<2>>       |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    --------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op2[3][7]_GND_9_o_wide_mux_37_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
```

resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <op2<3>>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op2[4][7]_GND_9_o_wide_mux_54_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <op2<4>>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_op2[5][7]_GND_9_o_wide_mux_71_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <op2<5>>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n0667> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n0102>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n1180> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	

```
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0105>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n1693> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0108>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n2206> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0111>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n2719> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0114>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -----------------------------------------------------------------------
Unit <RNS_ALU_mul> synthesized (advanced).

Synthesizing (advanced) Unit <RNS_PSS_module>.
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n2126> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -----------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 32-bit                  |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <A<1>>         |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
```

```
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0001_GND_11_o_wide_mux_3_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 512-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <n0976>         |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0003_PWR_12_o_wide_mux_17_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 512-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <n0981>         |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0007_GND_11_o_wide_mux_44_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 512-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <n0990>         |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0013_GND_11_o_wide_mux_86_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 512-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <n1005>         |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0001_GND_11_o_wide_mux_5_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
```

```
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <BUS_0001_GND_11_o_wide_mux_3_OUT> |
|
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0003_GND_11_o_wide_mux_19_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <BUS_0003_PWR_12_o_wide_mux_17_OUT> |
|
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0007_GND_11_o_wide_mux_46_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <BUS_0007_GND_11_o_wide_mux_44_OUT> |
|
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0013_GND_11_o_wide_mux_88_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <BUS_0013_GND_11_o_wide_mux_86_OUT> |
|
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n4435> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ---------------------------------------------------------------------
```

```
    | Port A                                                                  |
    |     aspect ratio   | 256-word x 24-bit                  |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <BUS_0002_GND_11_o_mux_9_OUT> |
|
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n3152> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    -------------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -------------------------------------------------------------------------
    | Port A                                                                  |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0978>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n2639> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    -------------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -------------------------------------------------------------------------
    | Port A                                                                  |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0983>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n3665> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    -------------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -------------------------------------------------------------------------
    | Port A                                                                  |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0992>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    -------------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n4178> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    -------------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    -------------------------------------------------------------------------
    | Port A                                                                  |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1007>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
```

```
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0002_GND_11_o_wide_mux_8_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 256-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <_n3152>        |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0005_PWR_12_o_wide_mux_31_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 512-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <n0986>         |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0004_PWR_12_o_wide_mux_22_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 256-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <_n2639>        |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0009_GND_11_o_wide_mux_58_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 512-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <n0995>         |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0008_PWR_12_o_wide_mux_49_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
```

```
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <_n3665>        |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0015_GND_11_o_wide_mux_100_OUT> will
be implemented on LUTs either because you have described an asynchronous read or
because of currently unsupported block RAM features. If you have described an
asynchronous read, making it synchronous would allow you to take advantage of
available block RAM resources, for optimized device usage and improved timings. Please
refer to your documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <n1010>         |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0014_PWR_12_o_wide_mux_91_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <_n4178>        |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n4692> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <BUS_0005_PWR_12_o_wide_mux_31_OUT> |
|
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0009_GND_11_o_wide_mux_60_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
```

```
    |     addrA          | connected to signal <BUS_0009_GND_11_o_wide_mux_58_OUT> |
|
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0015_GND_11_o_wide_mux_102_OUT> will
be implemented on LUTs either because you have described an asynchronous read or
because of currently unsupported block RAM features. If you have described an
asynchronous read, making it synchronous would allow you to take advantage of
available block RAM resources, for optimized device usage and improved timings. Please
refer to your documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <BUS_0015_GND_11_o_wide_mux_100_OUT> |
|
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n5205> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <("0",_n4692)> |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n6488> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 16-bit                  |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <BUS_0006_GND_11_o_mux_37_OUT> |
|
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n5718> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n0997>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
```

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n6231> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1012>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0006_PWR_12_o_wide_mux_36_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <_n5205>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0011_GND_11_o_wide_mux_72_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1000>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0010_PWR_12_o_wide_mux_63_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <_n5718>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0017_GND_11_o_wide_mux_114_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

```
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 512-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <n1015>          |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0016_PWR_12_o_wide_mux_105_OUT> will
be implemented on LUTs either because you have described an asynchronous read or
because of currently unsupported block RAM features. If you have described an
asynchronous read, making it synchronous would allow you to take advantage of
available block RAM resources, for optimized device usage and improved timings. Please
refer to your documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <_n6231>         |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0011_GND_11_o_wide_mux_74_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <BUS_0011_GND_11_o_wide_mux_72_OUT> |
|
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0017_GND_11_o_wide_mux_116_OUT> will
be implemented on LUTs either because you have described an asynchronous read or
because of currently unsupported block RAM features. If you have described an
asynchronous read, making it synchronous would allow you to take advantage of
available block RAM resources, for optimized device usage and improved timings. Please
refer to your documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <BUS_0017_GND_11_o_wide_mux_114_OUT> |
|
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    -----------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0012_GND_11_o_wide_mux_125_OUT> will
be implemented on LUTs either because you have described an asynchronous read or
because of currently unsupported block RAM features. If you have described an
asynchronous read, making it synchronous would allow you to take advantage of
available block RAM resources, for optimized device usage and improved timings. Please
refer to your documentation for coding guidelines.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>            | high     |
```

```
    |     addrA          | connected to signal <BUS_0012_GND_11_o_mux_78_OUT> |
|
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n7001> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1002>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n7514> will be implemented on LUTs either
because you have described an asynchronous read or because of currently unsupported
block RAM features. If you have described an asynchronous read, making it synchronous
would allow you to take advantage of available block RAM resources, for optimized
device usage and improved timings. Please refer to your documentation for coding
guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1017>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0012_PWR_12_o_wide_mux_77_OUT> will be
implemented on LUTs either because you have described an asynchronous read or because
of currently unsupported block RAM features. If you have described an asynchronous
read, making it synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 256-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <_n7001>       |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0019_GND_11_o_wide_mux_128_OUT> will
be implemented on LUTs either because you have described an asynchronous read or
because of currently unsupported block RAM features. If you have described an
asynchronous read, making it synchronous would allow you to take advantage of
available block RAM resources, for optimized device usage and improved timings. Please
refer to your documentation for coding guidelines.
    ---------------------------------------------------------------------
    | ram_type           | Distributed                        |          |
    ---------------------------------------------------------------------
    | Port A                                                  |          |
    |     aspect ratio   | 512-word x 8-bit                   |          |
    |     weA            | connected to signal <GND>          | high     |
    |     addrA          | connected to signal <n1020>        |          |
    |     diA            | connected to signal <GND>          |          |
    |     doA            | connected to internal node         |          |
    ---------------------------------------------------------------------
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0018_PWR_12_o_wide_mux_119_OUT> will
be implemented on LUTs either because you have described an asynchronous read or
```

because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <_n7514>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_BUS_0019_GND_11_o_wide_mux_130_OUT> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <BUS_0019_GND_11_o_wide_mux_128_OUT>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n8027> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	512-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <n1022>	
diA	connected to signal <GND>	
doA	connected to internal node	

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram__n8284> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

ram_type	Distributed	
Port A		
aspect ratio	256-word x 8-bit	
weA	connected to signal <GND>	high
addrA	connected to signal <_n8027>	
diA	connected to signal <GND>	
doA	connected to internal node	

Unit <RNS_PSS_module> synthesized (advanced).

==========

Advanced HDL Synthesis Report

Macro Statistics

RAMs : 518

128x7-bit single-port distributed Read Only RAM : 24

```
 256x16-bit single-port distributed Read Only RAM      : 1
 256x24-bit single-port distributed Read Only RAM      : 1
 256x32-bit single-port distributed Read Only RAM      : 1
 256x8-bit single-port block Read Only RAM             : 15
 256x8-bit single-port distributed Read Only RAM       : 117
 32x5-bit single-port distributed Read Only RAM        : 6
 512x40-bit single-port distributed Read Only RAM      : 3
 512x8-bit single-port block Read Only RAM             : 30
 512x8-bit single-port distributed Read Only RAM       : 314
 64x6-bit single-port distributed Read Only RAM        : 6
# Adders/Subtractors                                   : 573
 3-bit adder                                           : 3
 32-bit adder                                          : 104
 4-bit adder                                           : 3
 5-bit adder                                           : 6
 6-bit adder                                           : 6
 7-bit adder                                           : 24
 8-bit adder                                           : 66
 8-bit subtractor                                      : 15
 9-bit adder                                           : 346
# Registers                                            : 72
 Flip-Flops                                            : 72
# Multiplexers                                         : 109
 32-bit 2-to-1 multiplexer                             : 100
 8-bit 2-to-1 multiplexer                              : 9

=========================================================================

=========================================================================
*                           Low Level Synthesis                         *
=========================================================================

Optimizing unit <LR3_V000_Ionisyan> ...

Optimizing unit <RNS_ALU_add> ...

Optimizing unit <PSS_RNS_module> ...

Optimizing unit <RNS_ALU_mul> ...

Optimizing unit <RNS_ALU_neg> ...

Optimizing unit <RNS_PSS_module> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block LR3_V000_Ionisyan, actual ratio is
19.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 72
 Flip-Flops                                            : 72

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------
```

```
================================================================================
*                            Design Summary                                    *
================================================================================

Top Level Output File Name         : LR3_V000_Ionisyan.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 20441
#      GND                         : 1
#      INV                         : 97
#      LUT1                        : 66
#      LUT2                        : 1766
#      LUT3                        : 1279
#      LUT4                        : 874
#      LUT5                        : 2987
#      LUT6                        : 6387
#      MUXCY                       : 2806
#      MUXF7                       : 854
#      MUXF8                       : 400
#      VCC                         : 1
#      XORCY                       : 2923
# FlipFlops/Latches                : 72
#      FD                          : 32
#      FDR                         : 40
# RAMS                             : 45
#      RAMB18E1                    : 45
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 96
#      IBUF                        : 64
#      OBUF                        : 32

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:              72  out of  126800     0%
 Number of Slice LUTs:                13456  out of  63400    21%
    Number used as Logic:             13456  out of  63400    21%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:  13461
   Number with an unused Flip Flop:   13389  out of  13461    99%
   Number with an unused LUT:             5  out of  13461     0%
   Number of fully used LUT-FF pairs:    67  out of  13461     0%
   Number of unique control sets:         6

IO Utilization:
 Number of IOs:                           97
 Number of bonded IOBs:                   97  out of    210    46%

Specific Feature Utilization:
 Number of Block RAM/FIFO:                23  out of    135    17%
    Number using Block RAM only:          23
 Number of BUFG/BUFGCTRLs:                 1  out of     32     3%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


================================================================================
Timing Report
```

```
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 117   |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------
+---------------------------------------------------------------+-------+
Control Signal                     | Buffer(FF name)
| Load  |
-----------------------------------
+---------------------------------------------------------------+-------+
seven<1>(XST_GND:G)                |
NONE(a_plus_b_chip_Mram_BUS_0003_PWR_8_o_wide_mux_5_OUT)| 90    |
-----------------------------------
+---------------------------------------------------------------+-------+

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 94.013ns (Maximum Frequency: 10.637MHz)
   Minimum input arrival time before clock: 14.140ns
   Maximum output required time after clock: 0.640ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 94.013ns (frequency: 10.637MHz)
  Total number of paths / destination ports:
4542743409164522093731705046115889579820063781168735820178929378918 4 / 382
-------------------------------------------------------------------------
Delay:               94.013ns (Levels of Logic = 261)
  Source:            cRNS_chip_Mram_BUS_0001_PWR_8_o_wide_mux_1_OUT (RAM)
  Destination:       cRNS_to_c_chip/result_31 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: cRNS_chip_Mram_BUS_0001_PWR_8_o_wide_mux_1_OUT to
cRNS_to_c_chip/result_31
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     RAMB18E1:CLKARDCLK->DOADO2   19   1.846   0.595
cRNS_chip_Mram_BUS_0001_PWR_8_o_wide_mux_1_OUT (c_RNS<1><2>)
     LUT3:I0->O           10   0.097   0.337  cRNS_to_c_chip_Mram__n2126711_SW0
(cRNS_to_c_chip_N5)
     LUT6:I5->O            2   0.097   0.688  cRNS_to_c_chip_Mram__n21261121
(cRNS_to_c_chip/Msub_GND_11_o_GND_11_o_sub_2_OUT<7:0>_lut<5>)
     LUT5:I0->O            2   0.097   0.299
cRNS_to_c_chip/Msub_GND_11_o_GND_11_o_sub_2_OUT<7:0>_cy<5>11
(cRNS_to_c_chip/Msub_GND_11_o_GND_11_o_sub_2_OUT<7:0>_cy<5>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Madd_n0976_lut<6>
(cRNS_to_c_chip/Madd_n0976_lut<6>)
     MUXCY:S->O            1   0.353   0.000  cRNS_to_c_chip/Madd_n0976_cy<6>
(cRNS_to_c_chip/Madd_n0976_cy<6>)
     MUXCY:CI->O          22   0.253   0.391  cRNS_to_c_chip/Madd_n0976_cy<7>
(cRNS_to_c_chip/Madd_n0976_cy<7>)
```

```
     LUT6:I5->O            1   0.097   0.511
cRNS_to_c_chip_Mram_BUS_0001_GND_11_o_wide_mux_3_OUT1911_SW1 (cRNS_to_c_chip_N721)
     LUT6:I3->O           34   0.097   0.790
cRNS_to_c_chip_Mram_BUS_0001_GND_11_o_wide_mux_3_OUT1911
(cRNS_to_c_chip/BUS_0001_GND_11_o_wide_mux_3_OUT<4>)
     LUT6:I1->O            1   0.097   0.000
cRNS_to_c_chip_Mram_BUS_0001_GND_11_o_wide_mux_5_OUT142
(cRNS_to_c_chip_Mram_BUS_0001_GND_11_o_wide_mux_5_OUT142)
     MUXF7:I1->O           1   0.279   0.000
cRNS_to_c_chip_Mram_BUS_0001_GND_11_o_wide_mux_5_OUT14_f7_0
(cRNS_to_c_chip_Mram_BUS_0001_GND_11_o_wide_mux_5_OUT14_f71)
     MUXF8:I0->O           2   0.218   0.698
cRNS_to_c_chip_Mram_BUS_0001_GND_11_o_wide_mux_5_OUT14_f8
(cRNS_to_c_chip/BUS_0001_GND_11_o_wide_mux_5_OUT<7>)
     LUT6:I0->O            5   0.097   0.398  cRNS_to_c_chip/Madd_n0978_xor<7>11
(cRNS_to_c_chip/n0978<7>)
     LUT2:I0->O            2   0.097   0.299  cRNS_to_c_chip_Mram__n3152911_SW0
(cRNS_to_c_chip_N1531)
     LUT6:I5->O           32   0.097   0.486  cRNS_to_c_chip_Mram__n31521311
(cRNS_to_c_chip_N94)
     LUT6:I4->O            1   0.097   0.000
cRNS_to_c_chip_Mram_BUS_0002_GND_11_o_wide_mux_8_OUT43
(cRNS_to_c_chip_Mram_BUS_0002_GND_11_o_wide_mux_8_OUT42)
     MUXF7:I1->O           1   0.279   0.000
cRNS_to_c_chip_Mram_BUS_0002_GND_11_o_wide_mux_8_OUT4_f7_0
(cRNS_to_c_chip_Mram_BUS_0002_GND_11_o_wide_mux_8_OUT4_f71)
     MUXF8:I0->O           2   0.218   0.299
cRNS_to_c_chip_Mram_BUS_0002_GND_11_o_wide_mux_8_OUT4_f8
(cRNS_to_c_chip/BUS_0002_GND_11_o_wide_mux_8_OUT<2>)
     LUT2:I1->O           15   0.097   0.576
cRNS_to_c_chip/BUS_0002_GND_11_o_mux_9_OUT<2>_mand11
(cRNS_to_c_chip/BUS_0002_GND_11_o_mux_9_OUT<2>_mand1)
     LUT3:I0->O            5   0.097   0.314  cRNS_to_c_chip_Mram__n44351121_SW0
(cRNS_to_c_chip_N1031)
     LUT6:I5->O            4   0.097   0.525  cRNS_to_c_chip_Mram__n44351121
(cRNS_to_c_chip/_n4435<3>)
     LUT5:I2->O            1   0.097   0.000  cRNS_to_c_chip/Madd_n0986_lut<3>
(cRNS_to_c_chip/Madd_n0986_lut<3>)
     MUXCY:S->O            1   0.353   0.000  cRNS_to_c_chip/Madd_n0986_cy<3>
(cRNS_to_c_chip/Madd_n0986_cy<3>)
     XORCY:CI->O          17   0.370   0.586  cRNS_to_c_chip/Madd_n0986_xor<4>
(cRNS_to_c_chip/n0986<4>)
     LUT6:I3->O            1   0.097   0.379
cRNS_to_c_chip_Mram_BUS_0005_PWR_12_o_wide_mux_31_OUT13115_SW0 (cRNS_to_c_chip_N323)
     LUT5:I3->O            1   0.097   0.295
cRNS_to_c_chip_Mram_BUS_0005_PWR_12_o_wide_mux_31_OUT13115
(cRNS_to_c_chip_Mram_BUS_0005_PWR_12_o_wide_mux_31_OUT13114)
     LUT5:I4->O           26   0.097   0.485
cRNS_to_c_chip_Mram_BUS_0005_PWR_12_o_wide_mux_31_OUT131110
(cRNS_to_c_chip/BUS_0005_PWR_12_o_wide_mux_31_OUT<2>)
     LUT6:I4->O            1   0.097   0.000  cRNS_to_c_chip_Mram__n469261
(cRNS_to_c_chip_Mram__n469261)
     MUXF7:I1->O           1   0.279   0.000  cRNS_to_c_chip_Mram__n46926_f7_0
(cRNS_to_c_chip_Mram__n46926_f71)
     MUXF8:I0->O           6   0.218   0.716  cRNS_to_c_chip_Mram__n46926_f8
(cRNS_to_c_chip_Mram__n46926_f8)
     LUT6:I0->O           32   0.097   0.663  cRNS_to_c_chip_Mram__n520510111
(cRNS_to_c_chip_N237)
     LUT6:I2->O            1   0.097   0.000
cRNS_to_c_chip_Mram_BUS_0006_PWR_12_o_wide_mux_36_OUT43
(cRNS_to_c_chip_Mram_BUS_0006_PWR_12_o_wide_mux_36_OUT42)
     MUXF7:I1->O           1   0.279   0.000
cRNS_to_c_chip_Mram_BUS_0006_PWR_12_o_wide_mux_36_OUT4_f7_0
(cRNS_to_c_chip_Mram_BUS_0006_PWR_12_o_wide_mux_36_OUT4_f71)
     MUXF8:I0->O           2   0.218   0.299
cRNS_to_c_chip_Mram_BUS_0006_PWR_12_o_wide_mux_36_OUT4_f8
(cRNS_to_c_chip/BUS_0006_PWR_12_o_wide_mux_36_OUT<2>)
     LUT2:I1->O           10   0.097   0.553
cRNS_to_c_chip/BUS_0006_GND_11_o_mux_37_OUT<2>_mand11
(cRNS_to_c_chip/BUS_0006_GND_11_o_mux_37_OUT<2>_mand1)
```

```
     LUT3:I0->O            5   0.097   0.314  cRNS_to_c_chip_Mram__n6488711_SW0
(cRNS_to_c_chip_N2281)
     LUT6:I5->O            4   0.097   0.525  cRNS_to_c_chip_Mram__n6488711
(cRNS_to_c_chip/Msub_GND_11_o_GND_11_o_sub_71_OUT<7:0>_lut<3>)
     LUT5:I2->O            1   0.097   0.000  cRNS_to_c_chip/Madd_n1000_lut<3>
(cRNS_to_c_chip/Madd_n1000_lut<3>)
     MUXCY:S->O            1   0.353   0.000  cRNS_to_c_chip/Madd_n1000_cy<3>
(cRNS_to_c_chip/Madd_n1000_cy<3>)
     XORCY:CI->O          14   0.370   0.571  cRNS_to_c_chip/Madd_n1000_xor<4>
(cRNS_to_c_chip/n1000<4>)
     LUT6:I3->O            1   0.097   0.379
cRNS_to_c_chip_Mram_BUS_0011_GND_11_o_wide_mux_72_OUT7118_SW1 (cRNS_to_c_chip_N796)
     LUT6:I4->O           33   0.097   0.800
cRNS_to_c_chip_Mram_BUS_0011_GND_11_o_wide_mux_72_OUT7118
(cRNS_to_c_chip/BUS_0011_GND_11_o_wide_mux_72_OUT<1>)
     LUT6:I0->O            1   0.097   0.000
cRNS_to_c_chip_Mram_BUS_0011_GND_11_o_wide_mux_74_OUT103
(cRNS_to_c_chip_Mram_BUS_0011_GND_11_o_wide_mux_74_OUT103)
     MUXF7:I0->O           1   0.277   0.000
cRNS_to_c_chip_Mram_BUS_0011_GND_11_o_wide_mux_74_OUT10_f7_0
(cRNS_to_c_chip_Mram_BUS_0011_GND_11_o_wide_mux_74_OUT10_f71)
     MUXF8:I0->O           3   0.218   0.703
cRNS_to_c_chip_Mram_BUS_0011_GND_11_o_wide_mux_74_OUT10_f8
(cRNS_to_c_chip/BUS_0011_GND_11_o_wide_mux_74_OUT<5>)
     LUT6:I0->O            2   0.097   0.299  cRNS_to_c_chip/Madd_n1002_cy<6>11
(cRNS_to_c_chip/Madd_n1002_cy<6>)
     LUT2:I1->O            5   0.097   0.398  cRNS_to_c_chip/Madd_n1002_xor<7>11
(cRNS_to_c_chip/n1002<7>)
     LUT6:I4->O           32   0.097   0.618  cRNS_to_c_chip_Mram__n700114111
(cRNS_to_c_chip_N207)
     LUT6:I3->O            1   0.097   0.000
cRNS_to_c_chip_Mram_BUS_0012_PWR_12_o_wide_mux_77_OUT62
(cRNS_to_c_chip_Mram_BUS_0012_PWR_12_o_wide_mux_77_OUT62)
     MUXF7:I1->O           1   0.279   0.000
cRNS_to_c_chip_Mram_BUS_0012_PWR_12_o_wide_mux_77_OUT6_f7_0
(cRNS_to_c_chip_Mram_BUS_0012_PWR_12_o_wide_mux_77_OUT6_f71)
     MUXF8:I0->O           2   0.218   0.299
cRNS_to_c_chip_Mram_BUS_0012_PWR_12_o_wide_mux_77_OUT6_f8
(cRNS_to_c_chip/BUS_0012_PWR_12_o_wide_mux_77_OUT<3>)
     LUT2:I1->O            8   0.097   0.544
cRNS_to_c_chip/BUS_0012_GND_11_o_mux_78_OUT<3>_mand11
(cRNS_to_c_chip/BUS_0012_GND_11_o_mux_78_OUT<3>_mand1)
     LUT3:I0->O            1   0.097   0.295
cRNS_to_c_chip_Mram_BUS_0012_GND_11_o_wide_mux_125_OUT121_SW0 (cRNS_to_c_chip_N268)
     LUT6:I5->O            1   0.097   0.295
cRNS_to_c_chip_Mram_BUS_0012_GND_11_o_wide_mux_125_OUT121
(cRNS_to_c_chip/BUS_0012_GND_11_o_wide_mux_125_OUT<0>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Madd_n1020_lut<0>
(cRNS_to_c_chip/Madd_n1020_lut<0>)
     MUXCY:S->O            1   0.353   0.000  cRNS_to_c_chip/Madd_n1020_cy<0>
(cRNS_to_c_chip/Madd_n1020_cy<0>)
     XORCY:CI->O          23   0.370   0.781  cRNS_to_c_chip/Madd_n1020_xor<1>
(cRNS_to_c_chip/n1020<1>)
     LUT6:I1->O            1   0.097   0.511
cRNS_to_c_chip_Mram_BUS_0019_GND_11_o_wide_mux_128_OUT1911_SW0 (cRNS_to_c_chip_N299)
     LUT6:I3->O           33   0.097   0.790
cRNS_to_c_chip_Mram_BUS_0019_GND_11_o_wide_mux_128_OUT1911
(cRNS_to_c_chip/BUS_0019_GND_11_o_wide_mux_128_OUT<4>)
     LUT6:I1->O            1   0.097   0.000
cRNS_to_c_chip_Mram_BUS_0019_GND_11_o_wide_mux_130_OUT102
(cRNS_to_c_chip_Mram_BUS_0019_GND_11_o_wide_mux_130_OUT102)
     MUXF7:I1->O           1   0.279   0.000
cRNS_to_c_chip_Mram_BUS_0019_GND_11_o_wide_mux_130_OUT10_f7_0
(cRNS_to_c_chip_Mram_BUS_0019_GND_11_o_wide_mux_130_OUT10_f71)
     MUXF8:I0->O           2   0.218   0.697
cRNS_to_c_chip_Mram_BUS_0019_GND_11_o_wide_mux_130_OUT10_f8
(cRNS_to_c_chip/Madd_n1022_lut<5>)
     LUT6:I0->O            3   0.097   0.305  cRNS_to_c_chip/Madd_n1022_cy<5>11
(cRNS_to_c_chip/Madd_n1022_cy<5>)
     LUT3:I2->O           10   0.097   0.725  cRNS_to_c_chip/Madd_n1022_xor<7>11
(cRNS_to_c_chip/n1022<7>)
```

```
     LUT6:I1->O           32   0.097   0.790  cRNS_to_c_chip_Mram__n8027411
(cRNS_to_c_chip_N227)
     LUT6:I1->O            1   0.097   0.000  cRNS_to_c_chip_Mram__n8284142
(cRNS_to_c_chip_Mram__n8284142)
     MUXF7:I1->O           1   0.279   0.000  cRNS_to_c_chip_Mram__n828414_f7_0
(cRNS_to_c_chip_Mram__n828414_f71)
     MUXF8:I0->O          28   0.218   0.617  cRNS_to_c_chip_Mram__n828414_f8
(cRNS_to_c_chip/_n8284<0>)
     LUT4:I1->O            1   0.097   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_lut<7>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_lut<7>)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<7>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<7>)
     MUXCY:CI->O           1   0.023   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<8>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<8>)
     MUXCY:CI->O           1   0.023   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<9>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<9>)
     MUXCY:CI->O           1   0.023   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<10>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<10>)
     MUXCY:CI->O           0   0.023   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<11>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_cy<11>)
     XORCY:CI->O           4   0.370   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_220_OUT_xor<12>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_220_OUT<12>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1159411
(cRNS_to_c_chip/Mmux_n115941)
     MUXCY:S->O            0   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_223_OUT_cy<13>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_223_OUT_cy<13>)
     XORCY:CI->O           4   0.370   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_223_OUT_xor<14>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_223_OUT<14>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1164611
(cRNS_to_c_chip/Mmux_n116461)
     MUXCY:S->O            0   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_226_OUT_cy<15>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_226_OUT_cy<15>)
     XORCY:CI->O           3   0.370   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_226_OUT_xor<16>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_226_OUT<16>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1169811
(cRNS_to_c_chip/Mmux_n116981)
     MUXCY:S->O            0   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_229_OUT_cy<17>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_229_OUT_cy<17>)
     XORCY:CI->O           2   0.370   0.299
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_229_OUT_xor<18>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_229_OUT<18>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n11741011
(cRNS_to_c_chip/Mmux_n1174101)
     MUXCY:S->O            0   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_232_OUT_cy<19>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_232_OUT_cy<19>)
     XORCY:CI->O           1   0.370   0.295
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_232_OUT_xor<20>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_232_OUT<20>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1180131
(cRNS_to_c_chip/n1180<20>)
     MUXCY:S->O            0   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_234_OUT_cy<20>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_234_OUT_cy<20>)
     XORCY:CI->O          23   0.370   0.377
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_234_OUT_xor<21>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_234_OUT<21>)
```

```
     INV:I->O              1   0.113   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_270_OUT_lut<2>_INV_0
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_270_OUT_lut<2>)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_270_OUT_cy<2>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_270_OUT_cy<2>)
     XORCY:CI->O           4   0.370   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_270_OUT_xor<3>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_270_OUT<3>)
     LUT3:I2->O            1   0.097   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_273_OUT_lut<4>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_273_OUT_lut<4>)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_273_OUT_cy<4>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_273_OUT_cy<4>)
     XORCY:CI->O           3   0.370   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_273_OUT_xor<5>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_273_OUT<5>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n12472711
(cRNS_to_c_chip/Mmux_n1247271)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_276_OUT_cy<6>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_276_OUT_cy<6>)
     XORCY:CI->O           4   0.370   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_276_OUT_xor<7>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_276_OUT<7>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n12522911
(cRNS_to_c_chip/Mmux_n1252291)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_279_OUT_cy<8>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_279_OUT_cy<8>)
     XORCY:CI->O           3   0.370   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_279_OUT_xor<9>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_279_OUT<9>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n12573111
(cRNS_to_c_chip/Mmux_n1257311)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_282_OUT_cy<10>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_282_OUT_cy<10>)
     XORCY:CI->O           4   0.370   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_282_OUT_xor<11>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_282_OUT<11>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1262321
(cRNS_to_c_chip/Mmux_n126232)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_285_OUT_cy<12>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_285_OUT_cy<12>)
     XORCY:CI->O           3   0.370   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_285_OUT_xor<13>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_285_OUT<13>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1267511
(cRNS_to_c_chip/Mmux_n126751)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_288_OUT_cy<14>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_288_OUT_cy<14>)
     XORCY:CI->O           4   0.370   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_288_OUT_xor<15>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_288_OUT<15>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1272711
(cRNS_to_c_chip/Mmux_n127271)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_291_OUT_cy<16>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_291_OUT_cy<16>)
     XORCY:CI->O           3   0.370   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_291_OUT_xor<17>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_291_OUT<17>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1277911
(cRNS_to_c_chip/Mmux_n127791)
     MUXCY:S->O            1   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_294_OUT_cy<18>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_294_OUT_cy<18>)
```

```
     XORCY:CI->O           4   0.370   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_294_OUT_xor<19>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_294_OUT<19>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n12821111
(cRNS_to_c_chip/Mmux_n1282111)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_297_OUT_xor<20>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_297_OUT<20>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n12871311
(cRNS_to_c_chip/Mmux_n1287131)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_300_OUT_xor<21>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_300_OUT<21>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n12921411
(cRNS_to_c_chip/Mmux_n1292141)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_303_OUT_xor<22>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_303_OUT<22>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n12971511
(cRNS_to_c_chip/Mmux_n1297151)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_306_OUT_xor<23>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_306_OUT<23>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13021611
(cRNS_to_c_chip/Mmux_n1302161)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_309_OUT_xor<24>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_309_OUT<24>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13071711
(cRNS_to_c_chip/Mmux_n1307171)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_312_OUT_xor<25>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_312_OUT<25>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13121811
(cRNS_to_c_chip/Mmux_n1312181)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_315_OUT_xor<26>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_315_OUT<26>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13171911
(cRNS_to_c_chip/Mmux_n1317191)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_318_OUT_xor<27>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_318_OUT<27>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13222011
(cRNS_to_c_chip/Mmux_n1322201)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_321_OUT_xor<28>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_321_OUT<28>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13272111
(cRNS_to_c_chip/Mmux_n1327211)
     XORCY:LI->O           2   0.173   0.299
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_324_OUT_xor<29>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_324_OUT<29>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13322211
(cRNS_to_c_chip/Mmux_n1332221)
     XORCY:LI->O           1   0.173   0.295
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_327_OUT_xor<30>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_327_OUT<30>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n1338241
(cRNS_to_c_chip/n1338<30>)
     XORCY:LI->O           4   0.173   0.293
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_329_OUT_xor<30>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_329_OUT<30>)
     INV:I->O              1   0.113   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_338_OUT_lut<2>_INV_0
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_338_OUT_lut<2>)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_338_OUT_xor<2>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_338_OUT<2>)
     LUT3:I2->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13552311
(cRNS_to_c_chip/Mmux_n1355231)
```

```
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_341_OUT_xor<3>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_341_OUT<3>)
     LUT5:I4->O            1   0.097   0.000  cRNS_to_c_chip/Mmux_n13602511
(cRNS_to_c_chip/Mmux_n1360251)
     MUXCY:S->O            0   0.353   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_344_OUT_cy<4>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_344_OUT_cy<4>)
     XORCY:CI->O           4   0.370   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_344_OUT_xor<5>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_344_OUT<5>)
     LUT3:I2->O            0   0.097   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_347_OUT_lut<6>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_347_OUT_lut<6>)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_347_OUT_xor<6>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_347_OUT<6>)
     LUT5:I4->O            0   0.097   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_350_OUT_lut<7>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_350_OUT_lut<7>)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_350_OUT_xor<7>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_350_OUT<7>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n13752911
(cRNS_to_c_chip/Mmux_n1375291)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_353_OUT_xor<8>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_353_OUT<8>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n13803011
(cRNS_to_c_chip/Mmux_n1380301)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_356_OUT_xor<9>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_356_OUT<9>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n13853111
(cRNS_to_c_chip/Mmux_n1385311)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_359_OUT_xor<10>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_359_OUT<10>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1390211
(cRNS_to_c_chip/Mmux_n139021)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_362_OUT_xor<11>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_362_OUT<11>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1395321
(cRNS_to_c_chip/Mmux_n139532)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_365_OUT_xor<12>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_365_OUT<12>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1400411
(cRNS_to_c_chip/Mmux_n140041)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_368_OUT_xor<13>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_368_OUT<13>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1405511
(cRNS_to_c_chip/Mmux_n140551)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_371_OUT_xor<14>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_371_OUT<14>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1410611
(cRNS_to_c_chip/Mmux_n141061)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_374_OUT_xor<15>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_374_OUT<15>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1415711
(cRNS_to_c_chip/Mmux_n141571)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_377_OUT_xor<16>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_377_OUT<16>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1420811
(cRNS_to_c_chip/Mmux_n142081)
```

```
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_380_OUT_xor<17>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_380_OUT<17>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1425911
(cRNS_to_c_chip/Mmux_n142591)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_383_OUT_xor<18>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_383_OUT<18>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14301011
(cRNS_to_c_chip/Mmux_n1430101)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_386_OUT_xor<19>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_386_OUT<19>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14351111
(cRNS_to_c_chip/Mmux_n1435111)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_389_OUT_xor<20>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_389_OUT<20>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14401311
(cRNS_to_c_chip/Mmux_n1440131)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_392_OUT_xor<21>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_392_OUT<21>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14451411
(cRNS_to_c_chip/Mmux_n1445141)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_395_OUT_xor<22>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_395_OUT<22>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14501511
(cRNS_to_c_chip/Mmux_n1450151)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_398_OUT_xor<23>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_398_OUT<23>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14551611
(cRNS_to_c_chip/Mmux_n1455161)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_401_OUT_xor<24>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_401_OUT<24>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14601711
(cRNS_to_c_chip/Mmux_n1460171)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_404_OUT_xor<25>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_404_OUT<25>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14651811
(cRNS_to_c_chip/Mmux_n1465181)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_407_OUT_xor<26>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_407_OUT<26>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14701911
(cRNS_to_c_chip/Mmux_n1470191)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_410_OUT_xor<27>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_410_OUT<27>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14752011
(cRNS_to_c_chip/Mmux_n1475201)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_413_OUT_xor<28>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_413_OUT<28>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14802111
(cRNS_to_c_chip/Mmux_n1480211)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_416_OUT_xor<29>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_416_OUT<29>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14852211
(cRNS_to_c_chip/Mmux_n1485221)
     XORCY:LI->O           2   0.173   0.299
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_419_OUT_xor<30>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_419_OUT<30>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n14902411
(cRNS_to_c_chip/Mmux_n1490241)
```

```
     XORCY:LI->O           1   0.173   0.295
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_422_OUT_xor<31>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_422_OUT<31>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1496251
(cRNS_to_c_chip/n1496<31>)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_424_OUT_xor<31>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_424_OUT<31>)
     LUT2:I1->O            0   0.097   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_433_OUT_lut<3>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_433_OUT_lut<3>)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_433_OUT_xor<3>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_433_OUT<3>)
     LUT4:I3->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n15132511
(cRNS_to_c_chip/Mmux_n1513251)
     XORCY:LI->O           2   0.173   0.300
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_436_OUT_xor<4>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_436_OUT<4>)
     LUT6:I5->O            0   0.097   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_439_OUT_lut<5>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_439_OUT_lut<5>)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_439_OUT_xor<5>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_439_OUT<5>)
     LUT3:I2->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n15232711
(cRNS_to_c_chip/Mmux_n1523271)
     XORCY:LI->O           2   0.173   0.299
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_442_OUT_xor<6>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_442_OUT<6>)
     LUT5:I4->O            0   0.097   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_445_OUT_lut<7>
(cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_445_OUT_lut<7>)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_445_OUT_xor<7>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_445_OUT<7>)
     LUT3:I2->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n15332911
(cRNS_to_c_chip/Mmux_n1533291)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_448_OUT_xor<8>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_448_OUT<8>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n15383011
(cRNS_to_c_chip/Mmux_n1538301)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_451_OUT_xor<9>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_451_OUT<9>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n15433111
(cRNS_to_c_chip/Mmux_n1543311)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_454_OUT_xor<10>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_454_OUT<10>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1548211
(cRNS_to_c_chip/Mmux_n154821)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_457_OUT_xor<11>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_457_OUT<11>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1553321
(cRNS_to_c_chip/Mmux_n155332)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_460_OUT_xor<12>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_460_OUT<12>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1558411
(cRNS_to_c_chip/Mmux_n155841)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_463_OUT_xor<13>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_463_OUT<13>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1563511
(cRNS_to_c_chip/Mmux_n156351)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_466_OUT_xor<14>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_466_OUT<14>)
```

```
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1568611
(cRNS_to_c_chip/Mmux_n156861)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_469_OUT_xor<15>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_469_OUT<15>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1573711
(cRNS_to_c_chip/Mmux_n157371)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_472_OUT_xor<16>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_472_OUT<16>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1578811
(cRNS_to_c_chip/Mmux_n157881)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_475_OUT_xor<17>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_475_OUT<17>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1583911
(cRNS_to_c_chip/Mmux_n158391)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_478_OUT_xor<18>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_478_OUT<18>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n15881011
(cRNS_to_c_chip/Mmux_n1588101)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_481_OUT_xor<19>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_481_OUT<19>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n15931111
(cRNS_to_c_chip/Mmux_n1593111)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_484_OUT_xor<20>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_484_OUT<20>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n15981311
(cRNS_to_c_chip/Mmux_n1598131)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_487_OUT_xor<21>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_487_OUT<21>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16031411
(cRNS_to_c_chip/Mmux_n1603141)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_490_OUT_xor<22>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_490_OUT<22>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16081511
(cRNS_to_c_chip/Mmux_n1608151)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_493_OUT_xor<23>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_493_OUT<23>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16131611
(cRNS_to_c_chip/Mmux_n1613161)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_496_OUT_xor<24>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_496_OUT<24>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16181711
(cRNS_to_c_chip/Mmux_n1618171)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_499_OUT_xor<25>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_499_OUT<25>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16231811
(cRNS_to_c_chip/Mmux_n1623181)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_502_OUT_xor<26>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_502_OUT<26>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16281911
(cRNS_to_c_chip/Mmux_n1628191)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_505_OUT_xor<27>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_505_OUT<27>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16332011
(cRNS_to_c_chip/Mmux_n1633201)
     XORCY:LI->O           4   0.173   0.309
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_508_OUT_xor<28>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_508_OUT<28>)
```

```
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16382111
(cRNS_to_c_chip/Mmux_n1638211)
     XORCY:LI->O           3   0.173   0.305
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_511_OUT_xor<29>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_511_OUT<29>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16432211
(cRNS_to_c_chip/Mmux_n1643221)
     XORCY:LI->O           2   0.173   0.299
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_514_OUT_xor<30>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_514_OUT<30>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n16482411
(cRNS_to_c_chip/Mmux_n1648241)
     XORCY:LI->O           1   0.173   0.295
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_517_OUT_xor<31>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_517_OUT<31>)
     LUT5:I4->O            0   0.097   0.000  cRNS_to_c_chip/Mmux_n1654251
(cRNS_to_c_chip/n1654<31>)
     XORCY:LI->O           1   0.173   0.000
cRNS_to_c_chip/Madd_GND_11_o_GND_11_o_add_519_OUT_xor<31>
(cRNS_to_c_chip/GND_11_o_GND_11_o_add_519_OUT<31>)
     FD:D                      0.008          cRNS_to_c_chip/result_31
    ----------------------------------------
    Total                     94.013ns (45.188ns logic, 48.825ns route)
                                       (48.1% logic, 51.9% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 394677993036 / 90
-------------------------------------------------------------------------
Offset:              14.140ns (Levels of Logic = 37)
  Source:            b<29> (PAD)
  Destination:       b_to_bRNS_chip_Mram_BUS_0093_PWR_7_o_wide_mux_278_OUT (RAM)
  Destination Clock: clk rising

  Data Path: b<29> to b_to_bRNS_chip_Mram_BUS_0093_PWR_7_o_wide_mux_278_OUT
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            44   0.001   0.488  b_29_IBUF (b_29_IBUF)
     LUT2:I0->O           34   0.097   0.800
b_to_bRNS_chip/Mram_BUS_0002_PWR_7_o_wide_mux_34_OUT31
(b_to_bRNS_chip/Mram_BUS_0002_PWR_7_o_wide_mux_34_OUT3)
     LUT6:I0->O            1   0.097   0.556
b_to_bRNS_chip_Mram_BUS_0064_PWR_7_o_wide_mux_220_OUT8111
(b_to_bRNS_chip_Mram_BUS_0064_PWR_7_o_wide_mux_220_OUT811)
     LUT5:I1->O            1   0.097   0.000
b_to_bRNS_chip_Mram_BUS_0064_PWR_7_o_wide_mux_220_OUT8114_F (b_to_bRNS_chip_N1112)
     MUXF7:I0->O           1   0.277   0.379
b_to_bRNS_chip_Mram_BUS_0064_PWR_7_o_wide_mux_220_OUT8114
(b_to_bRNS_chip/BUS_0064_PWR_7_o_wide_mux_220_OUT<1>)
     LUT2:I0->O            1   0.097   0.000  b_to_bRNS_chip/Madd_n1093_lut<1>
(b_to_bRNS_chip/Madd_n1093_lut<1>)
     MUXCY:S->O            1   0.353   0.000  b_to_bRNS_chip/Madd_n1093_cy<1>
(b_to_bRNS_chip/Madd_n1093_cy<1>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1093_cy<2>
(b_to_bRNS_chip/Madd_n1093_cy<2>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1093_cy<3>
(b_to_bRNS_chip/Madd_n1093_cy<3>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1093_cy<4>
(b_to_bRNS_chip/Madd_n1093_cy<4>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1093_cy<5>
(b_to_bRNS_chip/Madd_n1093_cy<5>)
     XORCY:CI->O          26   0.370   0.799  b_to_bRNS_chip/Madd_n1093_xor<6>
(b_to_bRNS_chip/n1093<6>)
     LUT6:I0->O            1   0.097   0.683
b_to_bRNS_chip_Mram_BUS_0079_PWR_7_o_wide_mux_250_OUT18111
(b_to_bRNS_chip_Mram_BUS_0079_PWR_7_o_wide_mux_250_OUT1811)
     LUT6:I1->O            1   0.097   0.295
b_to_bRNS_chip_Mram_BUS_0079_PWR_7_o_wide_mux_250_OUT18113
(b_to_bRNS_chip_Mram_BUS_0079_PWR_7_o_wide_mux_250_OUT18112)
```

```
     LUT6:I5->O            1   0.097   0.295
b_to_bRNS_chip_Mram_BUS_0079_PWR_7_o_wide_mux_250_OUT18117
(b_to_bRNS_chip/BUS_0079_PWR_7_o_wide_mux_250_OUT<3>)
     LUT2:I1->O            1   0.097   0.000  b_to_bRNS_chip/Madd_n1114_lut<3>
(b_to_bRNS_chip/Madd_n1114_lut<3>)
     MUXCY:S->O            1   0.353   0.000  b_to_bRNS_chip/Madd_n1114_cy<3>
(b_to_bRNS_chip/Madd_n1114_cy<3>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1114_cy<4>
(b_to_bRNS_chip/Madd_n1114_cy<4>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1114_cy<5>
(b_to_bRNS_chip/Madd_n1114_cy<5>)
     XORCY:CI->O          27   0.370   0.799  b_to_bRNS_chip/Madd_n1114_xor<6>
(b_to_bRNS_chip/n1114<6>)
     LUT6:I0->O            1   0.097   0.683
b_to_bRNS_chip_Mram_BUS_0087_PWR_7_o_wide_mux_266_OUT18111
(b_to_bRNS_chip_Mram_BUS_0087_PWR_7_o_wide_mux_266_OUT1811)
     LUT6:I1->O            1   0.097   0.295
b_to_bRNS_chip_Mram_BUS_0087_PWR_7_o_wide_mux_266_OUT18113
(b_to_bRNS_chip_Mram_BUS_0087_PWR_7_o_wide_mux_266_OUT18112)
     LUT6:I5->O            1   0.097   0.295
b_to_bRNS_chip_Mram_BUS_0087_PWR_7_o_wide_mux_266_OUT18117
(b_to_bRNS_chip/BUS_0087_PWR_7_o_wide_mux_266_OUT<3>)
     LUT2:I1->O            1   0.097   0.000  b_to_bRNS_chip/Madd_n1126_lut<3>
(b_to_bRNS_chip/Madd_n1126_lut<3>)
     MUXCY:S->O            1   0.353   0.000  b_to_bRNS_chip/Madd_n1126_cy<3>
(b_to_bRNS_chip/Madd_n1126_cy<3>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1126_cy<4>
(b_to_bRNS_chip/Madd_n1126_cy<4>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1126_cy<5>
(b_to_bRNS_chip/Madd_n1126_cy<5>)
     XORCY:CI->O          27   0.370   0.799  b_to_bRNS_chip/Madd_n1126_xor<6>
(b_to_bRNS_chip/n1126<6>)
     LUT6:I0->O            1   0.097   0.683
b_to_bRNS_chip_Mram_BUS_0091_PWR_7_o_wide_mux_274_OUT18111
(b_to_bRNS_chip_Mram_BUS_0091_PWR_7_o_wide_mux_274_OUT1811)
     LUT6:I1->O            1   0.097   0.295
b_to_bRNS_chip_Mram_BUS_0091_PWR_7_o_wide_mux_274_OUT18113
(b_to_bRNS_chip_Mram_BUS_0091_PWR_7_o_wide_mux_274_OUT18112)
     LUT6:I5->O            1   0.097   0.295
b_to_bRNS_chip_Mram_BUS_0091_PWR_7_o_wide_mux_274_OUT18117
(b_to_bRNS_chip/BUS_0091_PWR_7_o_wide_mux_274_OUT<3>)
     LUT2:I1->O            1   0.097   0.000  b_to_bRNS_chip/Madd_n1132_lut<3>
(b_to_bRNS_chip/Madd_n1132_lut<3>)
     MUXCY:S->O            1   0.353   0.000  b_to_bRNS_chip/Madd_n1132_cy<3>
(b_to_bRNS_chip/Madd_n1132_cy<3>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1132_cy<4>
(b_to_bRNS_chip/Madd_n1132_cy<4>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1132_cy<5>
(b_to_bRNS_chip/Madd_n1132_cy<5>)
     MUXCY:CI->O           1   0.023   0.000  b_to_bRNS_chip/Madd_n1132_cy<6>
(b_to_bRNS_chip/Madd_n1132_cy<6>)
     XORCY:CI->O           1   0.370   0.279  b_to_bRNS_chip/Madd_n1132_xor<7>
(b_to_bRNS_chip/n1132<7>)
     RAMB18E1:ADDRARDADDR10        0.442
b_to_bRNS_chip_Mram_BUS_0093_PWR_7_o_wide_mux_278_OUT
    ----------------------------------------
    Total                     14.140ns (5.417ns logic, 8.723ns route)
                                       (38.3% logic, 61.7% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 32 / 32
--------------------------------------------------------------------------
Offset:              0.640ns (Levels of Logic = 1)
  Source:            cRNS_to_c_chip/result_31 (FF)
  Destination:       c<31> (PAD)
  Source Clock:      clk rising

  Data Path: cRNS_to_c_chip/result_31 to c<31>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
```

```
    ----------------------------------------  ------------
     FD:C->Q               1   0.361   0.279  cRNS_to_c_chip/result_31
(cRNS_to_c_chip/result_31)
     OBUF:I->O                 0.000          c_31_OBUF (c<31>)
    ----------------------------------------
    Total                      0.640ns (0.361ns logic, 0.279ns route)
                                       (56.4% logic, 43.6% route)

==========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |   94.013|         |         |         |
---------------+---------+---------+---------+---------+

==========================================================================


Total REAL time to Xst completion: 272.00 secs
Total CPU time to Xst completion: 267.37 secs

-->


Total memory usage is 605888 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    2 (   0 filtered)
Number of infos    :  202 (   0 filtered)
```

10. Энергопотребление схемы в Ваттах (содержимое таблиц XPower Analyzer среды проектирования).

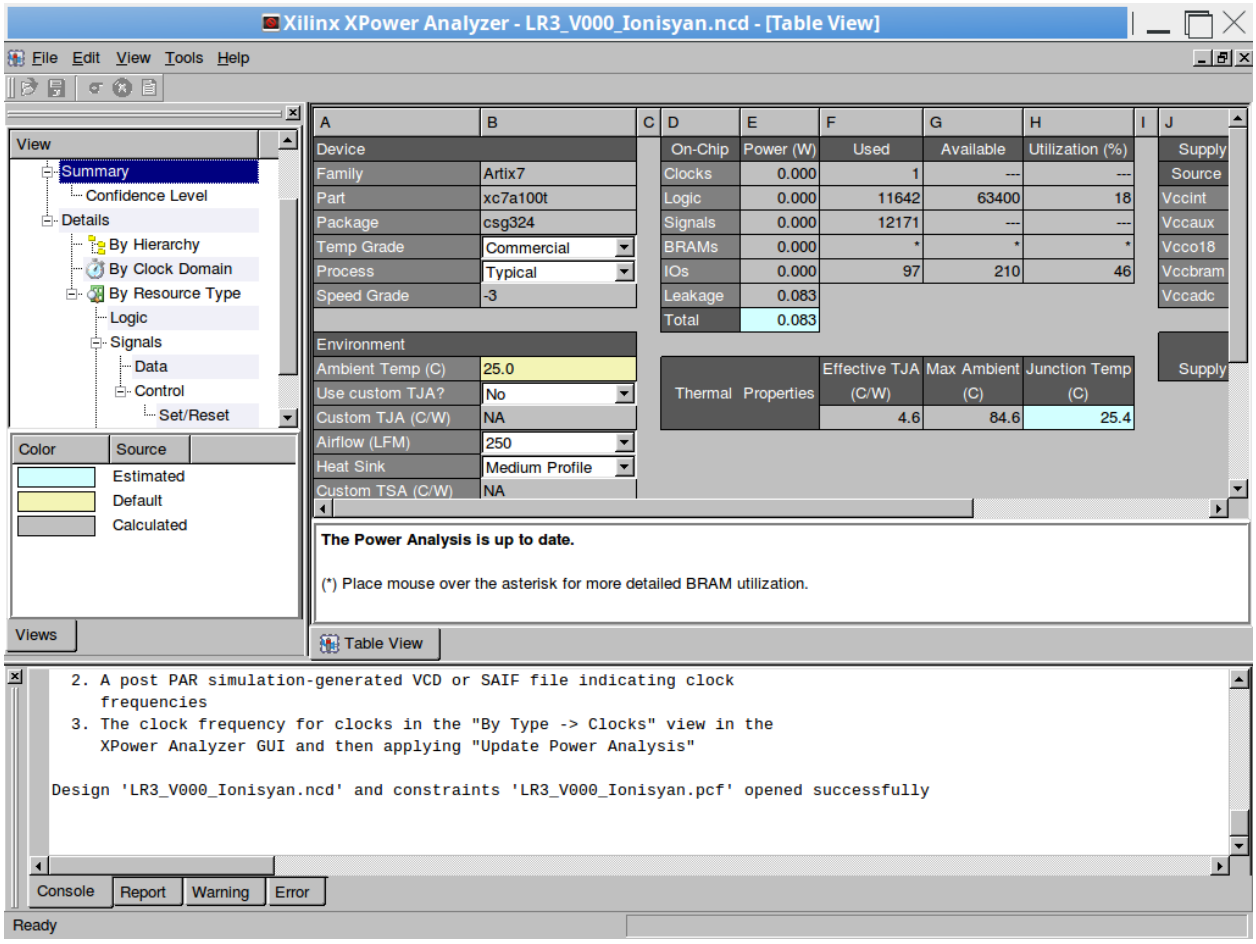
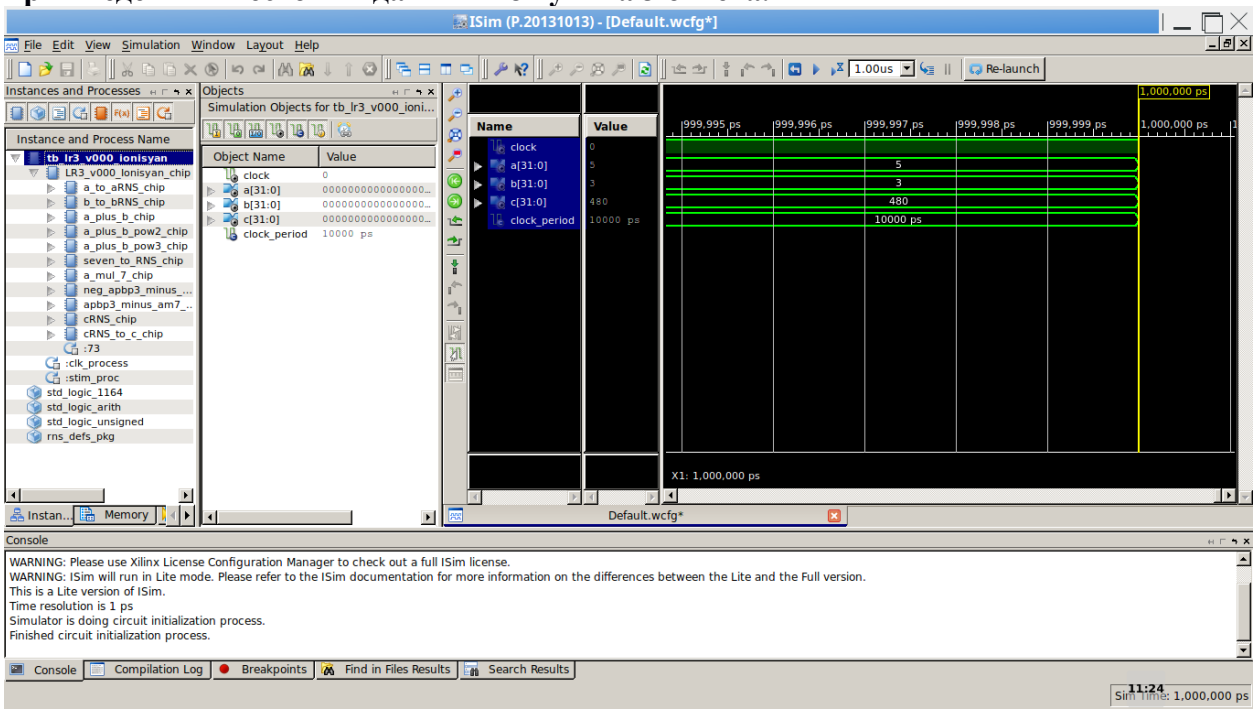


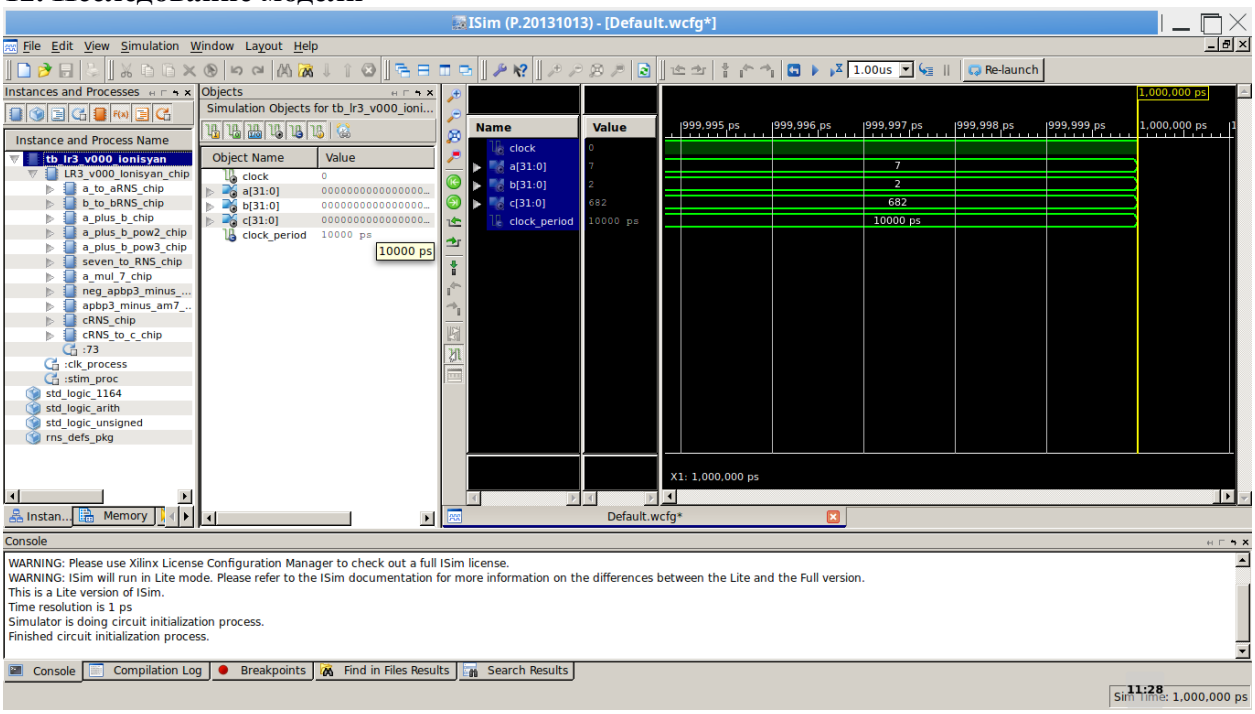
Схема имеет энергопотребление 0.083 Ватта

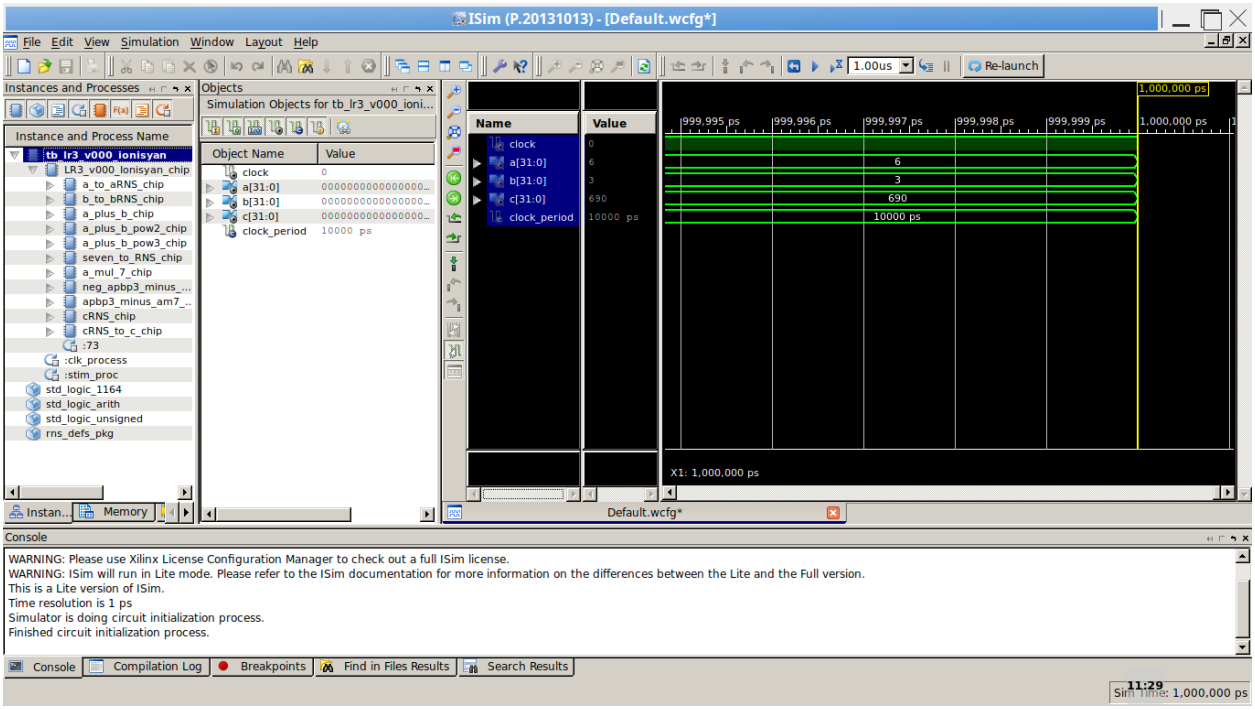
11. Экранный снимок или распечатка результата работы компьютерной программы при введенных тестовых данных из пункта 3 отчета.



Результат совпадает с тестовым решением

12. Исследование модели





13. Выводы о проделанной работе.

Мы разработали и реализовали в среде проектирования СБИС Xilinx ISE 14.7 принципиальную схему устройства рассчитывающую значения арифметической функции, выполняющую все промежуточные расчеты в системе остаточных классов (СОК), синтезировали схему, проверили ее работоспособность на нескольких тестовых наборах входных данных. Схема является экспериментальной и может быть усовершенствована (все компоненты).