

CSC369 Tutorial 1

Some review material
(part 2)

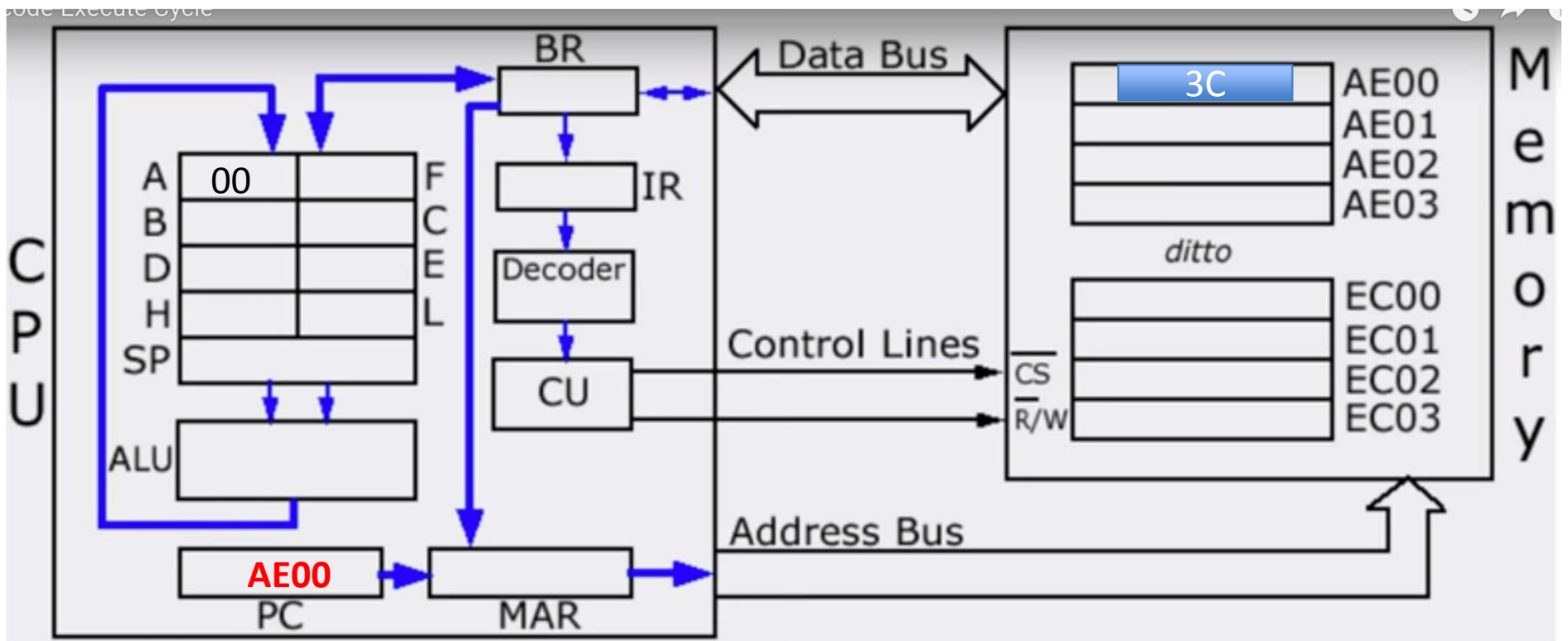
Architecture Review

CPU

- The Program Counter (PC)
- The Stack Pointer (SP)
- Data Registers
- Flow of normal execution
 - Memory address and load/store instructions
- Interrupts!

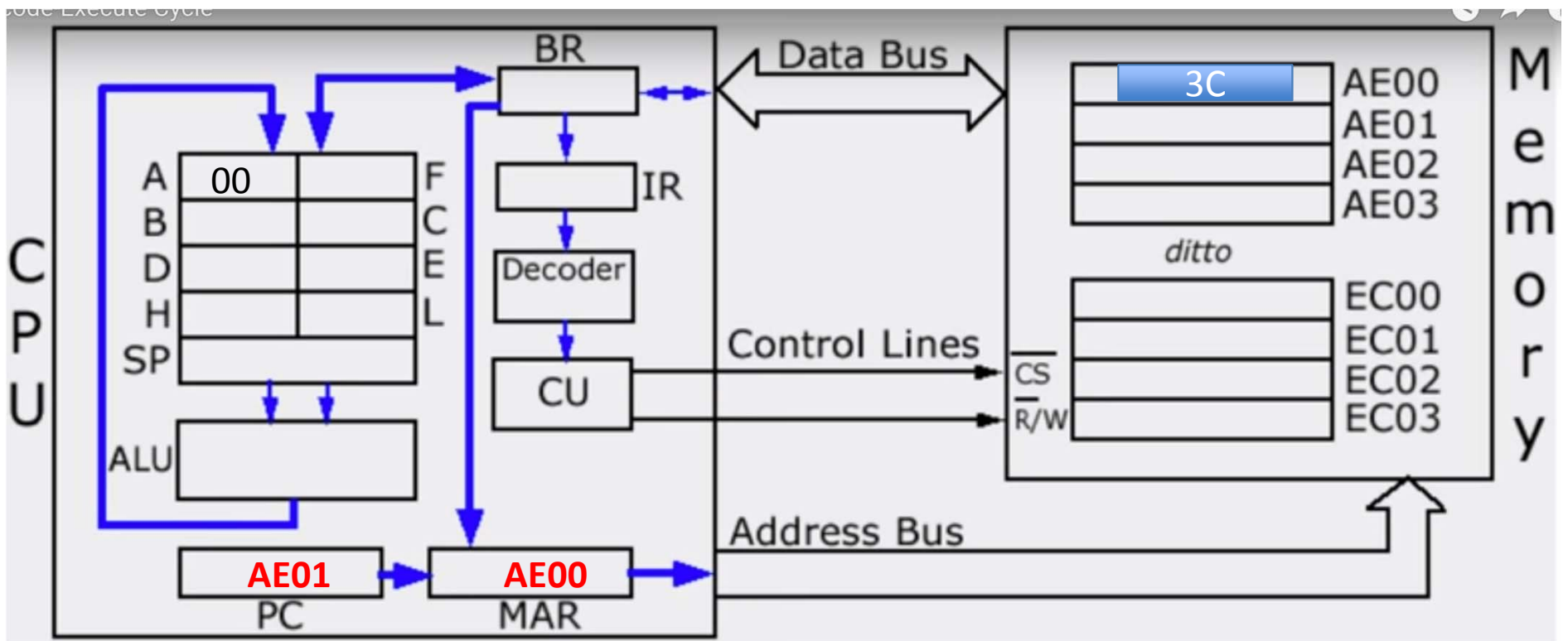
CPU

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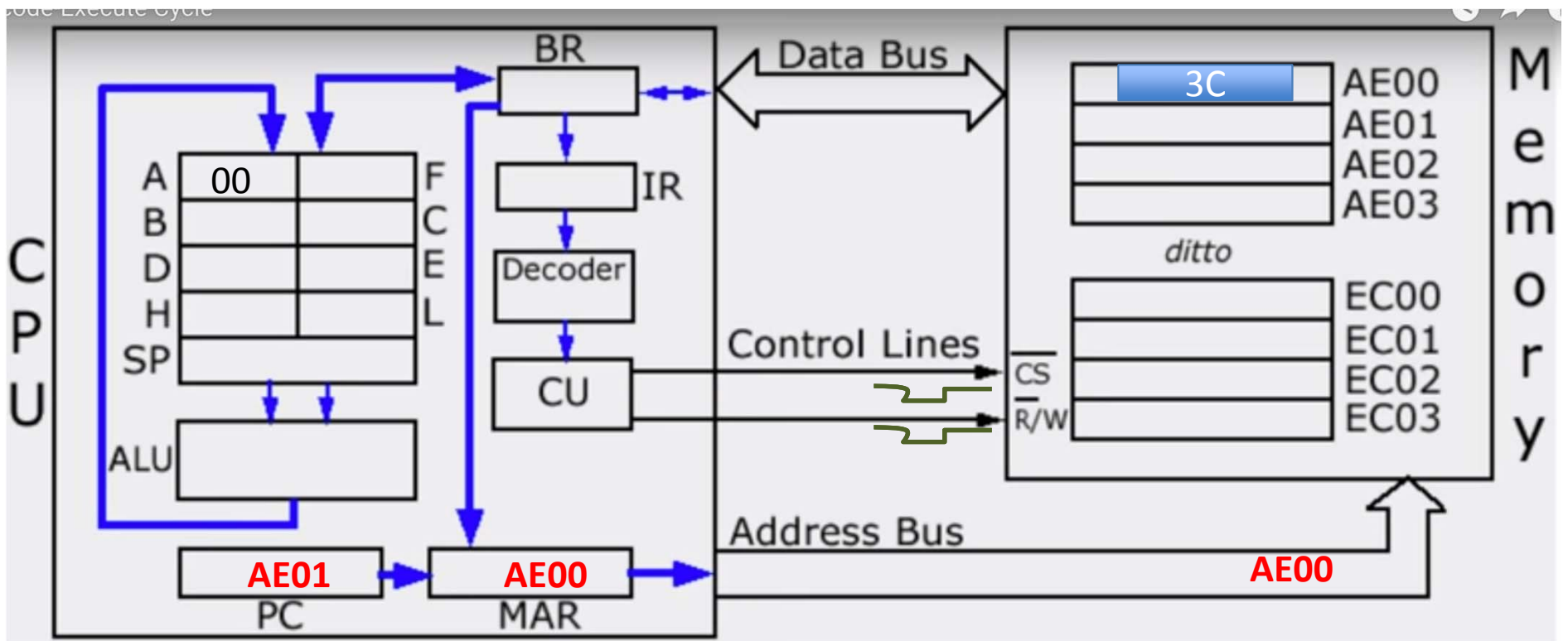
CPU

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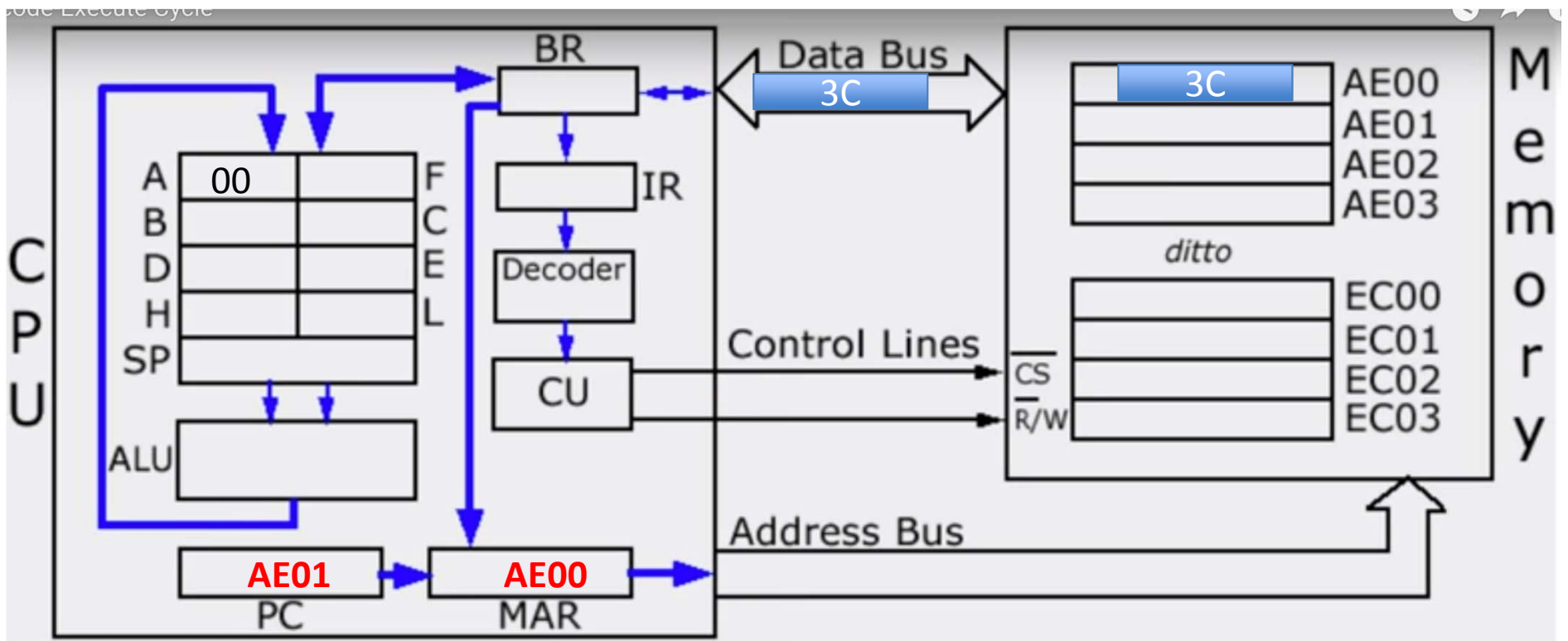
CPU

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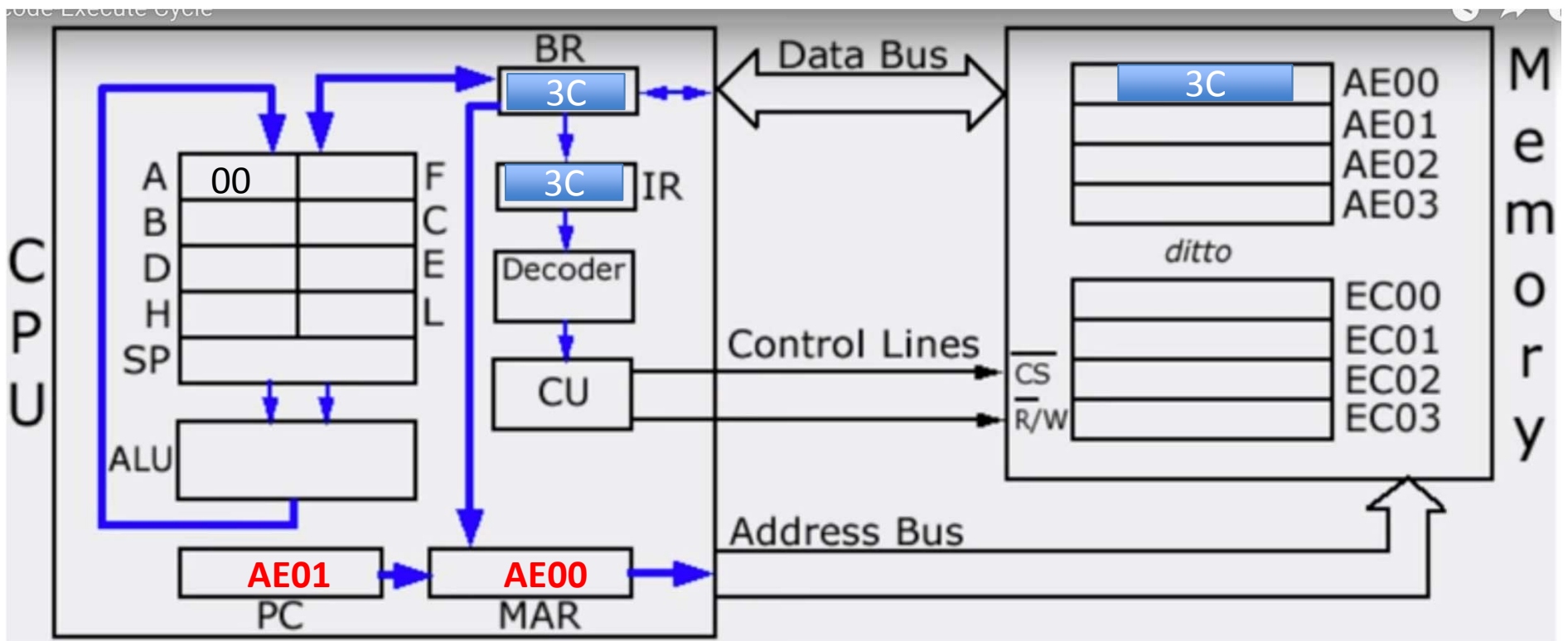
CPU

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CPU

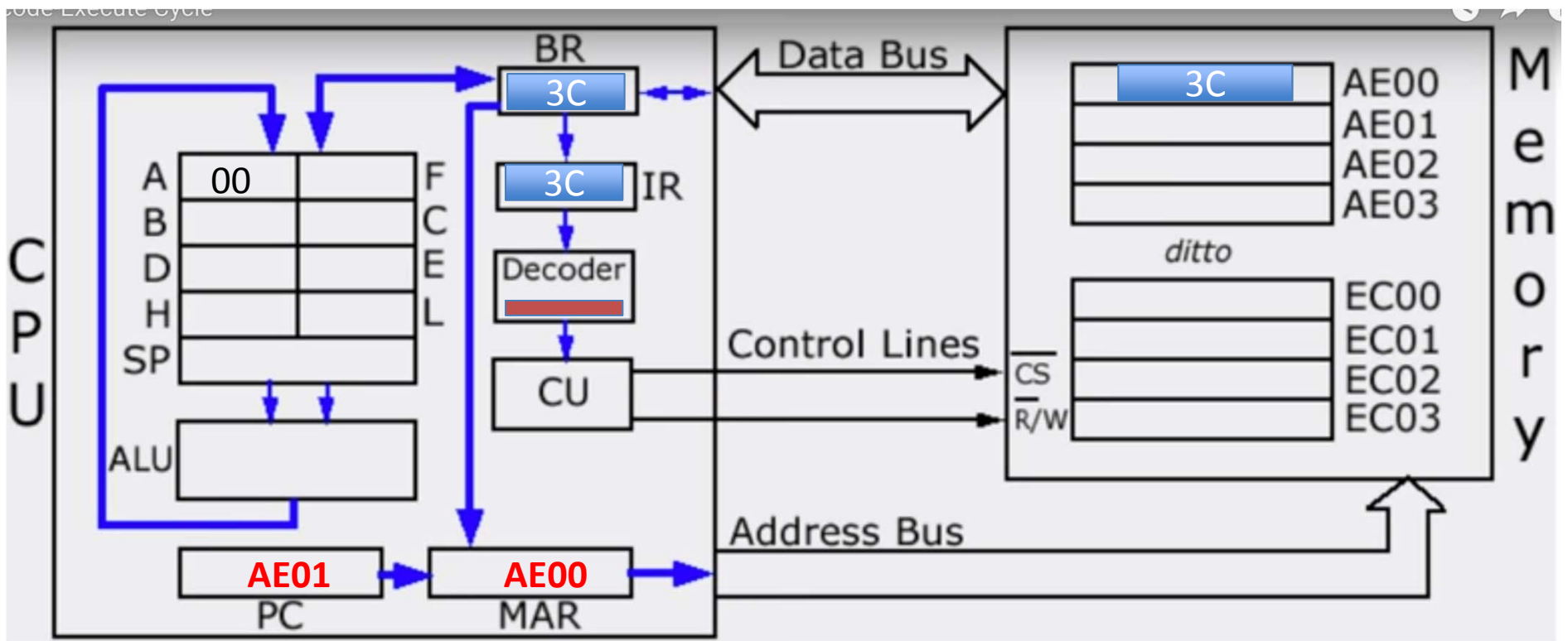
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End of FETCH

CPU

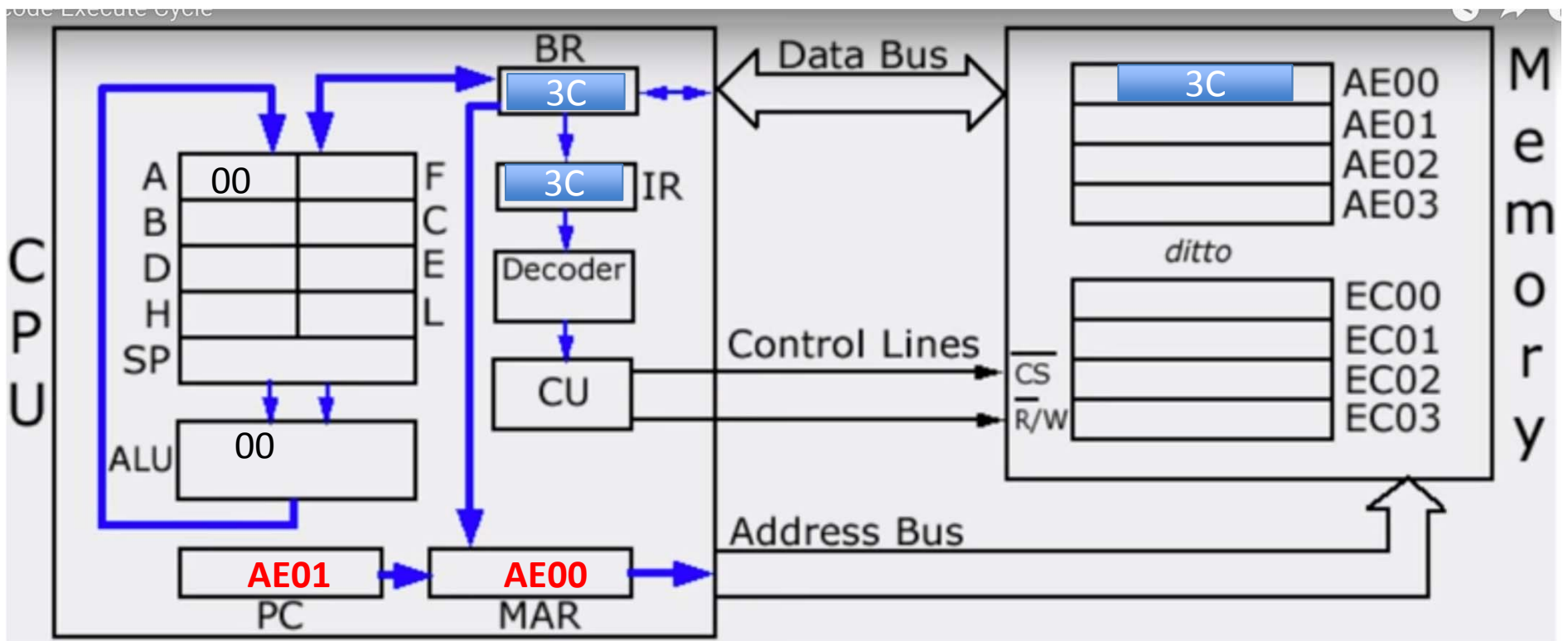
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DECODE

CPU

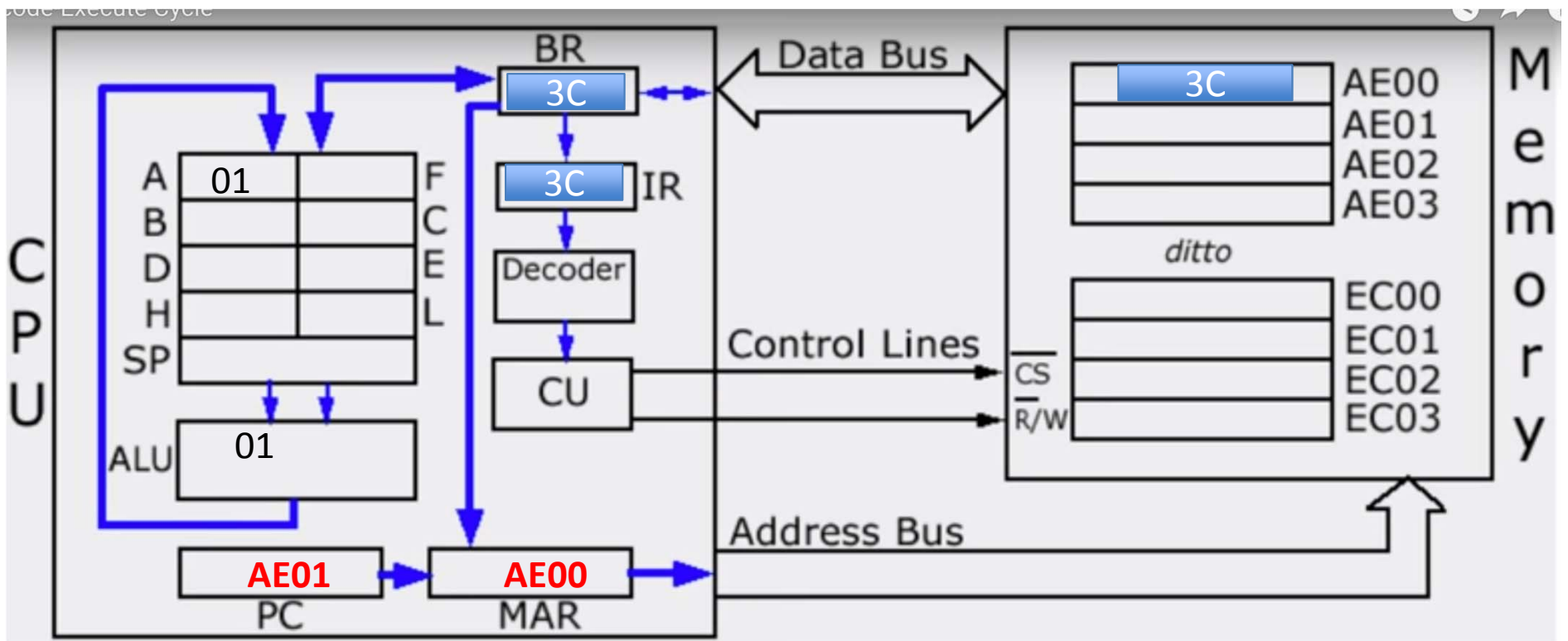
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EXECUTE

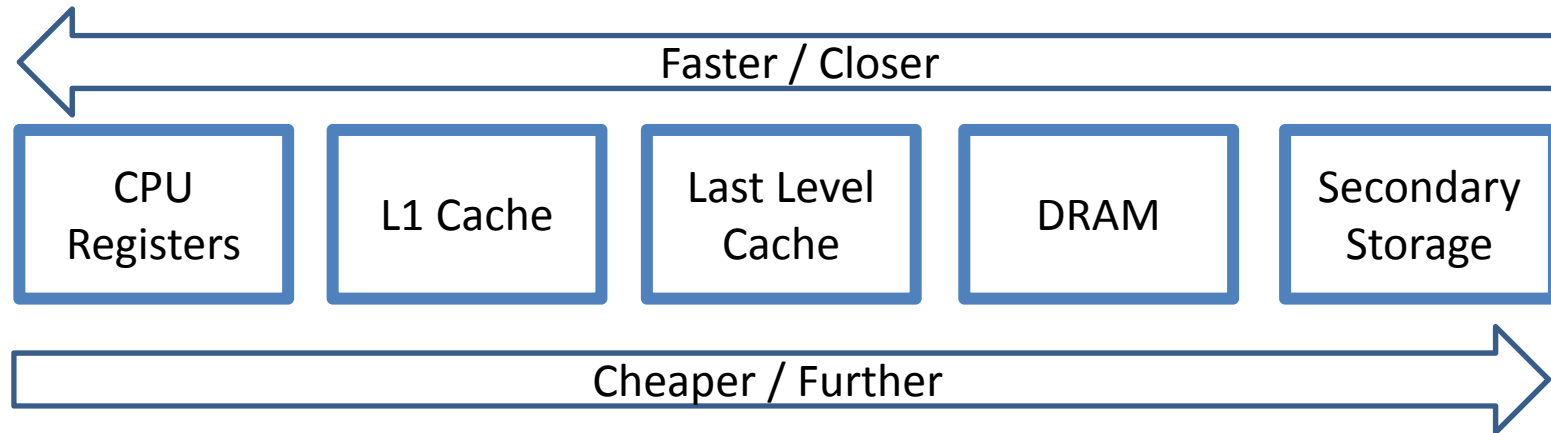
CPU

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EXECUTE

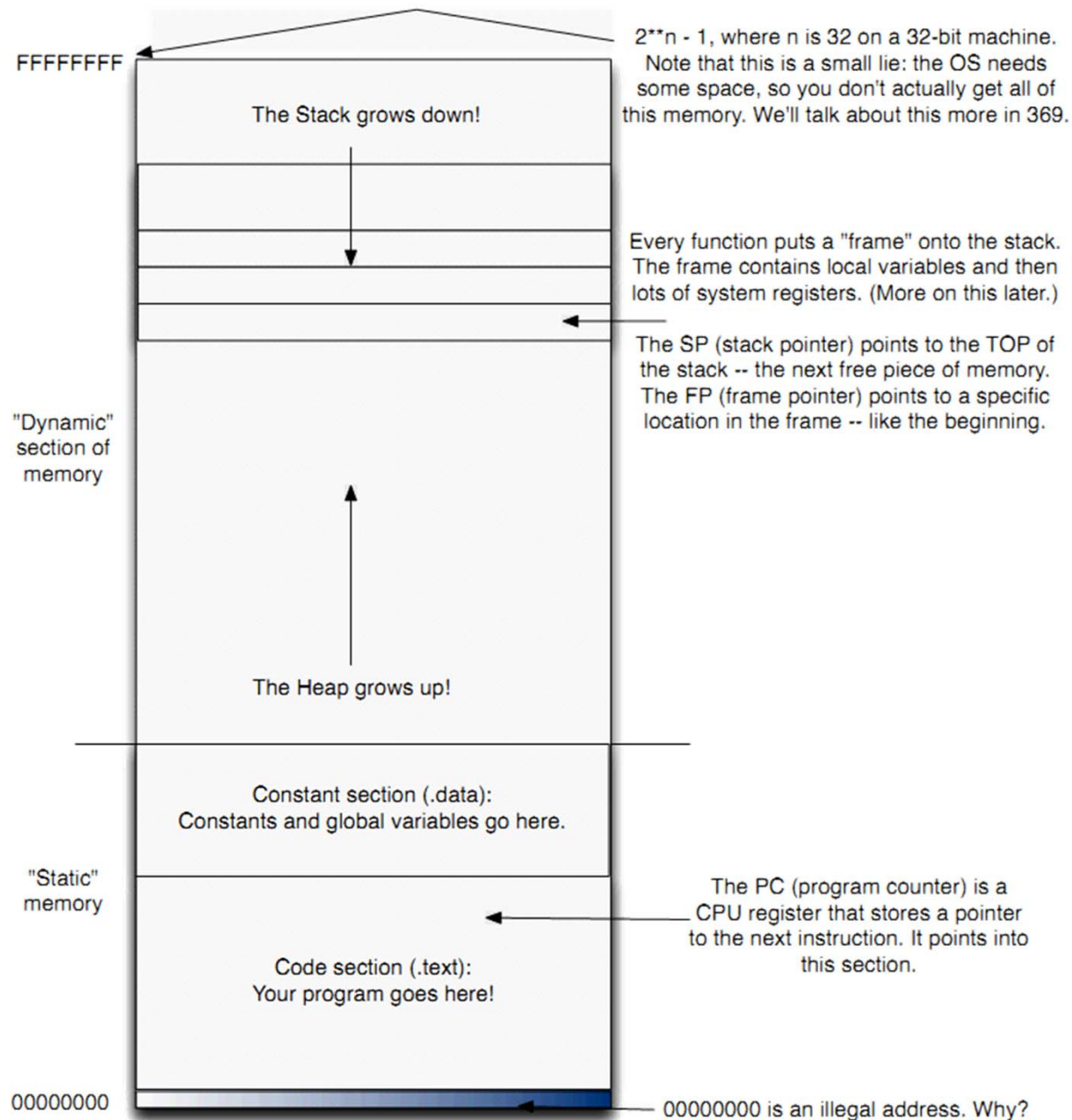
Memory Hierarchy and Trade-off



- Can't have the fastest memory, largest capacity, and be the cheapest...
- OS must do smart things to efficiently use different types of memory (Caching)

Memory

- Program sees linear address space, segmented
 - Code
 - Data
 - Stack
 - Heap
- Where does the OS go?
- Do programs share the same space?



Stack Frame of Function Call

Function 1

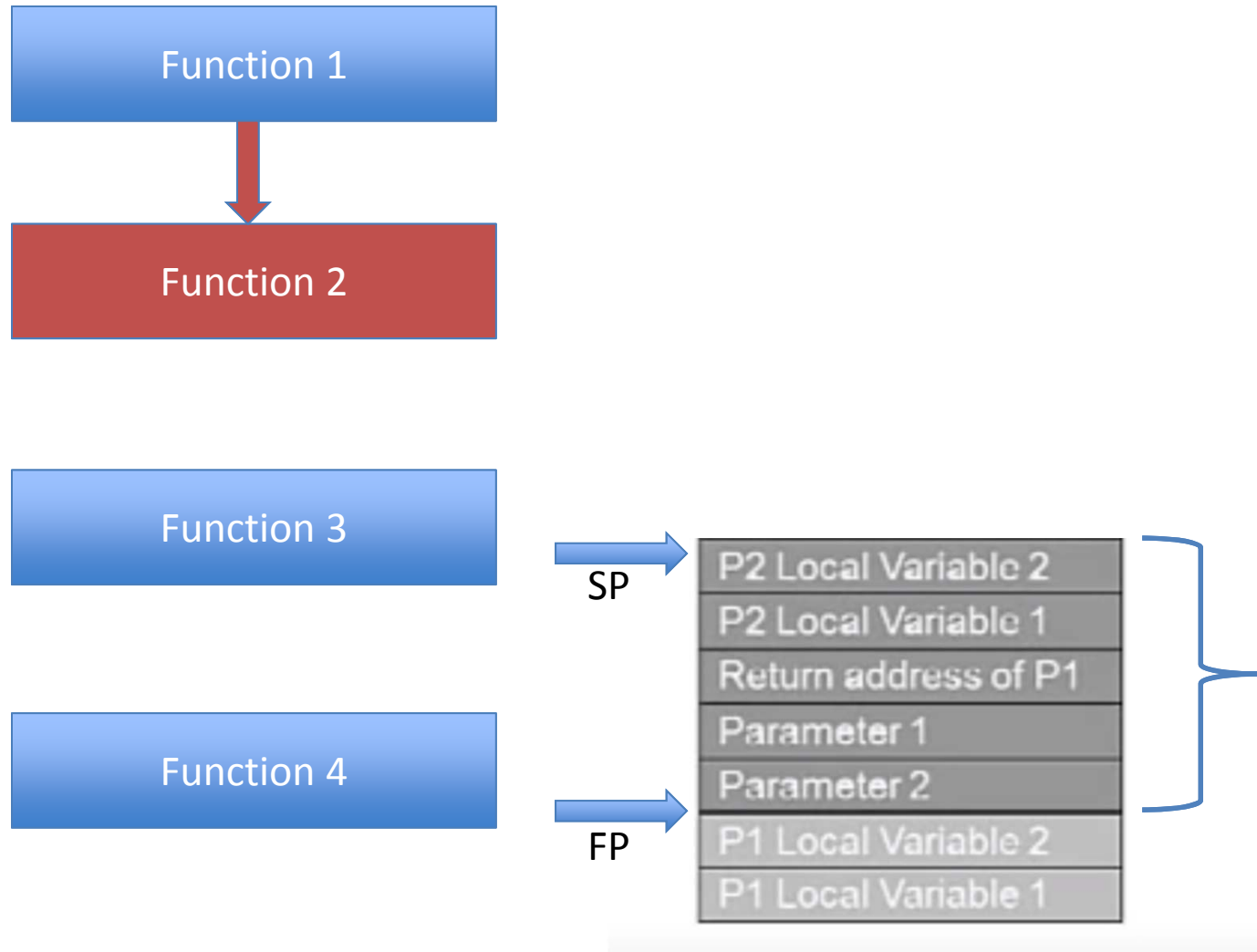
Function 2

Function 3

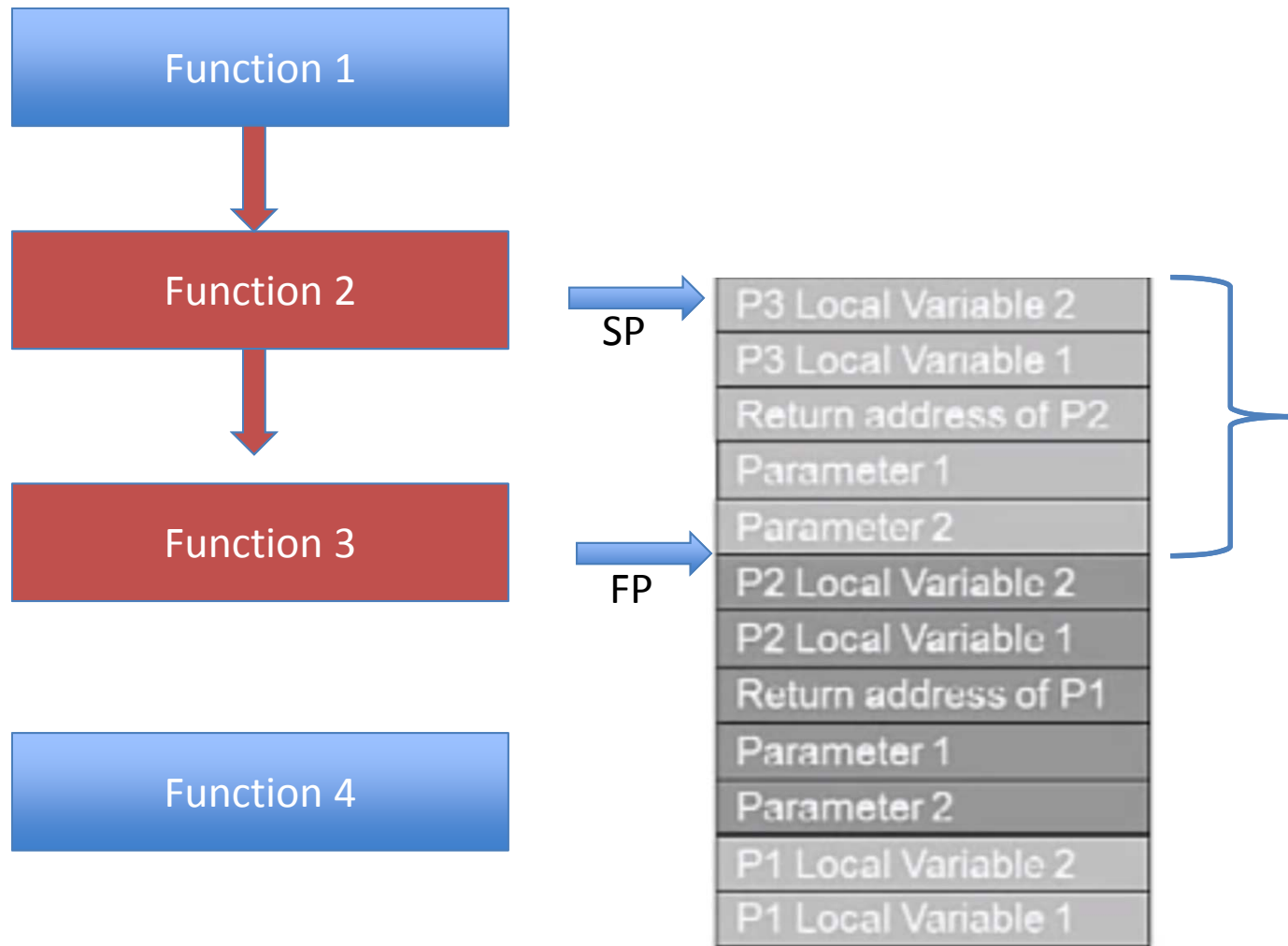
Function 4

P1 Local Variable 2
P1 Local Variable 1

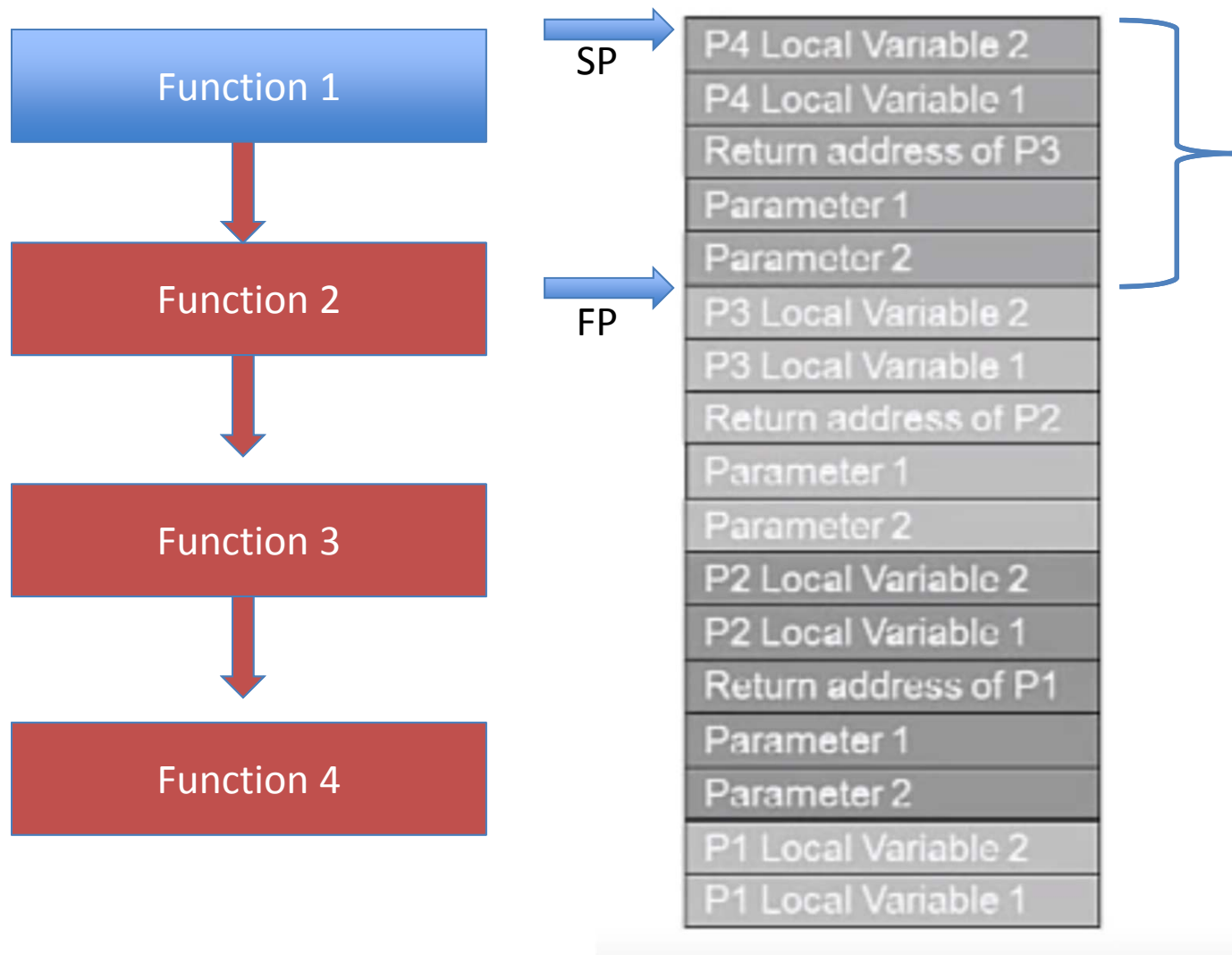
Stack Frame of Function Call



Stack Frame of Function Call

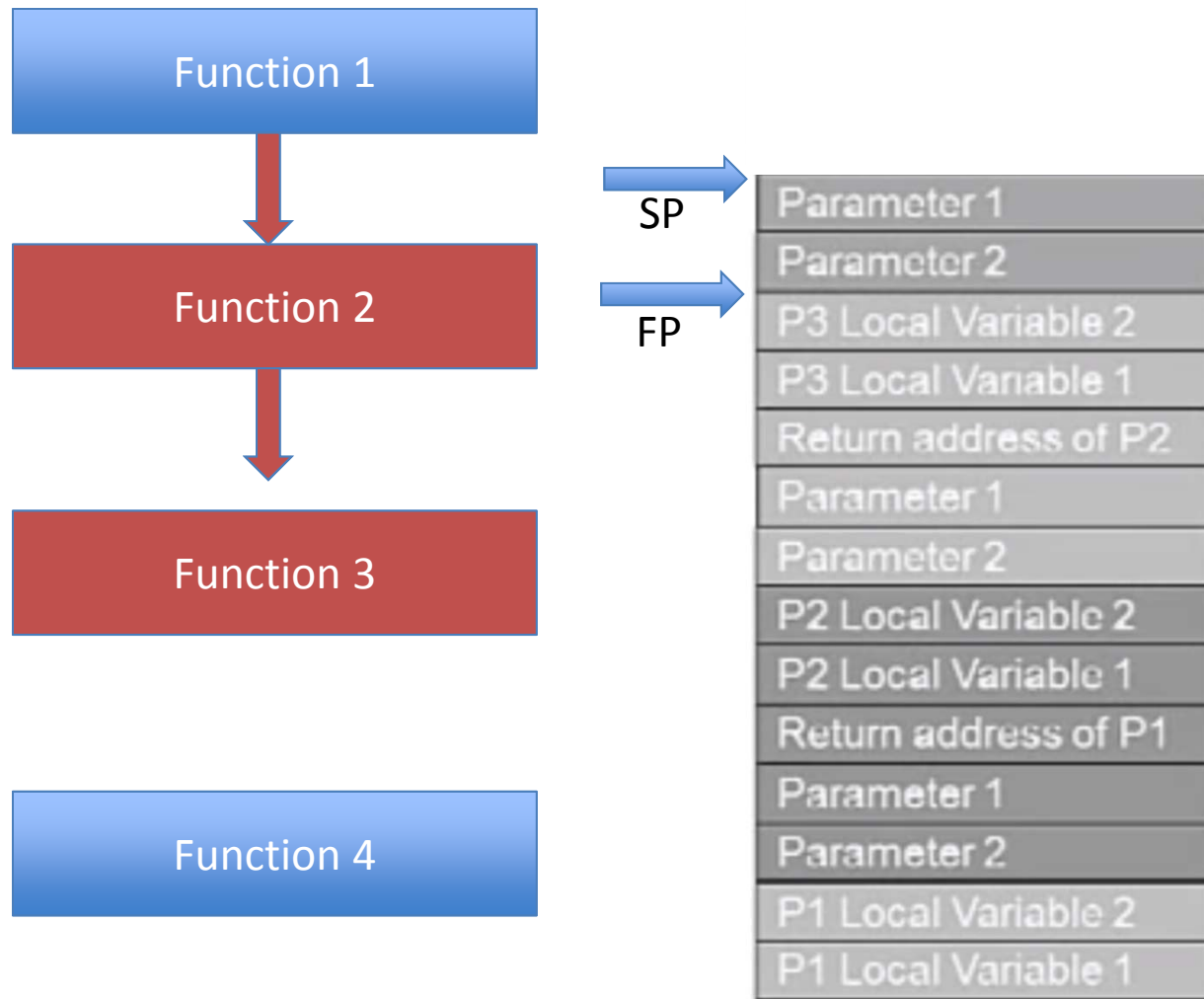


Stack Frame of Function Call



Stack Frame of Function Call

Returning

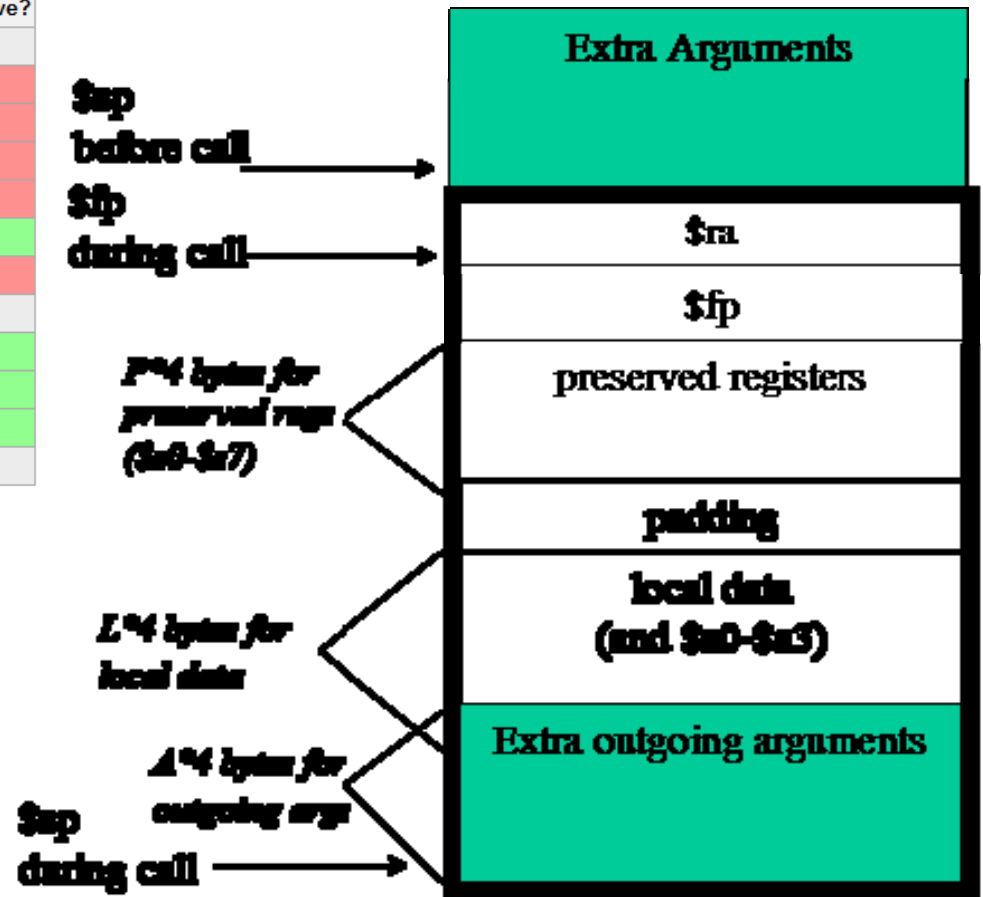


Stack Frames

Registers for O32 Calling Convention

Name	Number	Use	Callee must preserve?
\$zero	\$0	constant 0	N/A
\$at	\$1	assembler temporary	No
\$v0-\$v1	\$2-\$3	values for function returns and expression evaluation	No
\$a0-\$a3	\$4-\$7	function arguments	No
\$t0-\$t7	\$8-\$15	temporaries	No
\$s0-\$s7	\$16-\$23	saved temporaries	Yes
\$t8-\$t9	\$24-\$25	temporaries	No
\$k0-\$k1	\$26-\$27	reserved for OS kernel	N/A
\$gp	\$28	global pointer	Yes
\$sp	\$29	stack pointer	Yes
\$fp	\$30	frame pointer	Yes
\$ra	\$31	return address	N/A

- First 4 arguments: \$a0-\$a3
- Return value (or pointer to it): \$v0
- Return address: \$ra
- Frame pointer: \$fp



<http://www.cs.ucsb.edu/~franklin/30/spim/BookCallConvention.htm>