

SLAS704E - OCTOBER 2012 - REVISED MARCH 2015

4 Terminal Configuration and Functions

4.1 Pin Diagram - RGZ Package - MSP430FR596x and MSP430FR596x1

Figure 4-1 shows the 48-pin RGZ package. P2.3/TA0.0/UCA1STE/A6/C10 P2.4/TA1.0/UCA1CLK/A7/C11 PJ.7/HFXOUT ENU PJ.5/LFXOU PJ.4/LFXIN PJ.6/HFXIN AVCC AVSS AVSS AVSS Laurchpood LED 2 (year) 1.0/TAO.1/DMAEO/RTCCLK/AO/CO/VREF-/VeREF-P1.1/TA0.2/TA1CLK/COUT/A1/C1/VREF+/VeREF+ P4.6 - EMh wadens input P4:4/TB0.5 P1.7/TB0.4/UCB0SOMI/UCB0SCL/TA1.0 P3/2/A14/C14 P1.6/TB0.3/UCB0SIMO/UCB0SDA/TA0.0 P3/3/A15/C15 30 P4X 294 P3.6/TB0.5 P1.3 TA1.2/UCB0STE/A3/C3 P3.5/TB0.4/COUT 🐸 P1.4 TB0.1 UCA0STE/A4/C4 P3.4/TB0.3/SMCLK PWK P1.5 TB0.2 UCA0CLK/A5/C5 26 P2.2/TB0.2/UCB0CLK PJ.0/TDO/TB0OUTH/SMCLK/SRSCG1/C6 P2.1/TB0.0 UCAORXD/UCAOSOM/TBO 18 19 20 21 PJ.2/TMS/ACLK/SROSCOFF/C8 PJ.1/TDI/TCLK/MCLK/SRSCG0/C7 P2.5/TB0.0/UCA1TXD/UCA1SIMO TEST/SBWTCK, P2.6/TB0.1/UCA1RXD/UCA1SOM RST/NMI/SBWTDIO P2.0/TB0.6/UCA0TXD/UCA0SIMO/TB0CLK/ACLK NOTE: QFN package pad connection to V_{SS} recommended. On devices with UART BSL: P2.0: BSLTX; P2.1: BSLRX On devices with I²C BSL: P1.6: BSLSDA; P1.7: BSLSCL

Figure 4-1. 48-Pin RGZ Package (Top View) - MSP430FR596x and MSP430FR596x1