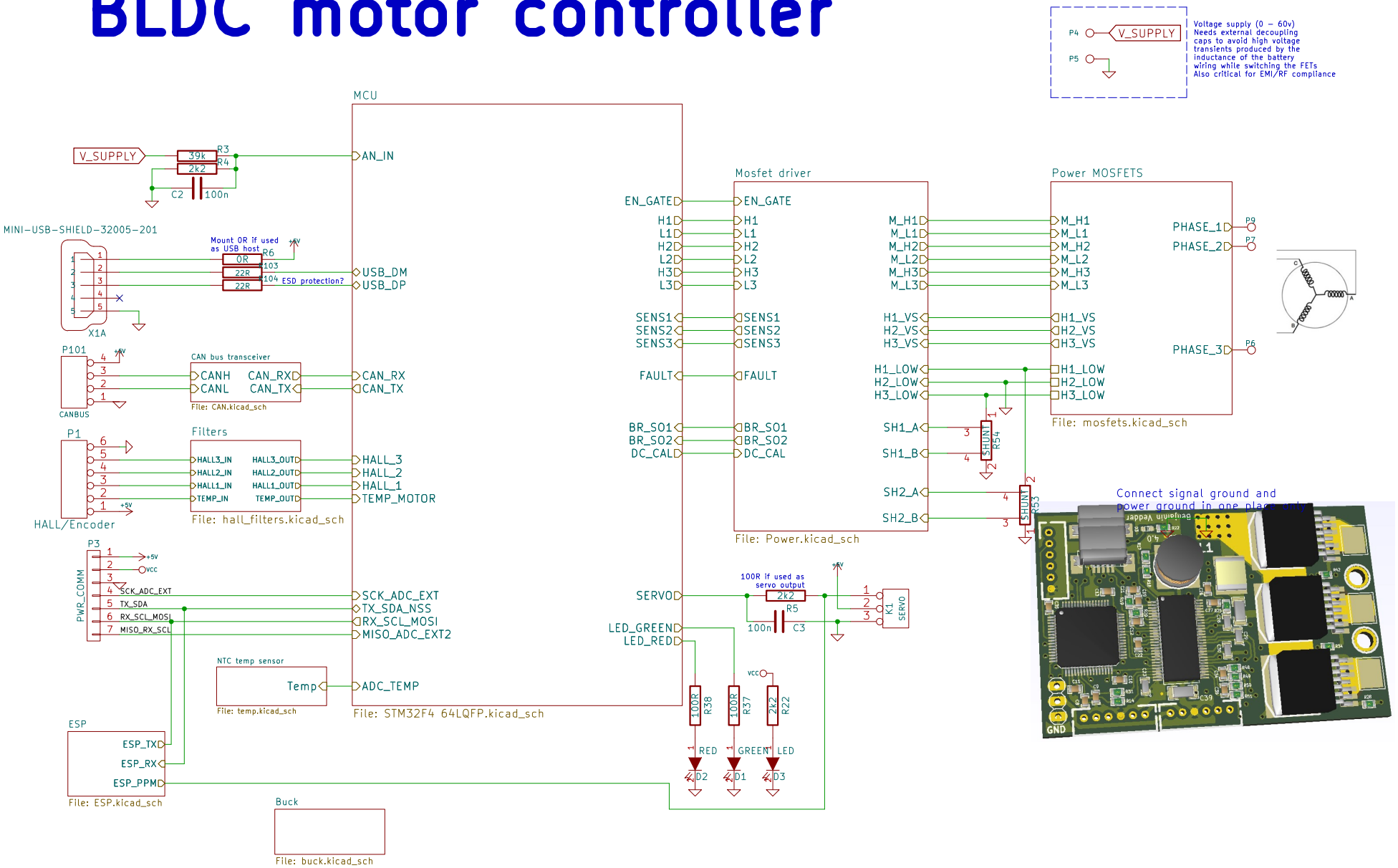
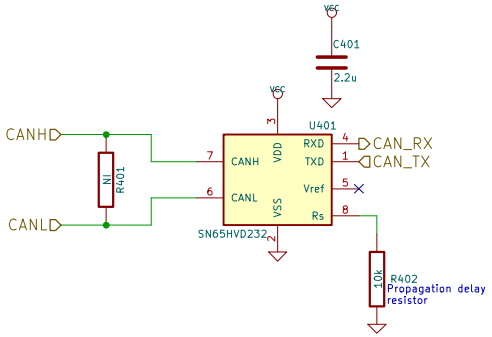
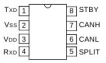
BLDC motor controller



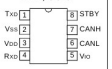


Package Types

MCP2561
PDIP, SOIC



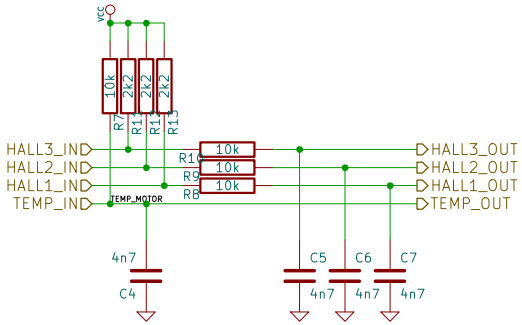
MCP2562
PDIP, SOIC

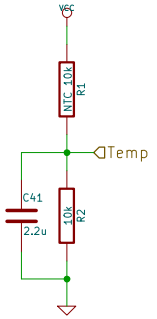


MCP2561
3x3 DFN*

MCP2562
3x3 DFN*

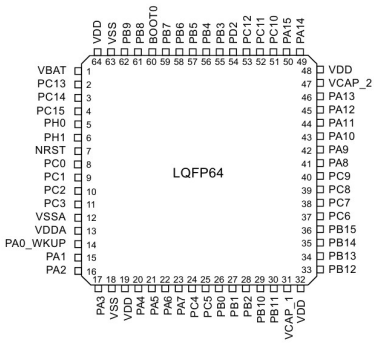
* Includes Exposed Thermal Pad (EP); see Table 1-2.

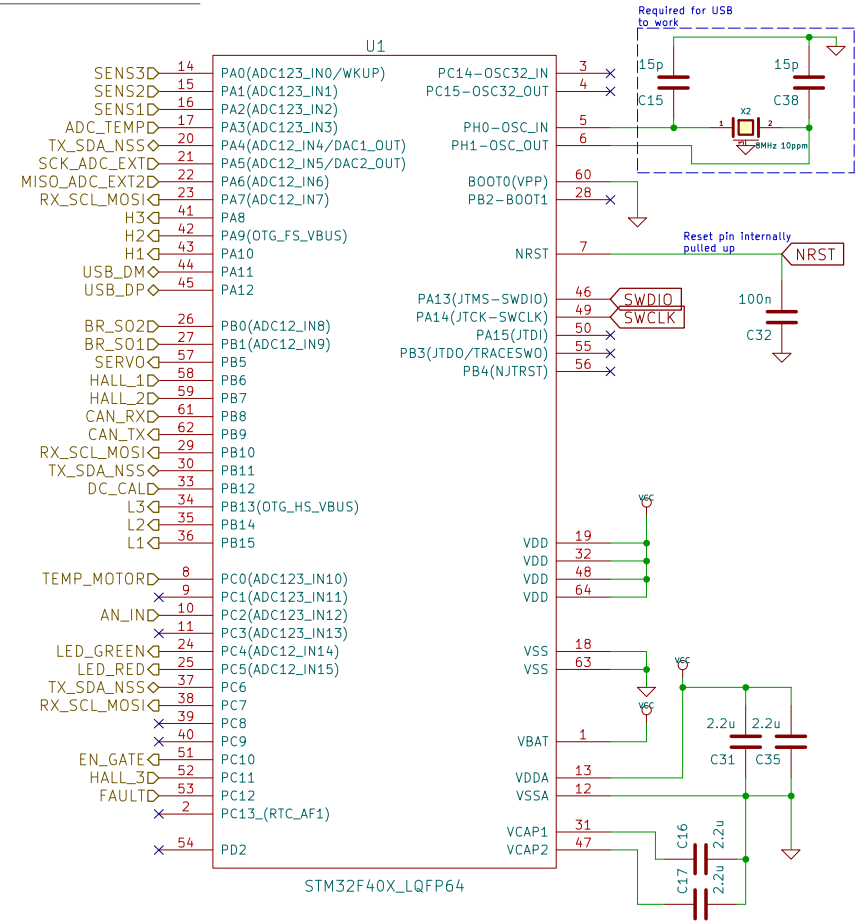

vcc
10k
2k2
2k2
2k2
R7
R12
R13
R14
HALL3_IN
HALL2_IN
HALL1_IN
TEMP_IN
10k
10k
10k
R10
R9
R8
HALL3_OUT
HALL2_OUT
HALL1_OUT
TEMP_OUT
TEMP_MOTOR
4n7
C4
C5
C6
C7
4n7
4n7
4n7

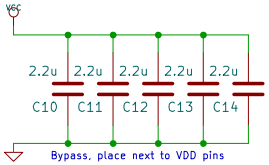

VCC
NTC_10k
R1
Temp
C41
2.2u
10k
R2

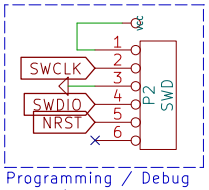
STM32F405xx
STM32F407xx

ARM Cortex-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera



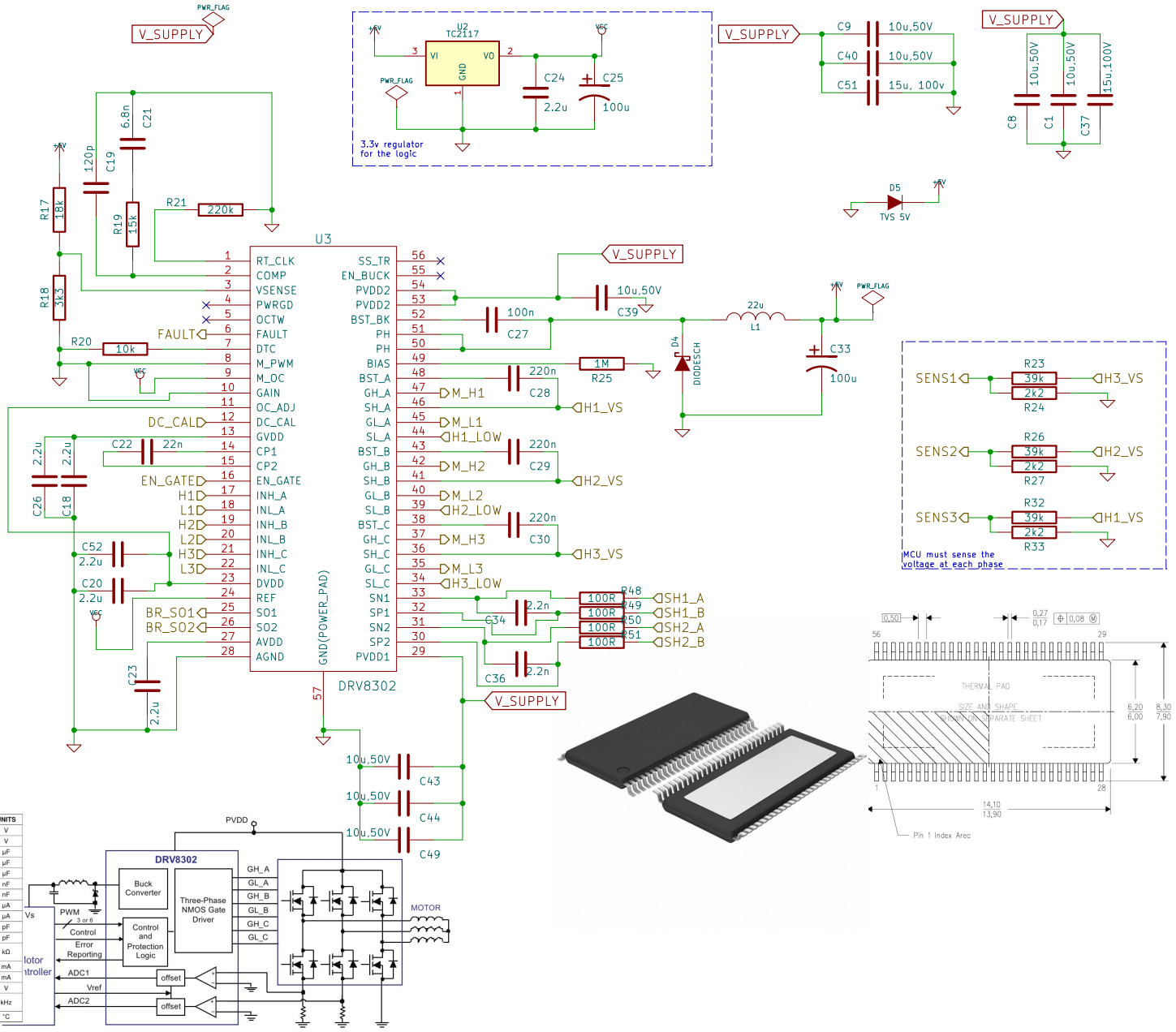






FEATURES

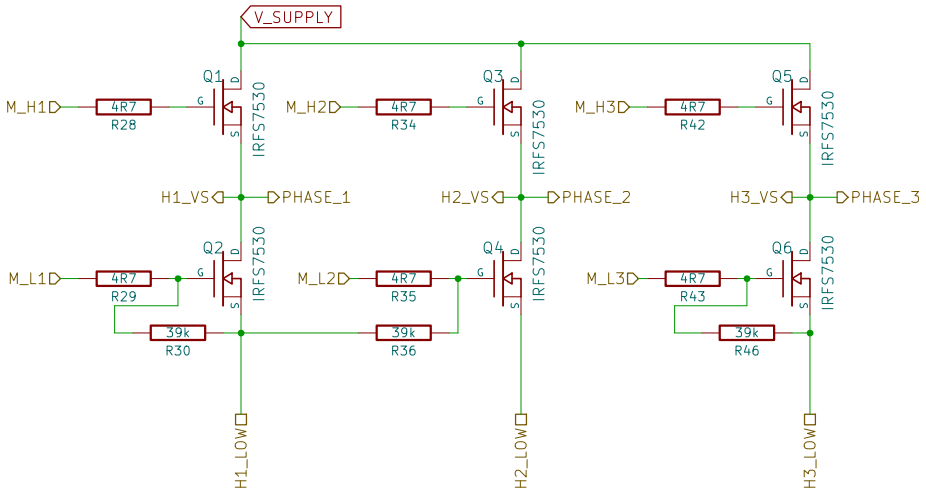
- Operating Supply Voltage 8V–60V
- 2.3A Sink and 1.7A Source Gate Drive Current Capability
- Integrated Dual Shunt Current Amplifiers With Adjustable Gain and Offset
- Integrated Buck Converter to Support up to 1.5A External Load
- Independent Control of 3 or 6 PWM Inputs
- Bootstrap Gate Driver With 100% Duty Cycle Support
- Programmable Dead Time to Protect External FETs from Shoot Through
- Programmable Overcurrent Protection of External MOSFETs
- Thermally Enhanced 56-Pin TSSOP Pad Down DCA Package

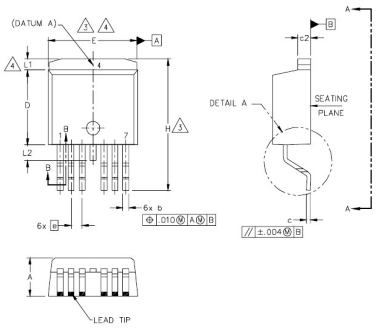


RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNITS
PVDD1	DC supply voltage PVDD1 for normal operation	Relative to PGND	8		60	V
PVDD2	DC supply voltage PVDD2 for buck converter		3.5		60	V
C_{AVDD}	External capacitance on AVDD pin (ceramic cap) 20% tolerance			1		µF
C_{DVDD}	External capacitance on DVDD pin (ceramic cap) 20% tolerance			1		µF
C_{GVDD}	External capacitance on GVDD pin (ceramic cap) 20% tolerance			2.2		µF
C_{CP}	Flying cap on charge pump pins (between CP1 and CP2) (ceramic cap) 20% tolerance			22		nF
C_{BST}	Bootstrap cap (ceramic cap)			100		nF
I_{DIN_EN}	Input current of digital pins when EN_GATE is high				100	µA
I_{DIN_DIS}	Input current of digital pins when EN_GATE is low				1	µA
C_{DIN}	Maximum capacitance on digital input pin				10	pF
C_{O_OPA}	Maximum output capacitance on outputs of shunt amplifier				20	pF
R_{DTC}	Dead time control resistor range. Time range is 50ns (-GND) to 500ns (150kΩ) with a linear approximation.		0		150	kΩ
I_{FAULT}	FAULT pin sink current. Open-drain	V = 0.4 V			2	mA
I_{OCTW}	OCTW pin sink current. Open-drain	V = 0.4 V			2	mA
V_{REF}	External voltage reference voltage for current shunt amplifiers		2		6	V
f_{gate}	Operating switching frequency of gate driver	Qg(TOT) = 25 nC or total 30 mA gate drive average current			200	kHz
T_A	Ambient temperature		–40		125	°C

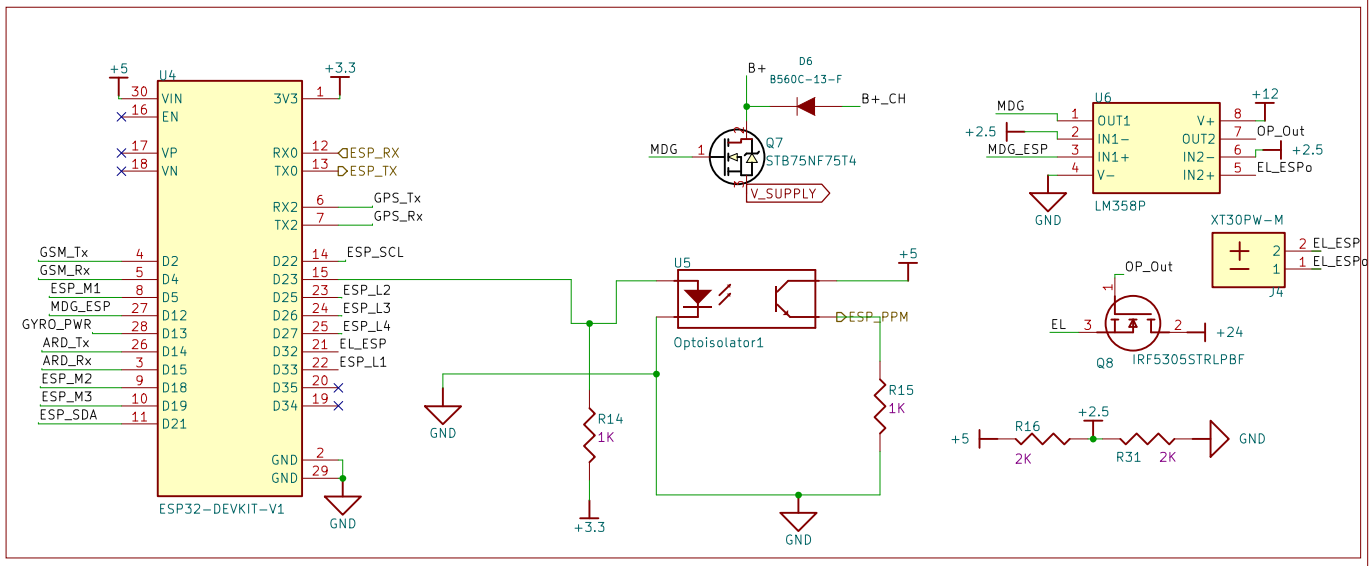
Figure 1. DRV8302 Simplified Application Schematic


V_SUPPLY
Q1
Q3
Q5
M_H1
M_H2
M_H3
4R7
R28
R34
R42
IRFS7530
H1_VS
H2_VS
H3_VS
PHASE_1
PHASE_2
PHASE_3
Q2
Q4
Q6
M_L1
M_L2
M_L3
R29
R35
R43
39k
R30
R36
R46
H1_LOW
H2_LOW
H3_LOW

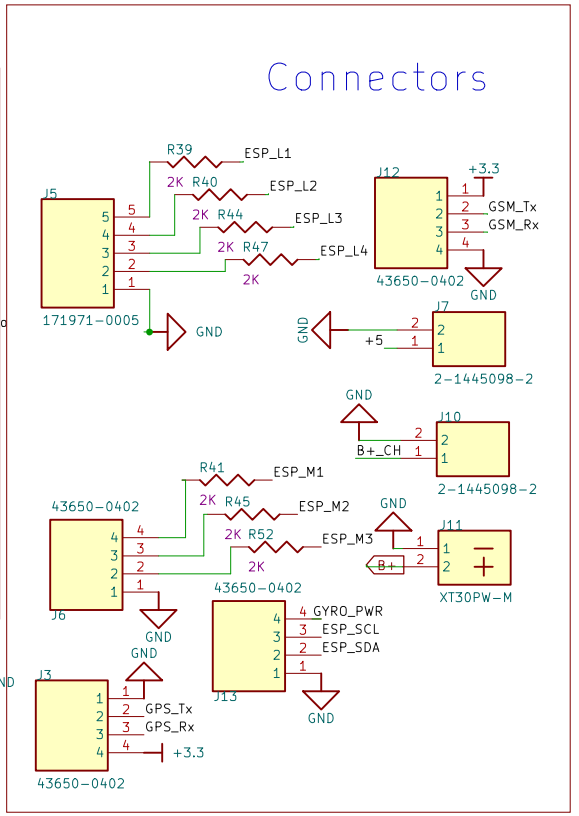

(DATUM A)
DETAIL A
SEATING PLANE
LEAD TIP

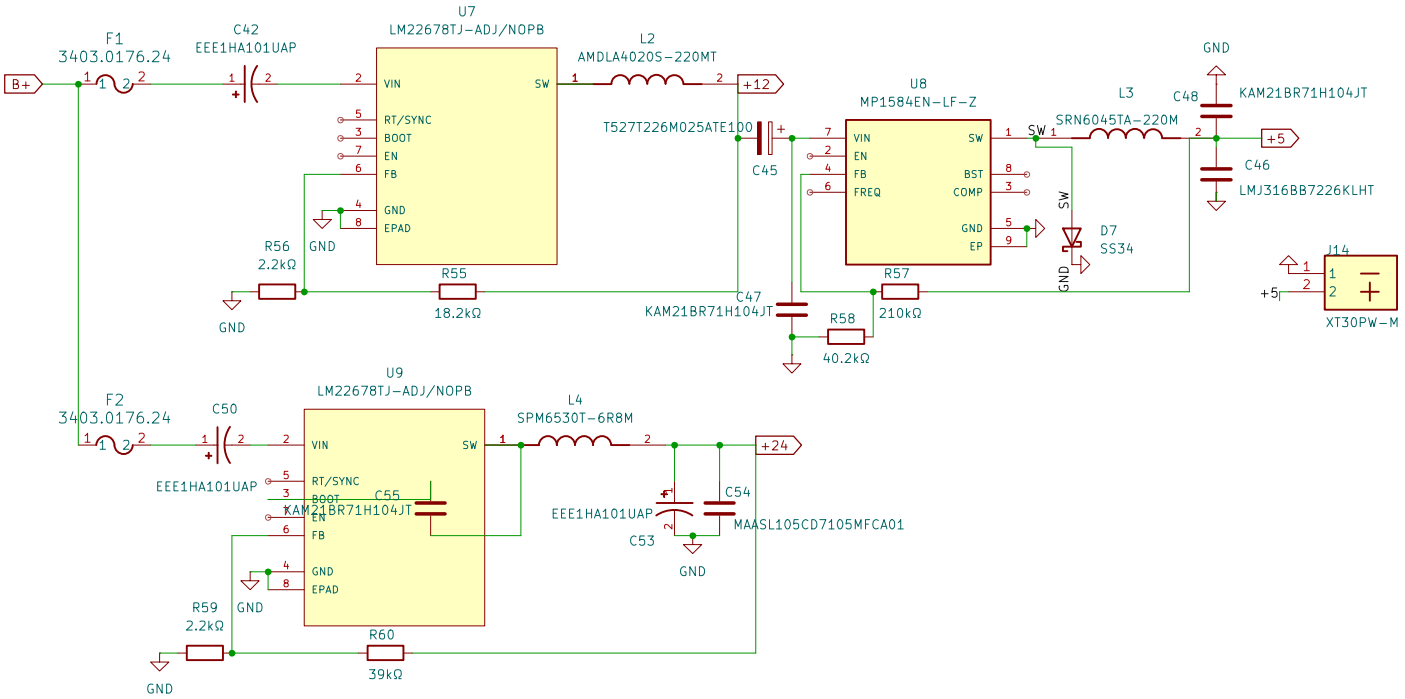
Current Design

BD139 IRFZ44 BD140(PNP)



Connectors




B+
F1
3403.0176.24
C42
EEE1HA101UAP
U7
LM22678TJ-ADJ/NOPB
VIN
SW
RT/SYNC
BOOT
EN
FB
GND
EPAD
L2
AMDLA4020S-220MT
+12
T527T226M025ATE100
C45
R56
2.2kΩ
R55
18.2kΩ
U8
MP1584EN-LF-Z
VIN
EN
FB
FREQ
SW
BST
COMP
GND
EP
L3
SRN6045TA-220M
C48
KAM21BR71H104JT
C46
LMJ316BB7226KLHT
+5
D7
SS34
J14
XT30PW-M
C47
KAM21BR71H104JT
R57
210kΩ
R58
40.2kΩ
F2
3403.0176.24
C50
EEE1HA101UAP
U9
LM22678TJ-ADJ/NOPB
C55
KAM21BR71H104JT
L4
SPM6530T-6R8M
+24
C53
EEE1HA101UAP
C54
MAASL105CD7105MFCA01
R59
2.2kΩ
R60
39kΩ