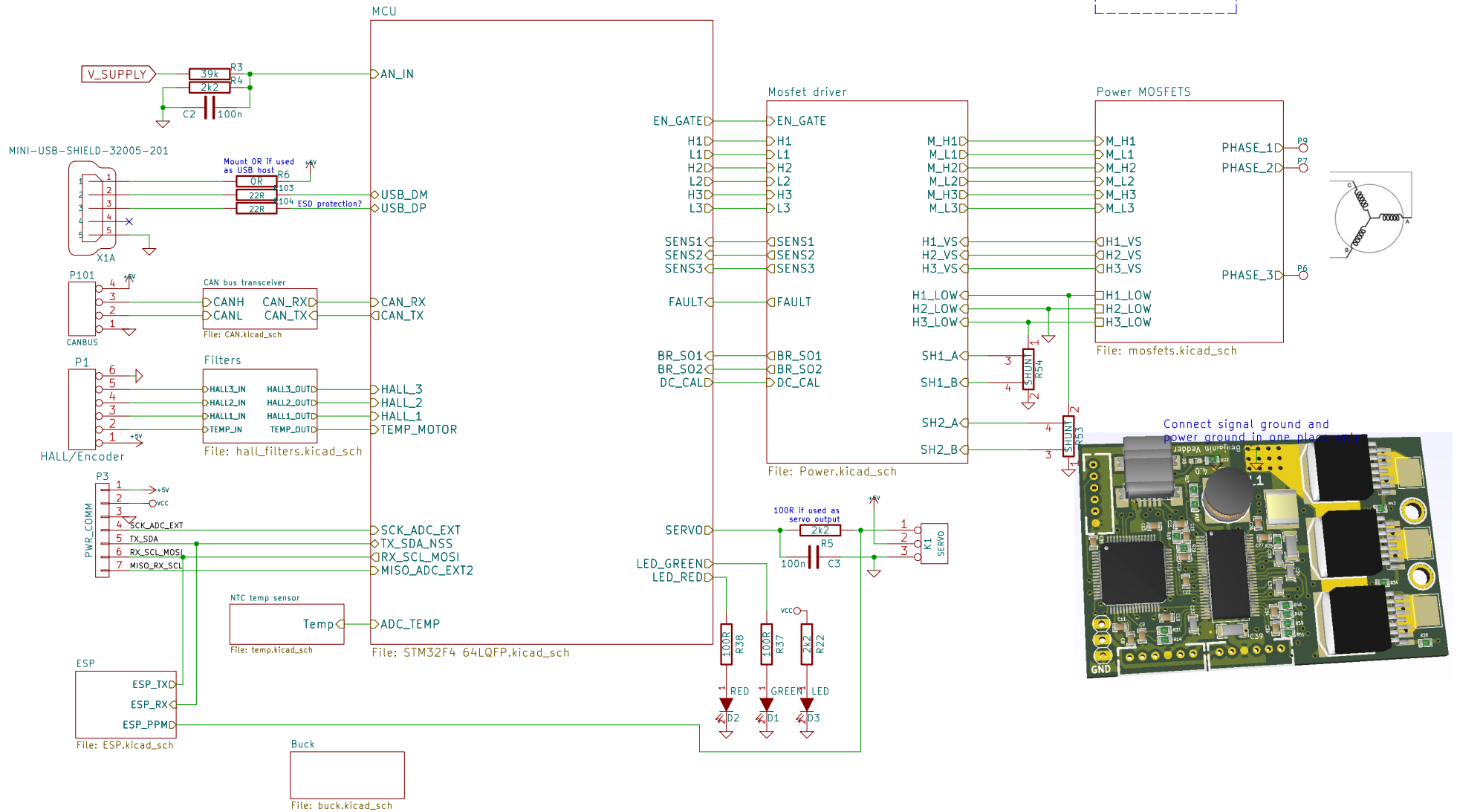
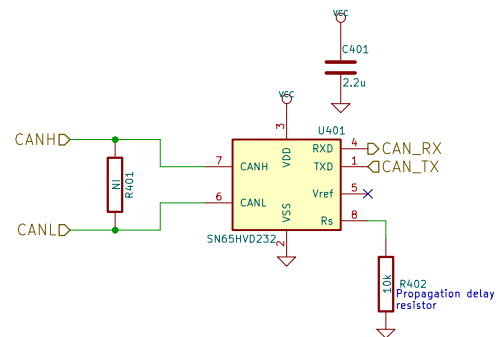


BLDC motor controller

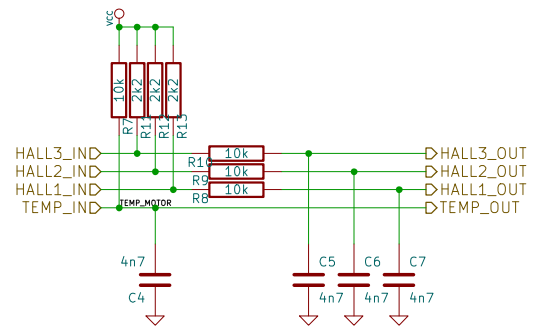


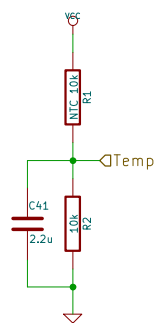


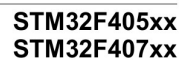
Package Types

MCP2561 PDIP, SOIC		MCP2562 PDIP, SOIC	
Txd [1]	8] STBY	Txd [1]	8] STBY
Vss [2]	7] CANH	Vss [2]	7] CANH
Vdd [3]	6] CANL	Vdd [3]	6] CANL
Rxd [4]	5] SPLIT	Rxd [4]	5] Vio
MCP2561 3x3 DFN*		MCP2562 3x3 DFN*	
Txd [1]	8] STBY	Txd [1]	8] STBY
Vss [2]	7] CANH	Vss [2]	7] CANH
Vdd [3]	6] CANL	Vdd [3]	6] CANL
Rxd [4]	5] SPLIT	Rxd [4]	5] Vio

* Includes Exposed Thermal Pad (EP); see [Table 1-2](#).



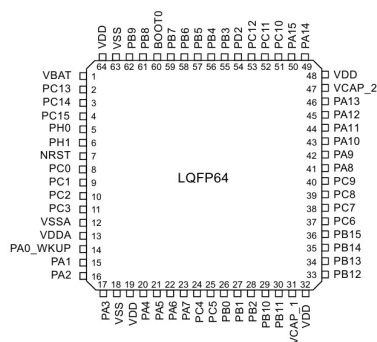
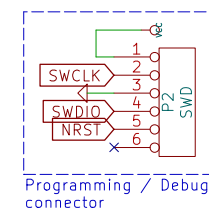




The schematic diagram illustrates the pin connections for the STM32F40X-LQFP64 microcontroller. The pins are organized into two columns, with the left column showing the pin number and the right column showing the pin name and its function. The connections are as follows:

- Pin 14:** SENS3D to PA0 (ADC123_IN0/WKUP)
- Pin 15:** SENS2D to PA1 (ADC123_IN1)
- Pin 16:** SENS1D to PA2 (ADC123_IN2)
- Pin 17:** ADC_TEMP to PA3 (ADC123_IN3)
- Pin 20:** TX_SDA_NSS to PA4 (ADC12_IN4/DAC1_OUT)
- Pin 21:** SCK_ADC_EXT to PA5 (ADC12_IN5/DAC2_OUT)
- Pin 22:** MISO_ADC_EXT to PA6 (ADC12_IN6)
- Pin 23:** RX_SCL_MOSI to PA7 (ADC12_IN7)
- Pin 41:** H3 to PA8
- Pin 42:** H2 to PA9 (OTG_FS_VBUS)
- Pin 43:** H1 to PA10
- Pin 44:** USB_DM to PA11
- Pin 45:** USB_DP to PA12
- Pin 26:** BR_S02D to PB0 (ADC12_IN8)
- Pin 27:** BR_S01D to PB1 (ADC12_IN9)
- Pin 57:** SERVO to PB5
- Pin 58:** HALL_1D to PB6
- Pin 59:** HALL_2D to PB7
- Pin 61:** CAN_RXD to PB8
- Pin 62:** CAN_TX to PB9
- Pin 29:** RX_SCL_MOSI to PB10
- Pin 30:** TX_SDA_NSS to PB11
- Pin 33:** DC_CALD to PB12
- Pin 34:** L3 to PB13 (OTG_HS_VBUS)
- Pin 35:** L2 to PB14
- Pin 36:** L1 to PB15
- Pin 8:** TEMP_MOTORD to PC0 (ADC123_IN10)
- Pin 9:** AN_IND to PC1 (ADC123_IN11)
- Pin 10:** LED_GREEN to PC2 (ADC123_IN12)
- Pin 11:** LED_RED to PC3 (ADC123_IN13)
- Pin 24:** LED_GREEN to PC4 (ADC12_IN14)
- Pin 25:** LED_RED to PC5 (ADC12_IN15)
- Pin 37:** TX_SDA_NSS to PC6
- Pin 38:** RX_SCL_MOSI to PC7
- Pin 39:** EN_GATE to PC8
- Pin 40:** HALL_3D to PC9
- Pin 51:** FAULT to PC10
- Pin 52:** HALL_3D to PC11
- Pin 53:** FAULT to PC12
- Pin 2:** PC13 (RTC_AF1)
- Pin 54:** PD2
- Pin 3:** PC14-OSC32_IN
- Pin 4:** PC15-OSC32_OUT
- Pin 5:** PH0-OSC_IN
- Pin 6:** PH1-OSC_OUT
- Pin 60:** BOOT0 (VFP)
- Pin 28:** PB2-BOOT1
- Pin 7:** NRST (Reset pin internally pulled up)
- Pin 46:** PA13 (JTMS-SWDIO)
- Pin 49:** PA14 (JTCK-SWCLK)
- Pin 50:** PA15 (JTDI)
- Pin 55:** PB3 (JTDO/TRACESW0)
- Pin 56:** PB4 (NJTRST)
- Pin 19:** VDD
- Pin 32:** VDD
- Pin 48:** VDD
- Pin 64:** VDD
- Pin 18:** VSS
- Pin 63:** VSS
- Pin 1:** VBAT
- Pin 13:** VDDA
- Pin 12:** VSSA
- Pin 31:** VCAP1
- Pin 47:** VCAP2

The diagram also shows a crystal oscillator circuit with a 8MHz crystal (X2) and two 15pF capacitors (C15, C38). A 100nF capacitor (C32) is connected to the NRST pin. Power management components include a 2.2uF capacitor (C31) connected to VBAT, a 2.2uF capacitor (C35) connected to VDDA, and two 2.2uF capacitors (C16, C17) connected to VCAP1 and VCAP2 respectively.



FEATURES

- Operating Supply Voltage 8V–60V
- 2.3A Sink and 1.7A Source Gate Drive Current Capability
- Integrated Dual Shunt Current Amplifiers With Adjustable Gain and Offset
- Integrated Buck Converter to Support up to 1.5A External Load
- Independent Control of 3 or 6 PWM Inputs
- Bootstrap Gate Driver With 100% Duty Cycle Support
- Programmable Dead Time to Protect External FETs from Shoot Through
- Programmable Overcurrent Protection of External MOSFETs
- Thermally Enhanced 56-Pin TSSOP Pad Down DCA Package

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNITS
PVDD1	DC supply voltage PVDD1 for normal operation	8	60		V
PVDD2	DC supply voltage PVDD2 for buck converter	3.5	60		V
C _{AVDD}	External capacitance on AVDD pin (ceramic cap) 20% tolerance		1		μF
C _{PVDD}	External capacitance on PVDD pin (ceramic cap) 20% tolerance		1		μF
C _{GVDD}	External capacitance on GVDD pin (ceramic cap) 20% tolerance		2.2		μF
C _{CP}	Flying cap on charge pump pins (between CP1 and CP2) (ceramic cap) 20% tolerance		22		nF
C _{BS1}	Bootstrap cap (ceramic cap)		100		nF
I _{SEN_H}	Input current of digital pins when EN_GATE is high		100		μA
I _{SEN_L}	Input current of digital pins when EN_GATE is low		1		μA
C _{DI}	Maximum capacitance on digital input pin		10		pF
C _{LO}	Maximum output capacitance on outputs of shunt amplifier		20		pF
R _{OTC}	Dead time control resistor range. Time range is 50ns (150kΩ) to 500ns (150kΩ) with a linear approximation.	0	150		kΩ
I _{FAULT}	FAULT pin sink current. Open-drain		2		mA
I _{OCTW}	OCTW pin sink current. Open-drain		2		mA
V _{REF}	External voltage reference voltage for current shunt amplifiers		2		V
f _{sw}	Operating switching frequency of gate driver		200		kHz
T _A	Ambient temperature	-40	125		°C

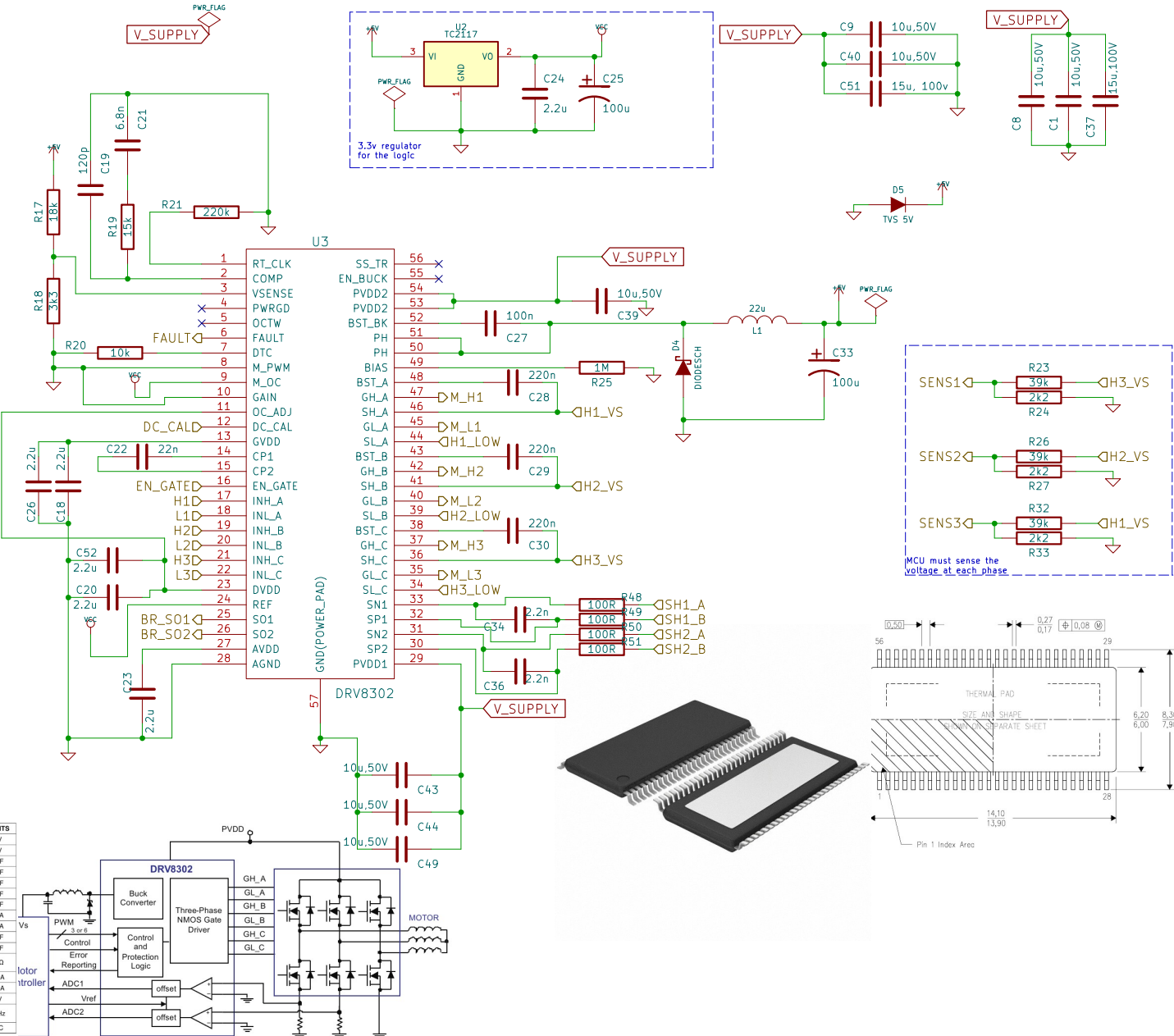
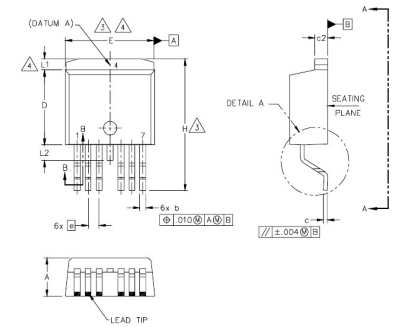
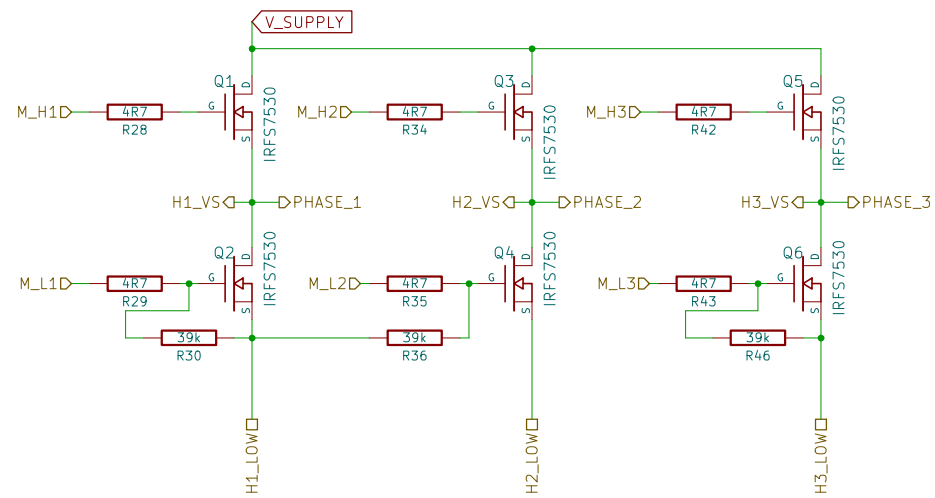
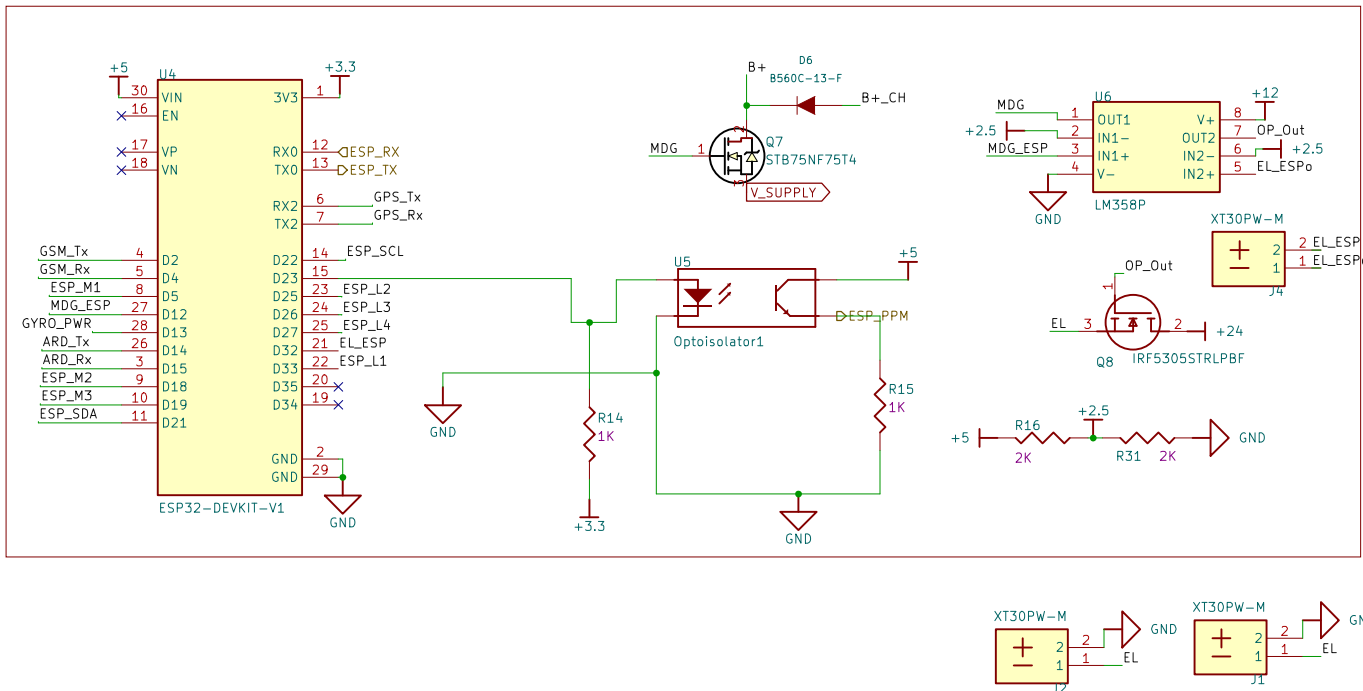


Figure 1. DRV8302 Simplified Application Schematic



Current Design

BD139 IRFZ44 BD140(PNP)



Connectors

