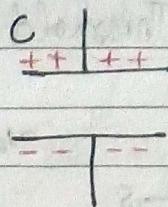
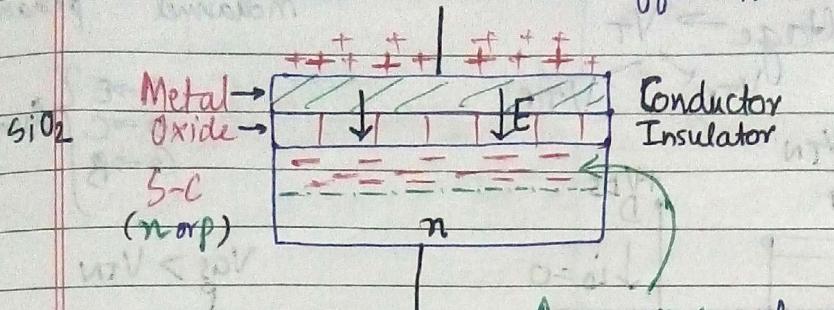


MOSFET

Metal Oxide Semiconductor Field Effect Transistor

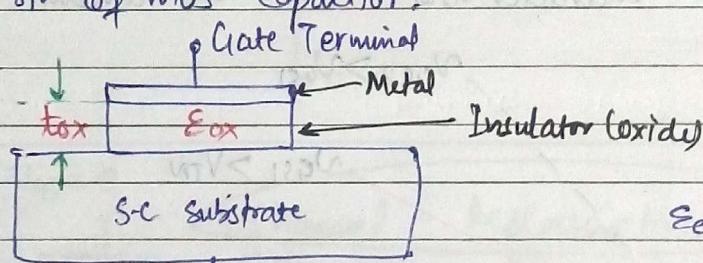


Accumulation (n-type S-C) { Collection of -ve charges

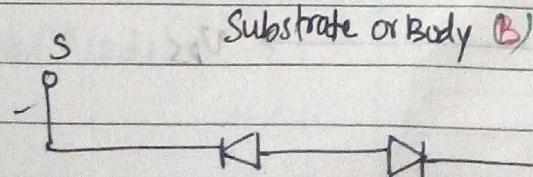
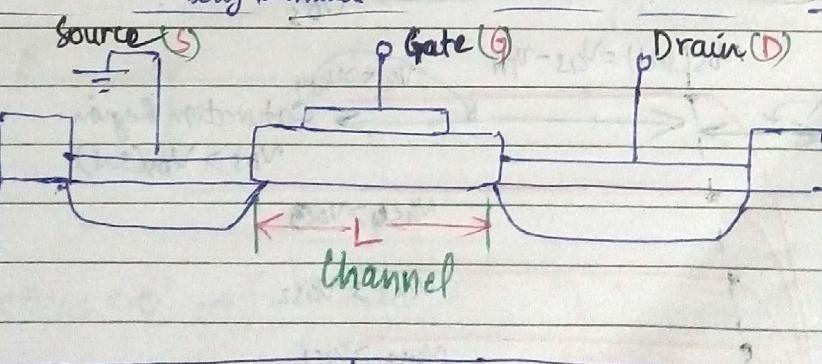
for p type S-C, -ve charge comes from battery.

→ pseudo n type region is formed, called Inversion.

Basic str. of MOS capacitor:-



E_{ox} = Permittivity of oxide material.

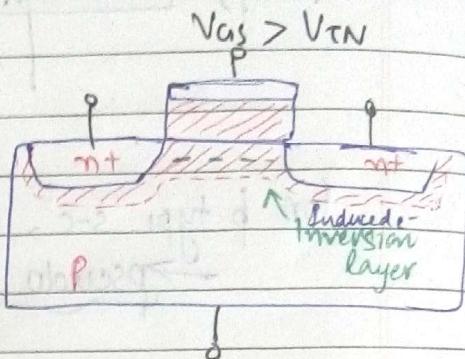
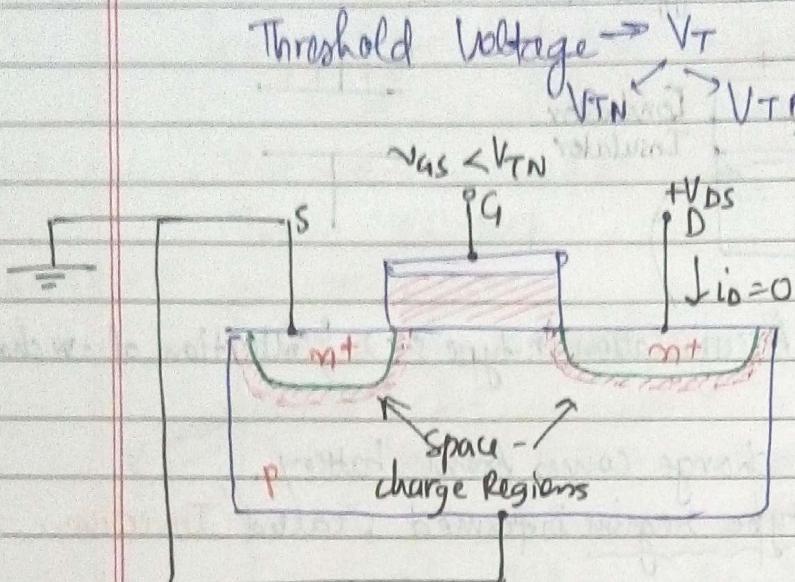


(Drain & Source can be interchanged).

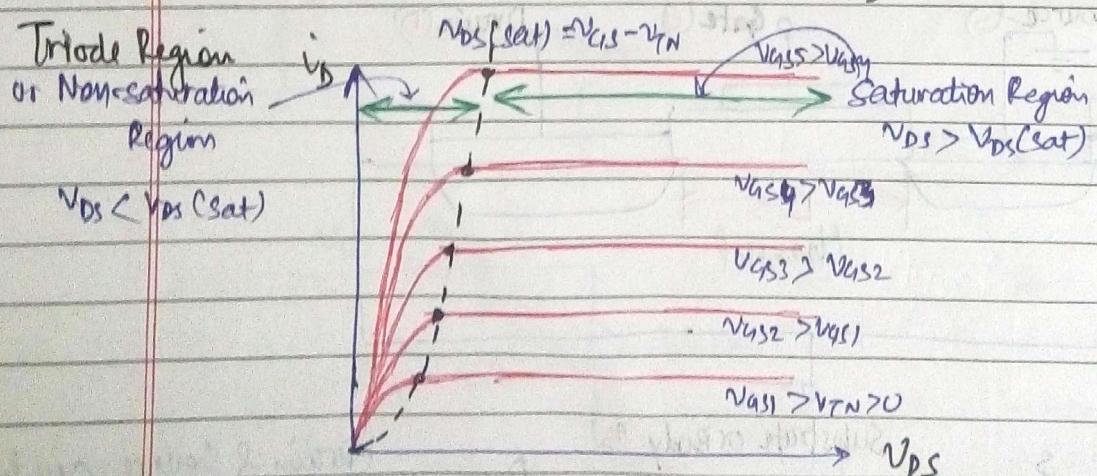
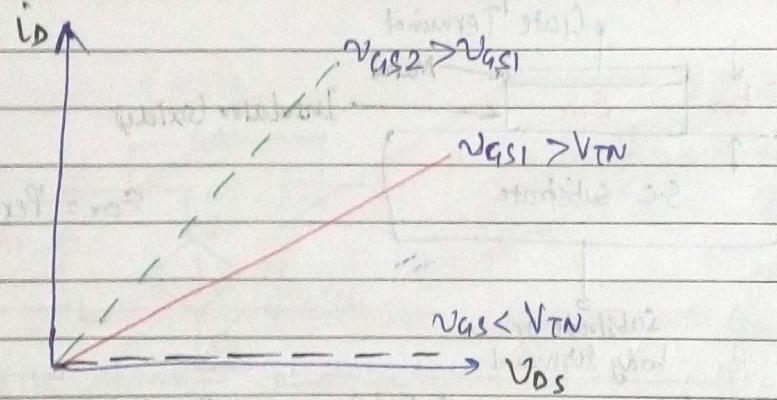
A conductive channel is formed between S & D after formation of inversion layer.

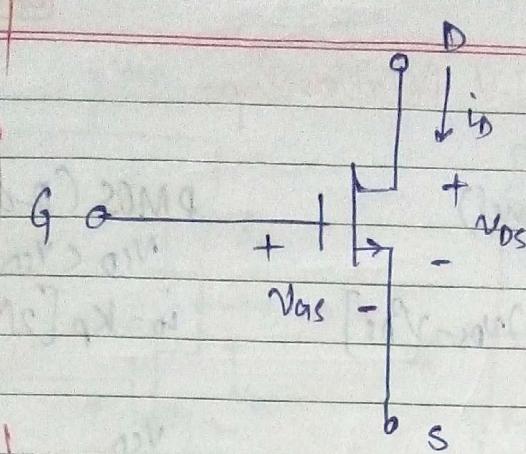
MOSFET
 mchannel pchannel

S → E }
 D → C }
 G → B }
 Analogy

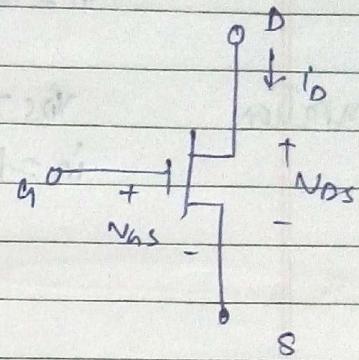
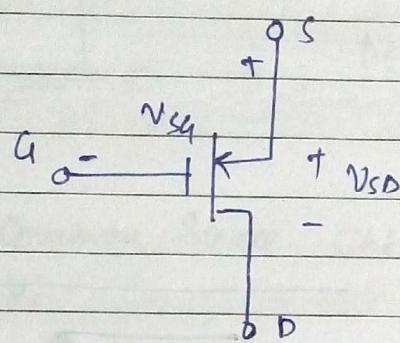


I vs V characteristics : Enhancement mode in MOSFET.

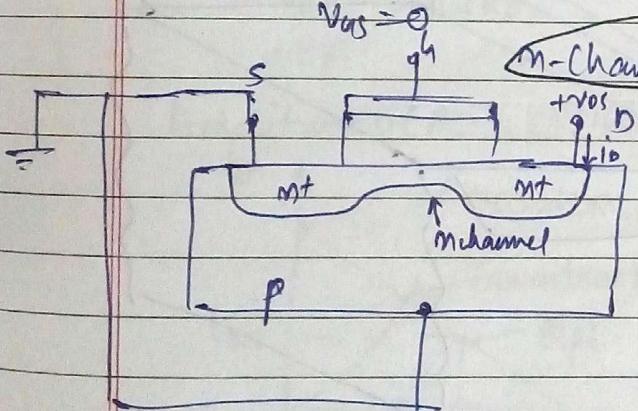




Symbols for n-channel
Enhancement-Mode
MOSFET
(Normally OFF)

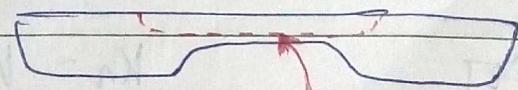


$V_{GS} = 0$ n-channel Depletion-Mode - MOSFET



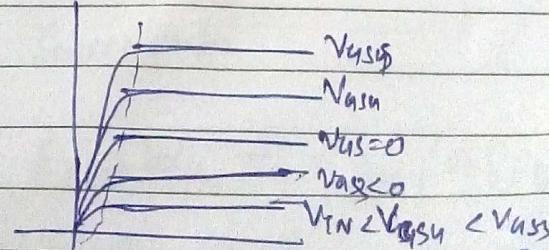
Pre-established connectivity
(normally ON)

$$V_{TN} < V_{GS} < 0 \rightarrow$$



Depletion Region

Depletion Mode:-



Summary of I-V Relationships

Region

Max-saturation

NMOS (n-channel)

$$V_{DS} < V_{DS(\text{sat})}$$

$$i_D = K_n [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

PMOS (p-channel)

$$V_{SD} < V_{SD(\text{sat})}$$

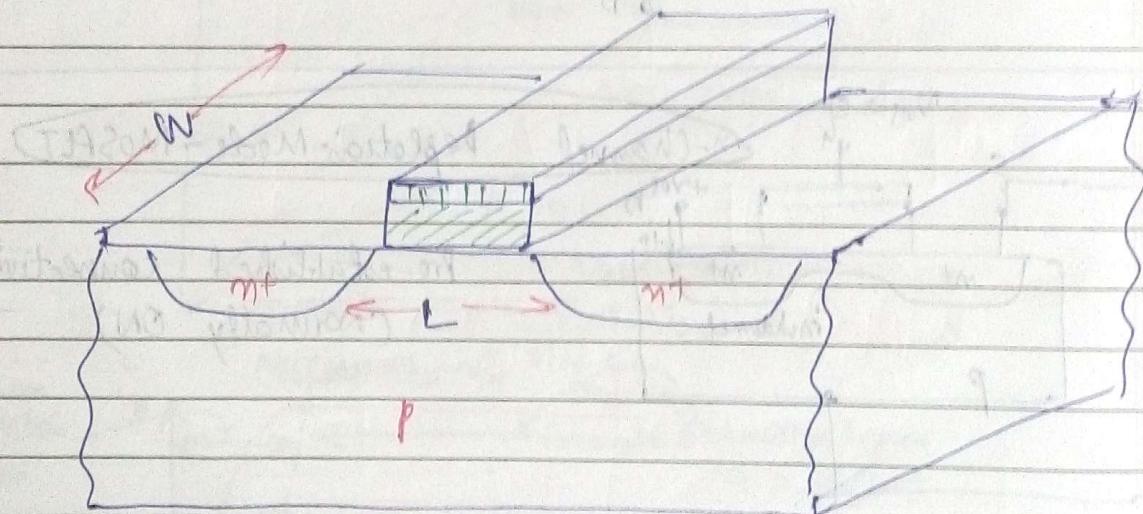
$$i_D = K_p [2(V_{SG} + V_{CP})V_{SD} - V_{SD}^2]$$

Saturation

$$V_{DS} > V_{DS(\text{sat})}$$

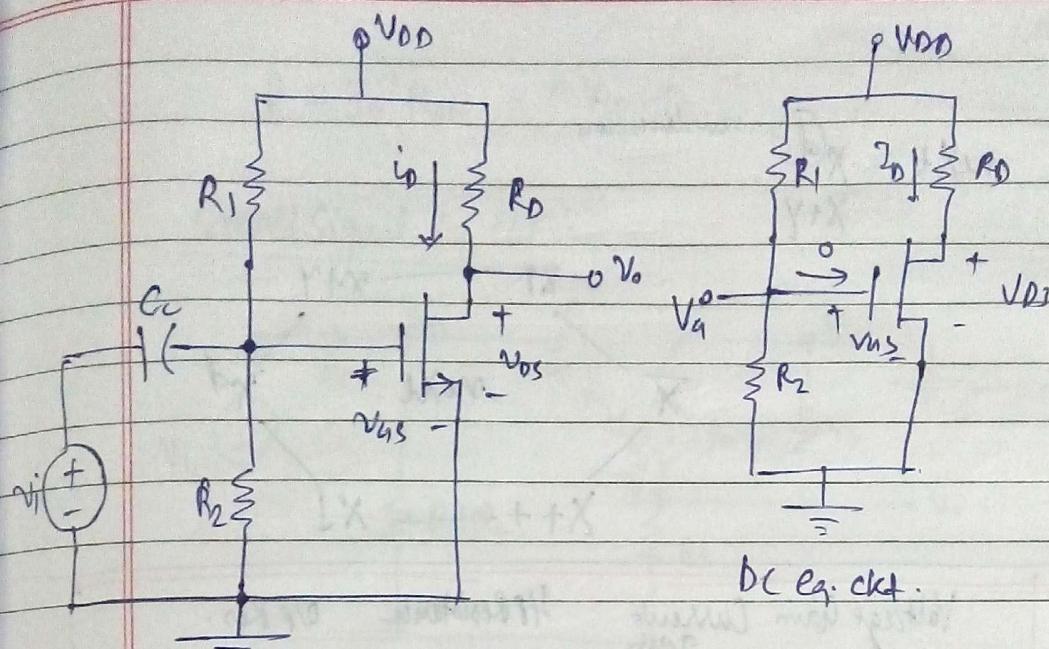
$$i_D = K_n [V_{GS} - V_{TN}]^2$$

$$V_{SD}$$



N-MOSFET

$$K_n = \frac{W}{L} \mu_n C_{ox} = k_n \frac{W}{L}$$

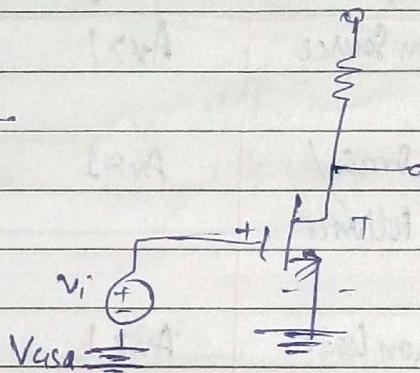


NMOS Common Source Ckt.

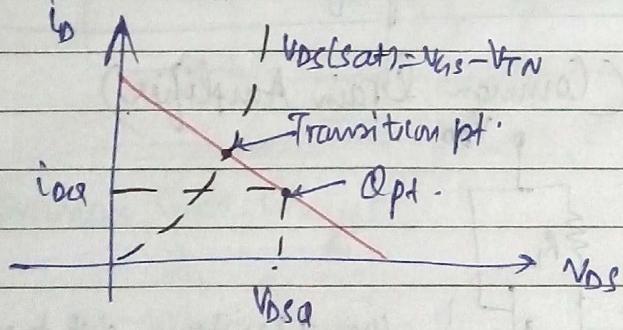
$$V_{gs} = V_i$$

$$I_d = g_m V_{gs}$$

$$V_{ds} = -I_d R_o$$



Addition of $R \rightarrow$ Time const of ckt $\tau_{os} \Rightarrow$ ckt becomes relatively slow.



Transfer ch. (slope = gm) V_{os} up I_D

e NMOS common Source Ckt.

ANUBHAV
AIN NOTES

$$\Delta v = v_o / v_i = -g_m (R_o || R_o)$$

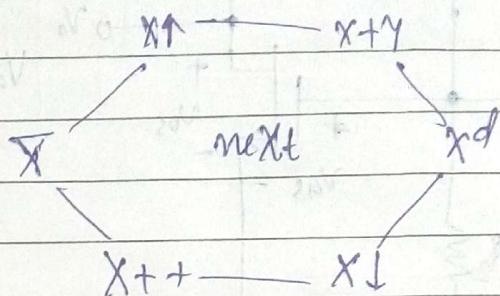
$v_h = \sqrt{KTR}$ Small Signal Eq. Ckt.

$$\Delta v = v_o / v_i = -g_m (R_o || R_o) \left(\frac{R_i}{R_i + R_{si}} \right)$$

Idea Hexagon.

$$\text{next} = x^{(d)} \text{ new dimension}$$

$$x+y$$

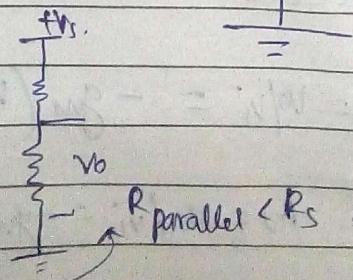
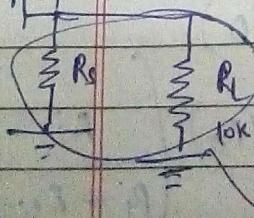
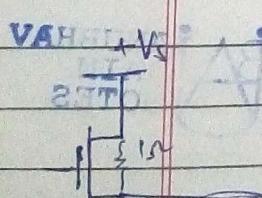
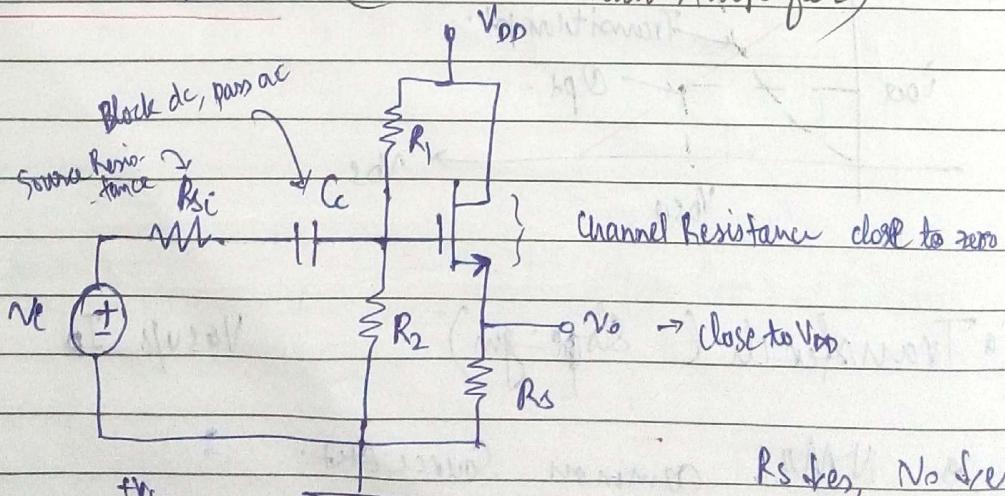


28/09/16

Conf.	Voltage gain Current gain	R_{TH}	O/P Res.
Common Source	$A_v > 1$	R_{TH}	Moderate to high
Common Drain/ Source follower	$A_v \approx 1$	R_{TH}	Low
Common Gate	$A_v \approx 1$, $A_I \approx 1$	Low	Moderate to high

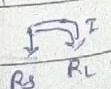
3 Basic MOSFET Amplifiers.

NMOS Source follower (Common Drain Amplifier)



$$R_{\text{parallel}} < R_S \Rightarrow R_{\text{load}} \Rightarrow V_{O \text{ load}}$$

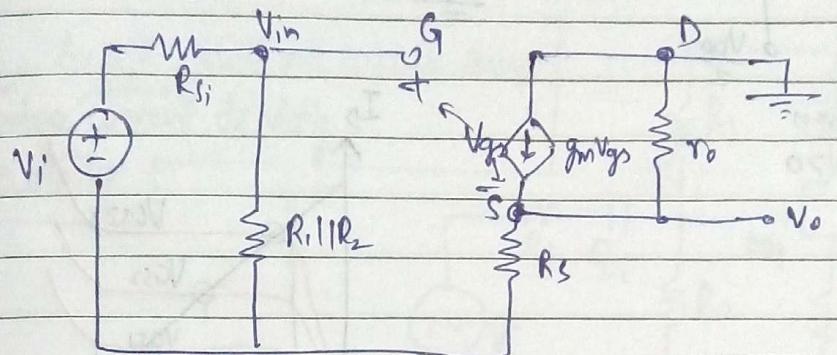
$$R_S = 1/V_{A2}, R_V = V_{A2}$$



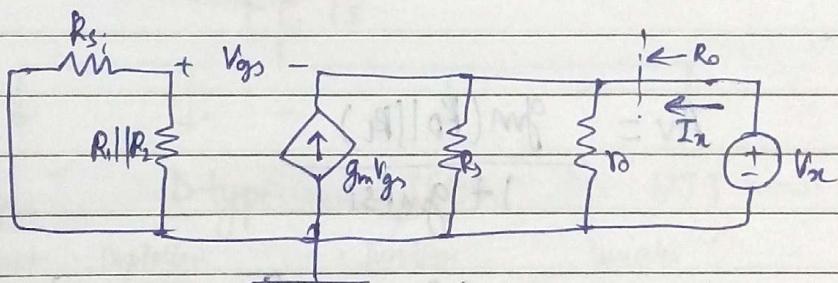
$R_S \downarrow \text{res.}$, $N_o \downarrow \text{res.}$

$$P = I_D^2 R_{ON} = V_{CE} \cdot I_D.$$

Small Signal Eq. (Cut) -

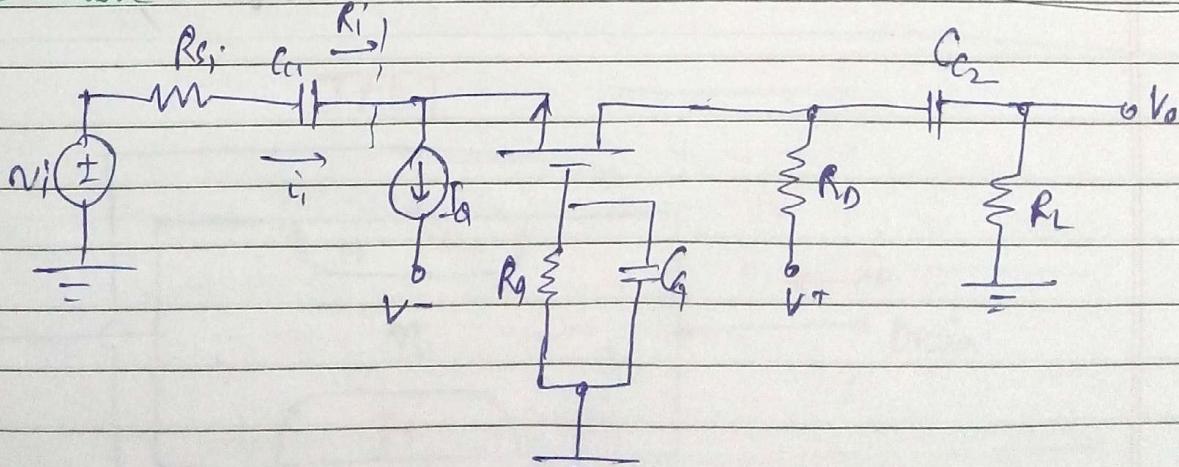


$$A_V = \frac{R_S || R_O}{\frac{1}{g_m} + R_S || R_O} \times \frac{(R_i)}{(R_i + R_{S,i})}$$

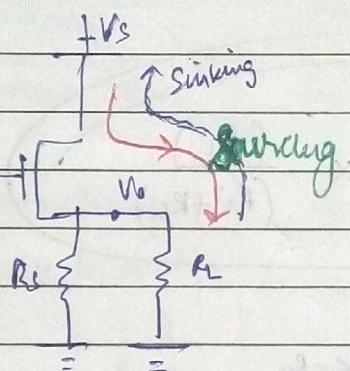
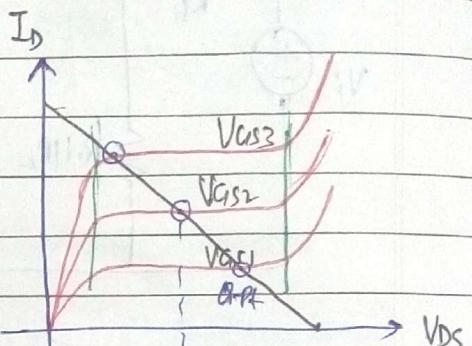
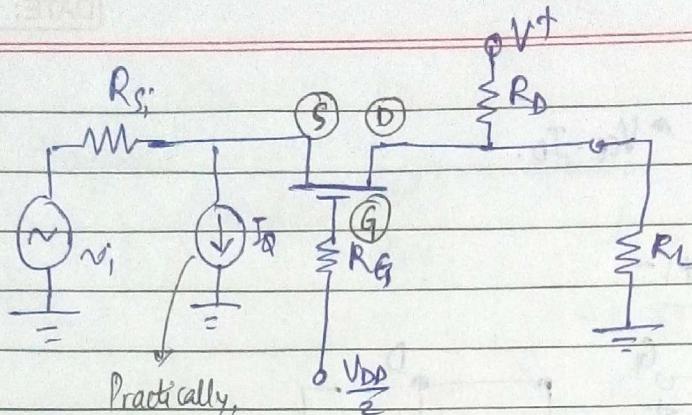


$$R_o = \frac{1}{g_m} || R_S || R_O.$$

Common Gate Circuit



V-I characteristics intersects load line $\Rightarrow Q$ -point



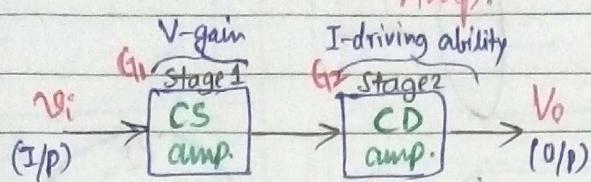
$$A_v = \frac{g_m (R_D / R_L)}{1 + g_m R_{si}}$$

$$A_i = \frac{I_0}{I_i} = \left(\frac{R_D}{R_D + R_L} \right) \left(\frac{g_m R_{si}}{1 + g_m R_{si}} \right)$$

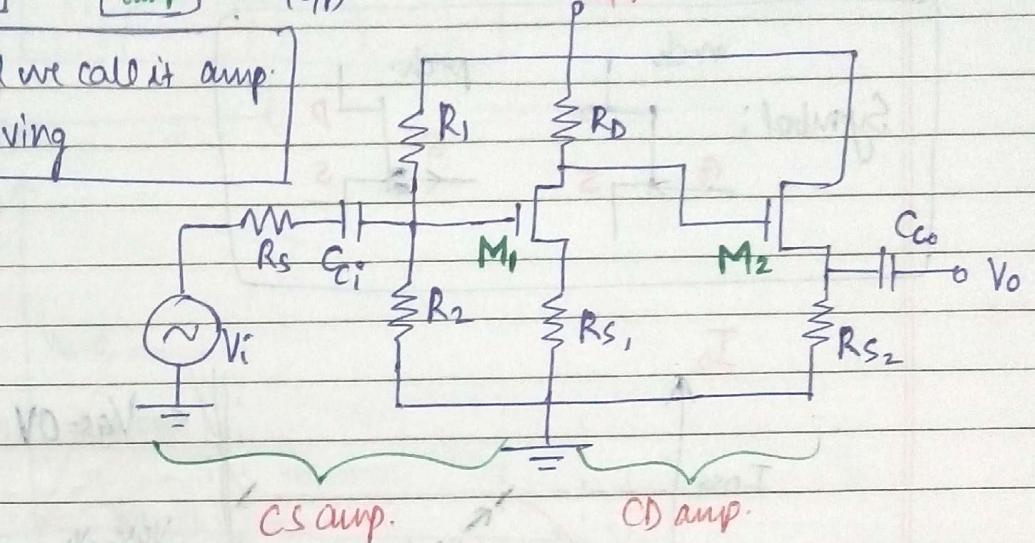
VANNA
N
25T

Cascaded Mosfet

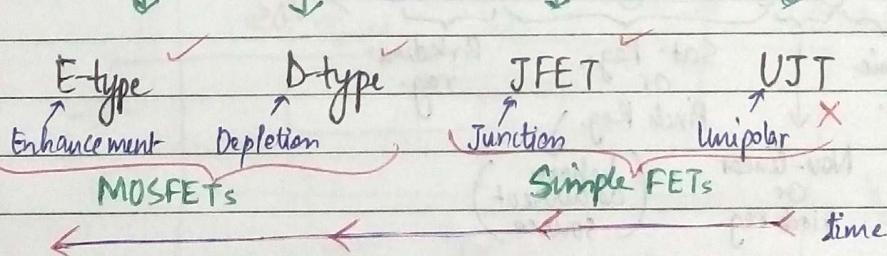
Amp.



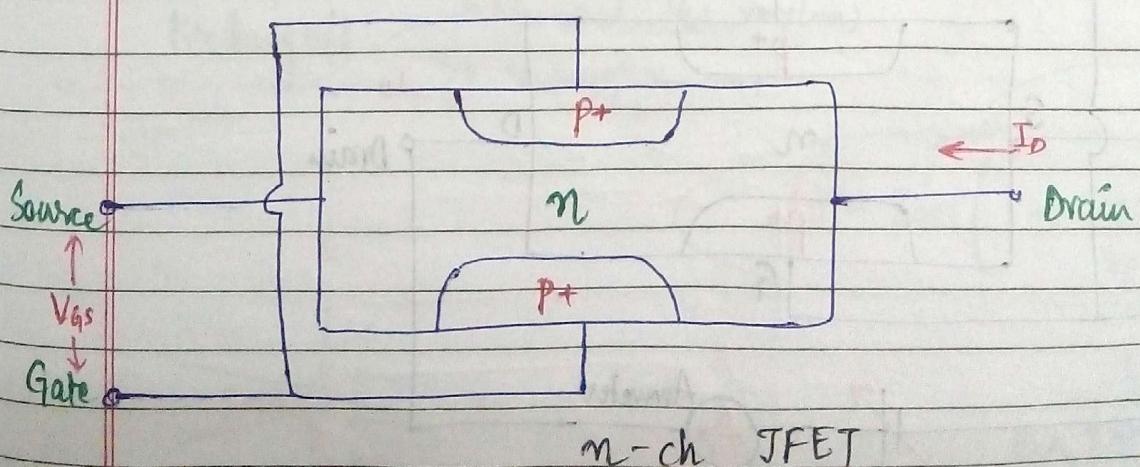
CD amp; $A_v \approx 1$, still we call it amp.
 \because It helps in improving current driving ability [enhancing]

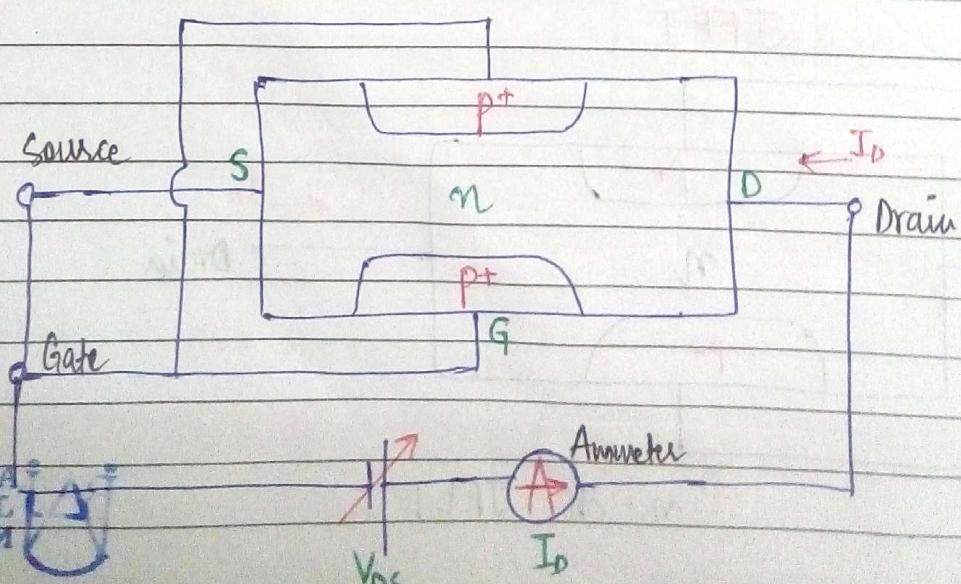
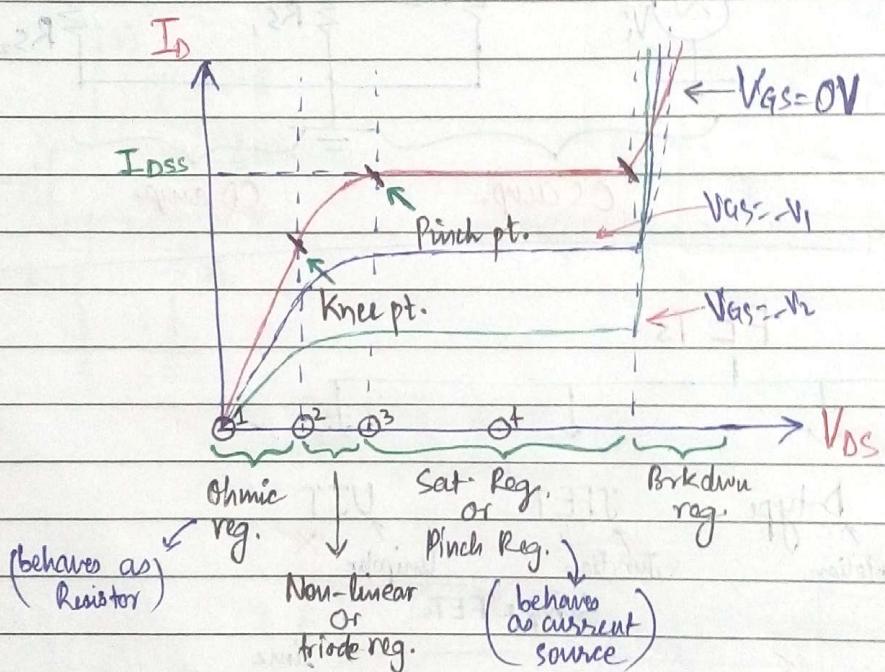
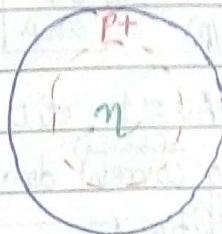
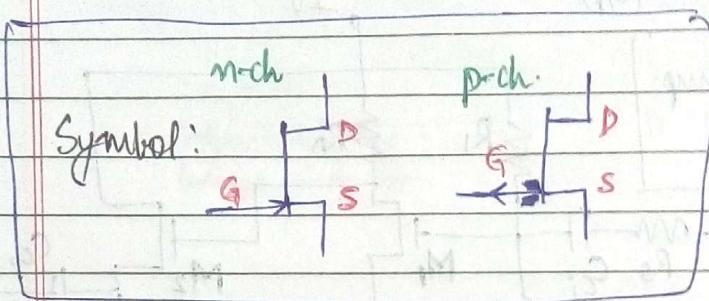
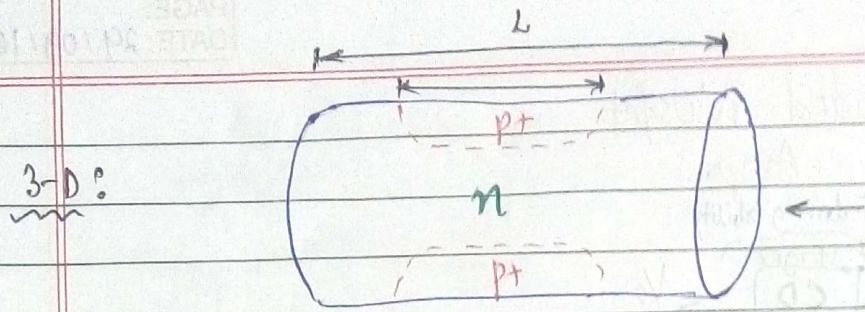


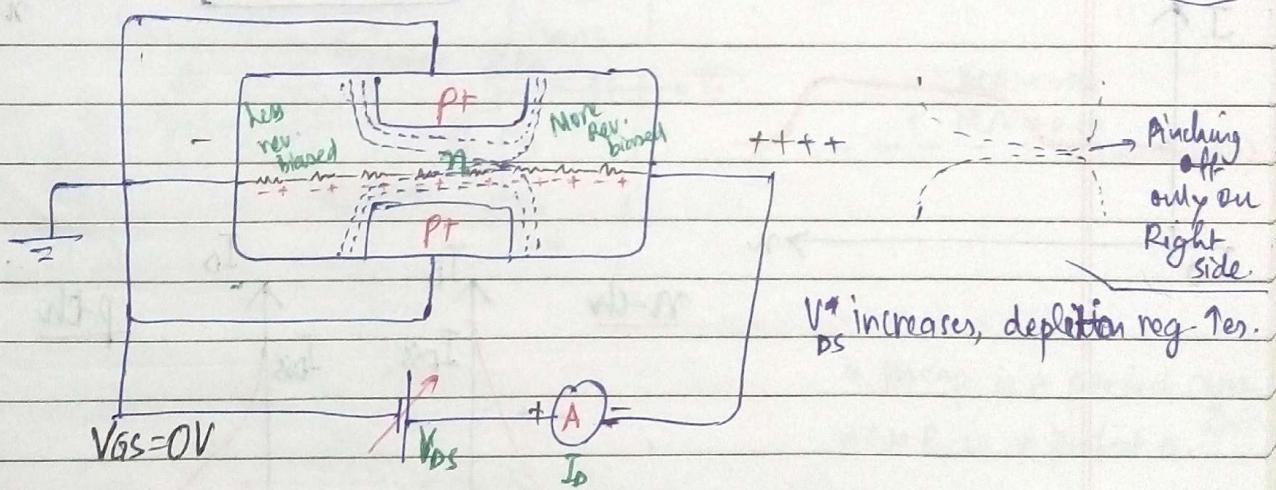
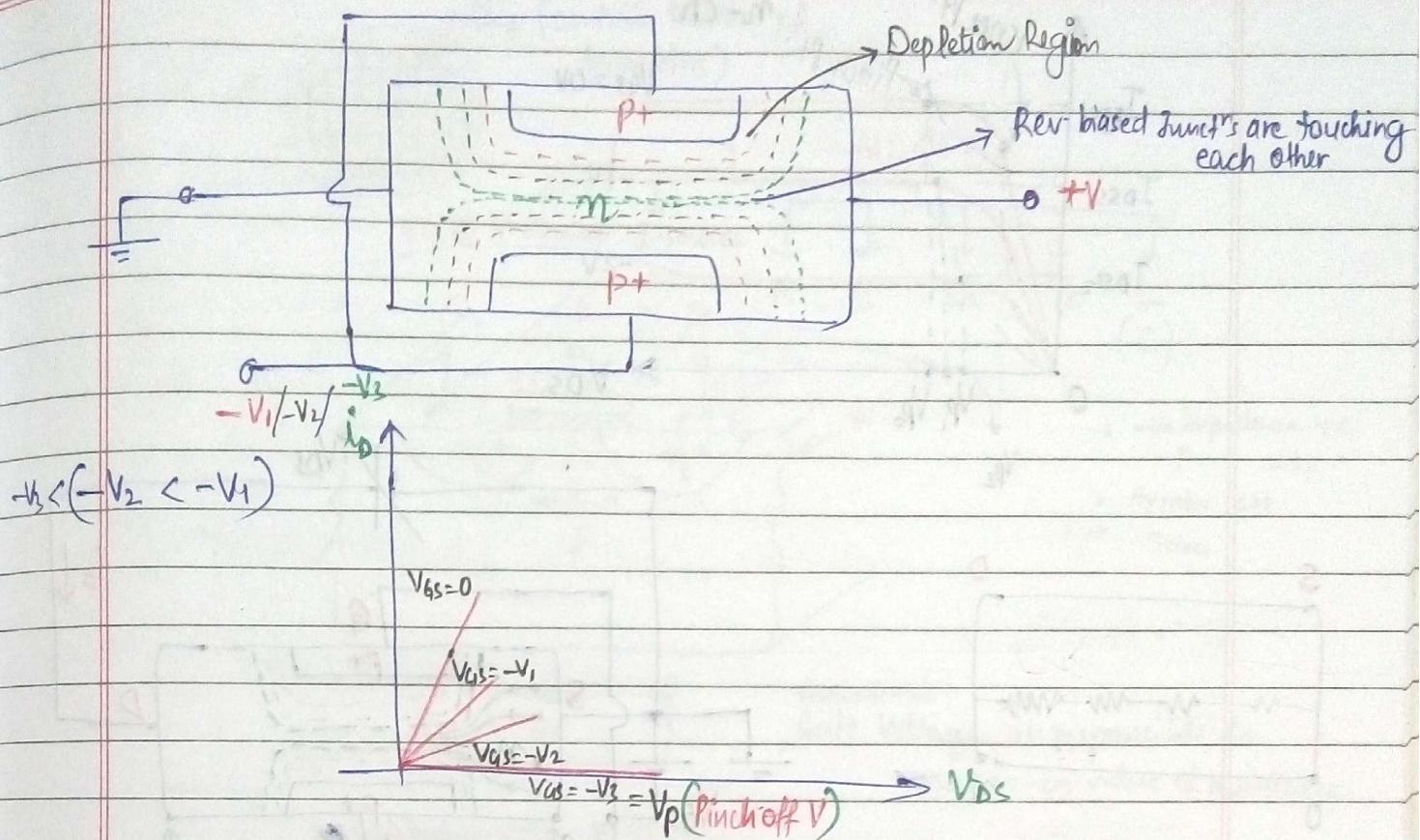
FETs



JFET







Pinching off:

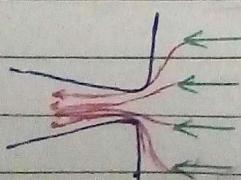
- \rightarrow Nos cont., V_{GS} vary (neg)
- \rightarrow $V_{GS} = \text{const}$, V_{DS} vary

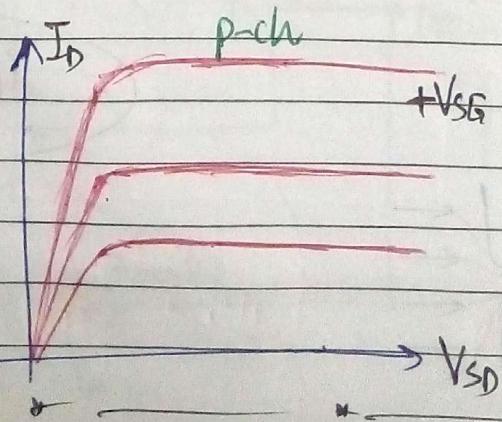
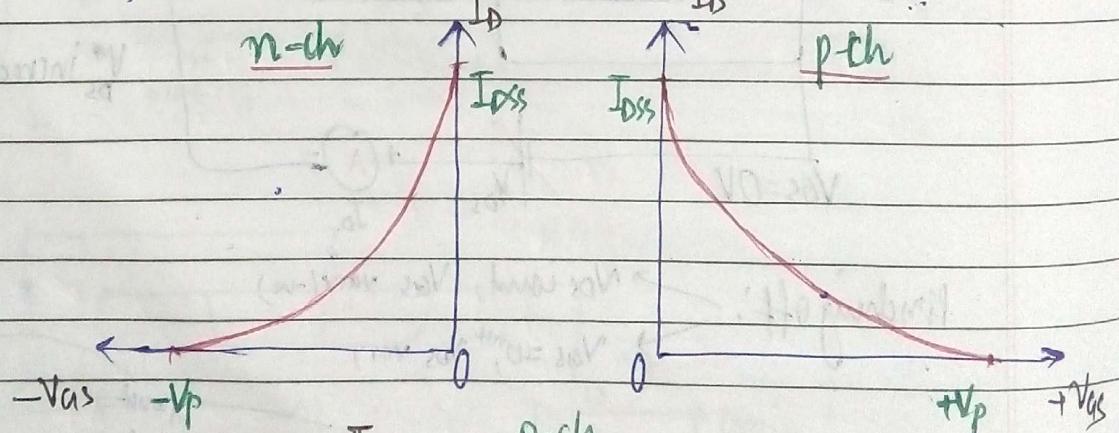
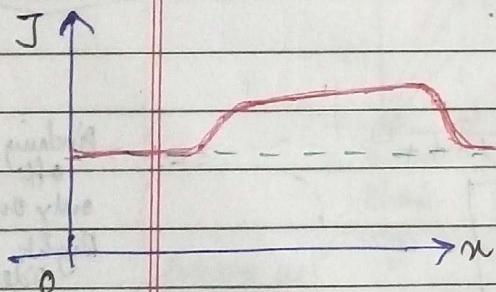
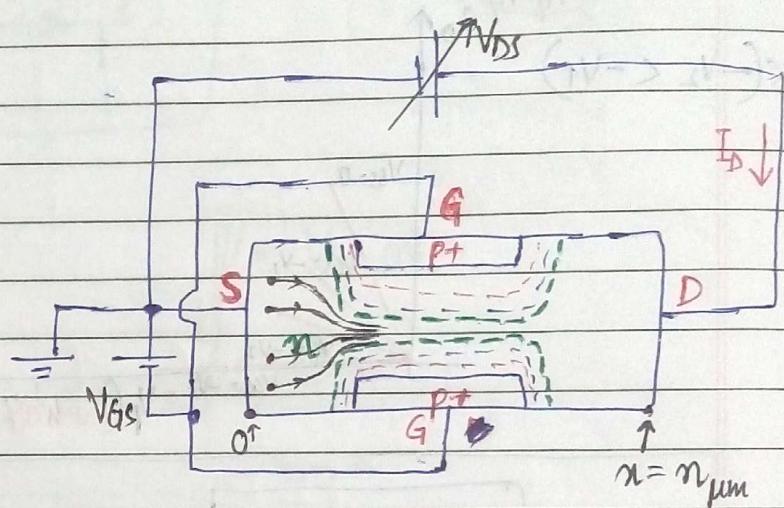
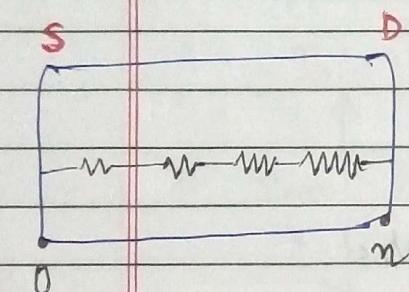
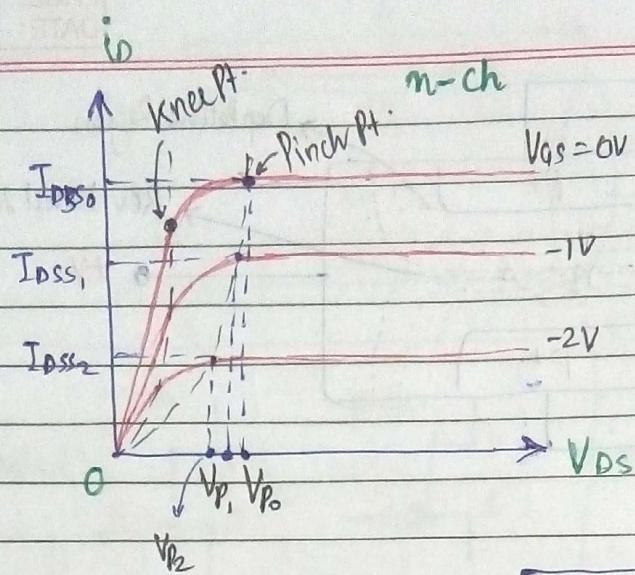
$$i_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

with I_{DSS} const.

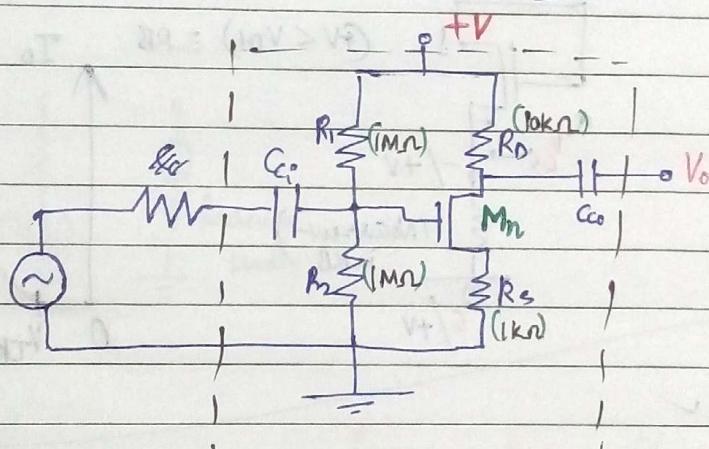
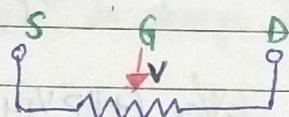
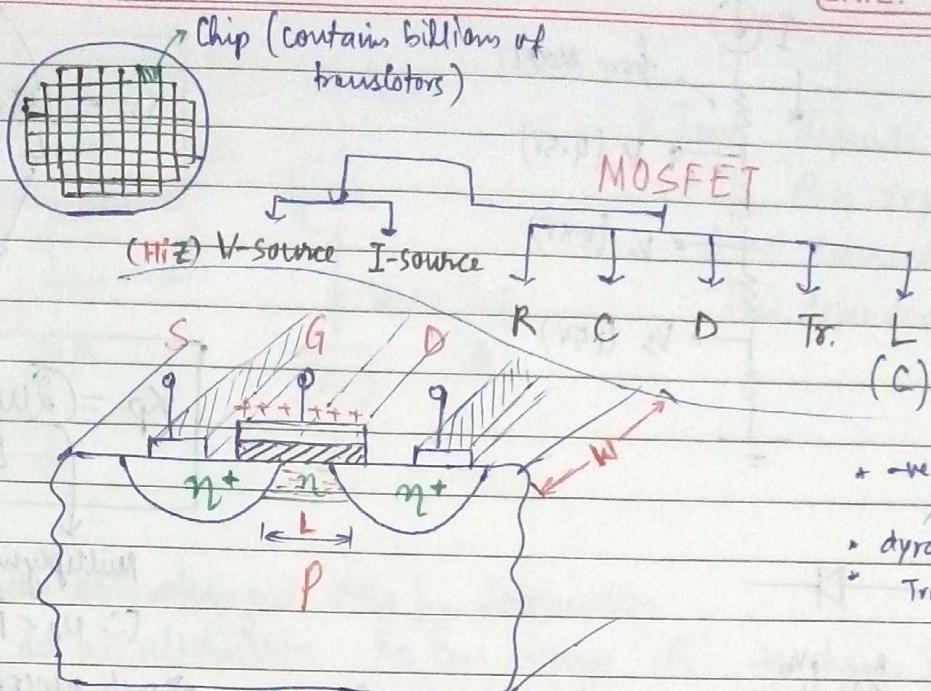
(Characteristic parameters)

Brijesh
Jain
NOTES

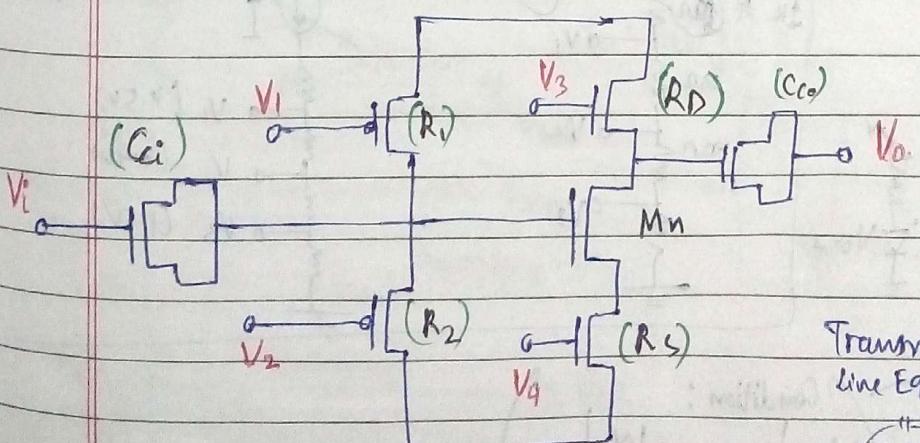




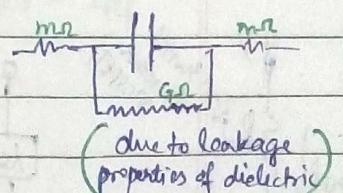
Value
Max
Min
Avg



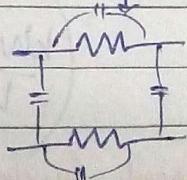
* No cap. is a perfect capacitor.
* No R is a perfect R.



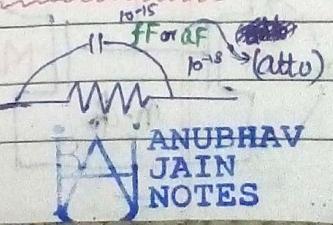
Practical Capacitor!:-



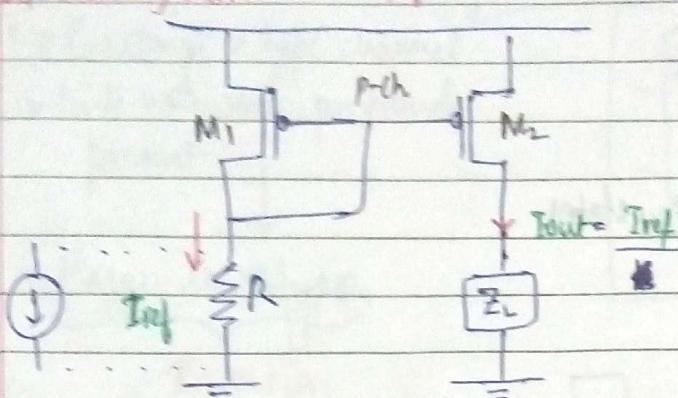
Transmission line Eq. Model



Practical Resistor!:-



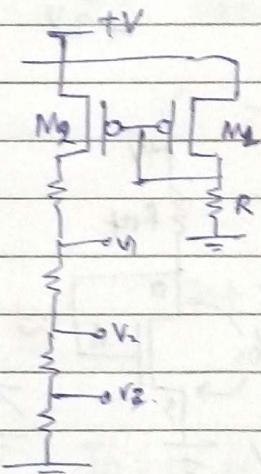
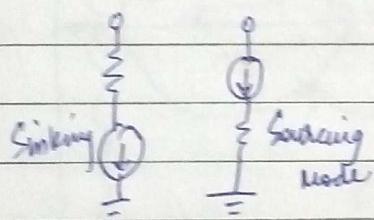
Current Matching Mirror



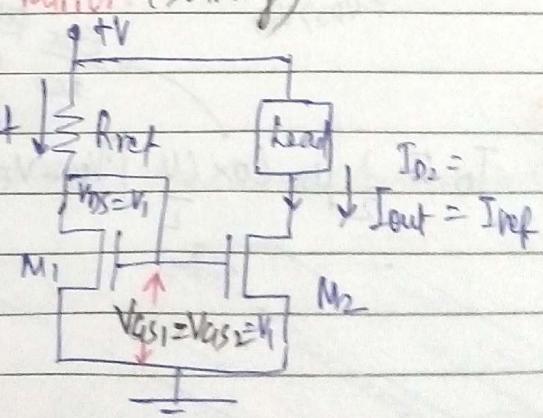
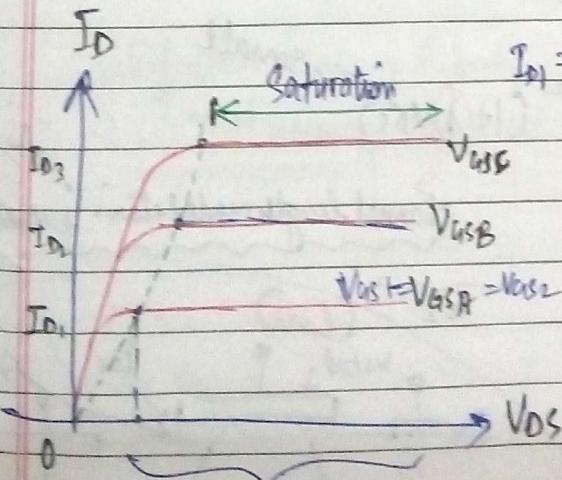
* I_{out} depends on V_t .
 → If R is replaced by const. current source, this dependence \downarrow .

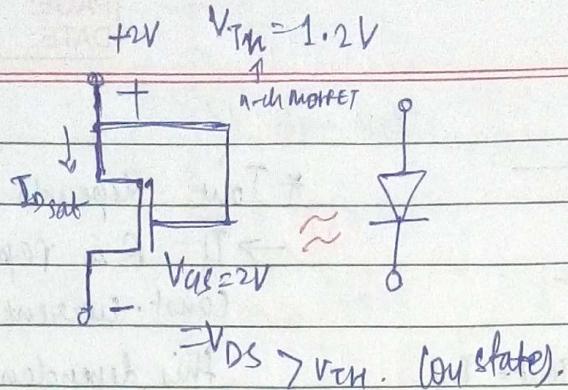
- V_t can be changed only by fabrication.

So, as an alternative, we can change R to change I_{ref} and finally, to change I_{out} .

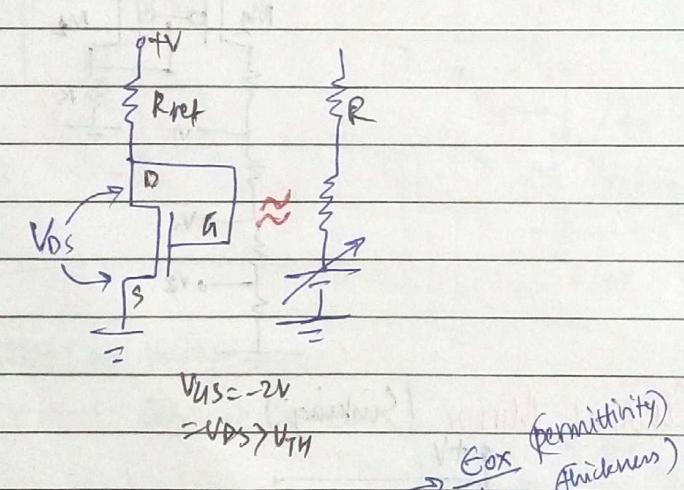
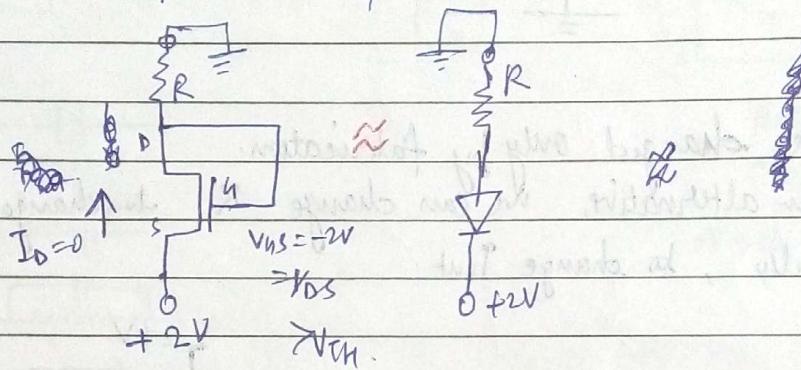


Current Mirror (Sinking)





Polarity Reverse \Rightarrow

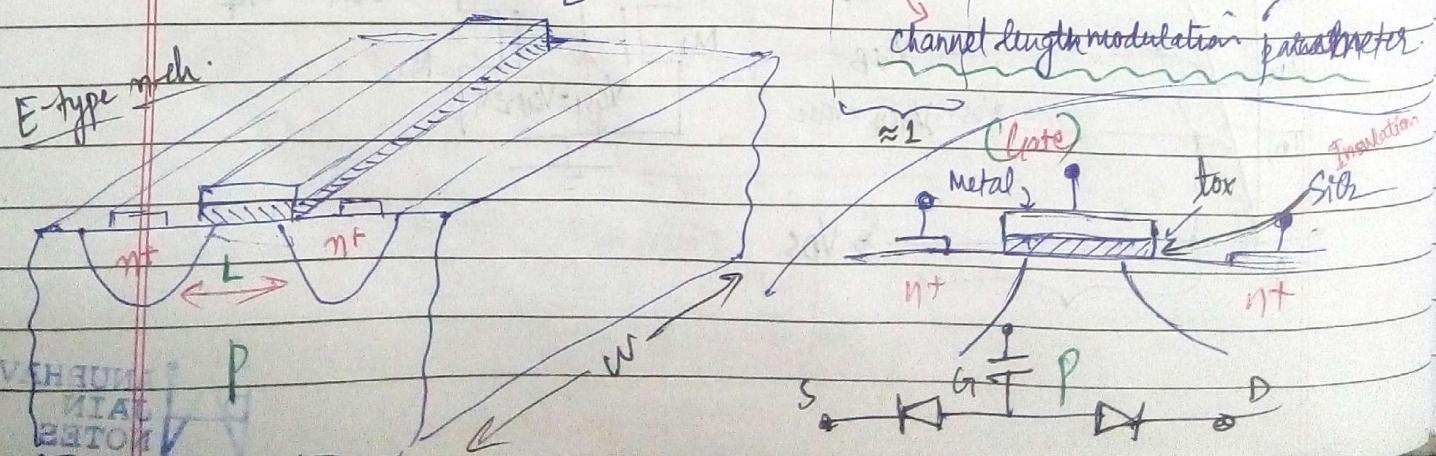


$$I_D = \frac{1}{2} \mu n C_{ox} W [V_{GS} - V_{TH}]^2 (1 + \lambda V_{DS})$$

small

C_{ox} (permittivity)
 t_{ox} (thickness)

channel length modulation parameter.



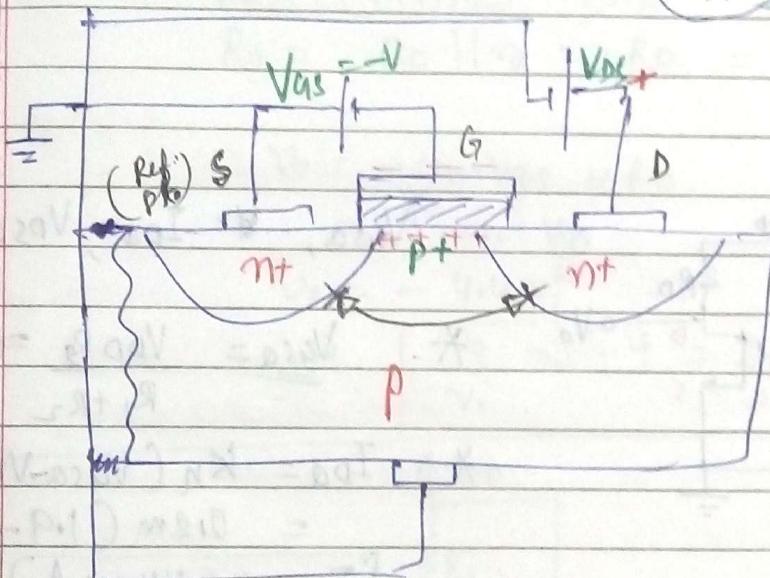
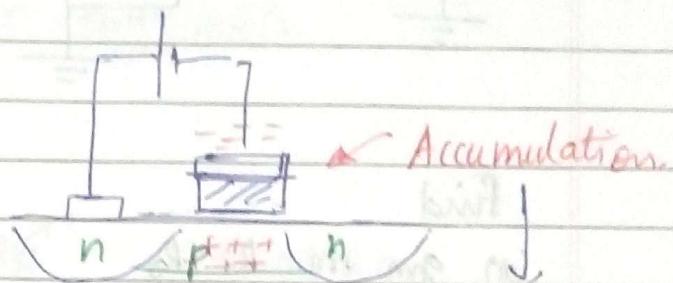
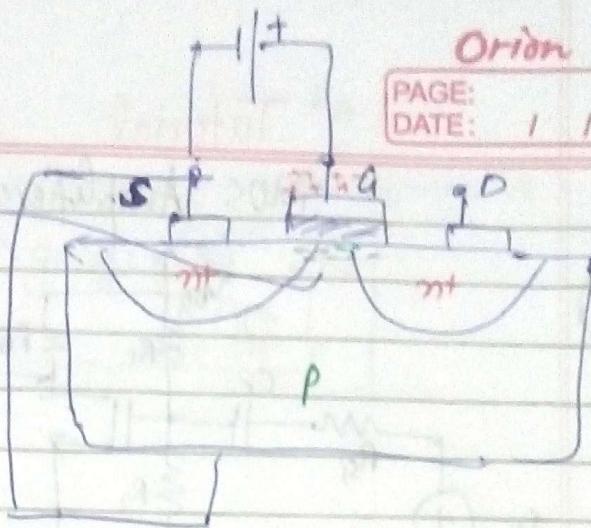
enhancement type

→ Creating n-type channel which was not previously present

p-type to n-type

Inversion

$V_{GS} > 0$ for n-ch MOSFET
(> 0 for p-ch)



$V_{GS} < 0$ for n-ch MOSFET
(> 0 for p-ch)

n+: highly doped n-type

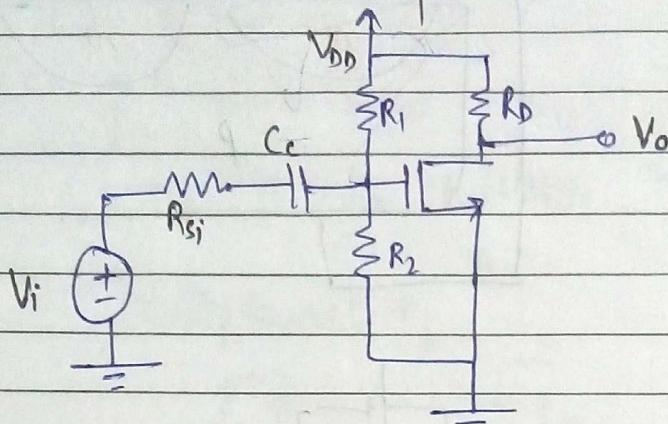
$I_D = 0$ if $V_{GS} = 0$

Substrate biasing & body effect

→ Not always connected to source, sometimes connected to drain also.

Tutorial MOS Amplifiers.

Q 1.



Given:-

$$V_{DD} = 5V$$

$$R_1 = 520k\Omega$$

$$R_2 = 320k\Omega$$

$$R_D = 10k\Omega$$

$$R_{si} = 0$$

$$V_{TN} = 0.8V$$

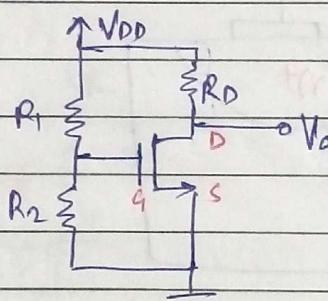
$$K_n = 0.20 \text{ mA/V}^2$$

$$\lambda = 0$$

Find

- (a) g_m , r_o , R_i , R_o
- (b) A_v

Soln:- DC circuit :-



V_{GSA} , I_{DQ} , V_{DSQ} ←

$$V_{GSA} = \frac{V_{DD} R_2}{R_1 + R_2} = 1.9V$$

$$I_{DQ} = K_n (V_{GSA} - V_{TN})^2 \\ = 0.2m (1.9 - 0.8)^2$$

$$I_{DQ} = 0.244 \text{ mA}$$

KVL

$$V_{DD} - I_{DQ} R_D - V_{DSQ} = 0$$

$$\Rightarrow V_{DSQ} = V_{DD} - I_{DQ} R_D$$

$$V_{DSQ} = 2.56V$$

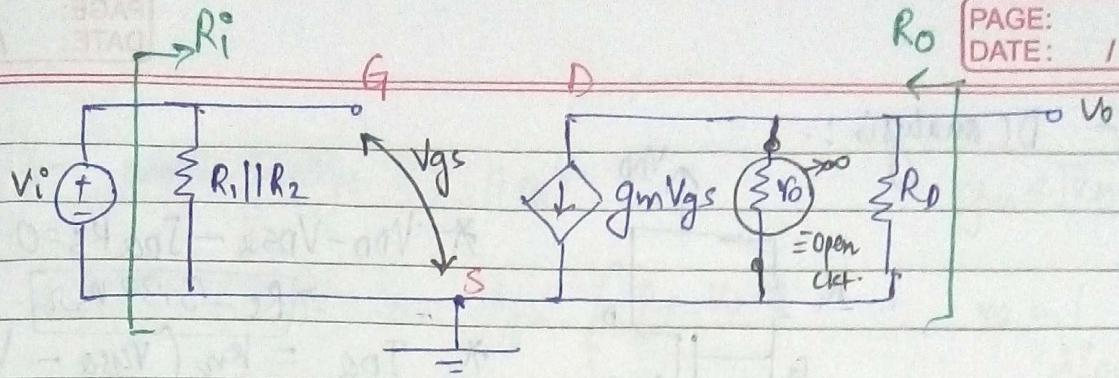
Sat. Region:

$$(V_{GSA} - V_{TN}) < V_{DSQ}^{2.56} \rightarrow \text{Condition Satisfied} \quad \checkmark$$

\downarrow

\Rightarrow MOSFET will operate.

else, $(V_{GSA} - V_{TN}) \neq V_{DSQ} \rightarrow$ Triode Region. (Non-Sat).



(a) $A_v = \frac{V_o}{V_i}$

$$gm = 2\sqrt{k_n I_{DQ}} = 0.44 \text{ mA/V}$$

$$R_i = \frac{1}{\lambda I_{DQ}} = \infty$$

$$R_i = (R_1 || R_2) + R_{si} = 198.09 \text{ k}\Omega$$

$$R_o = R_D || r_o = R_D = 10 \text{ k}\Omega$$

(b) $V_o = -gm V_{gs} \times R_D$

$$= -4.4 V_{gs}$$

$$V_o = -4.4 V_i$$

$$(V_{gs} = V_i)$$

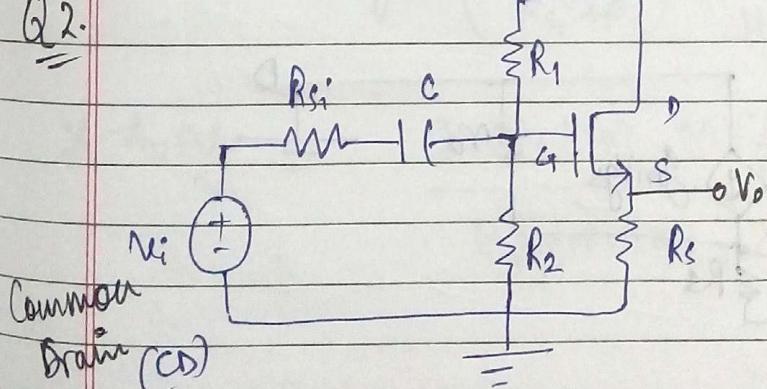
$$\Rightarrow \boxed{\frac{V_o}{V_i} = -4.4 = A_v}$$

Given:

$$I_{DQ} = 1.5 \text{ mA}$$

$$V_{DSQ} = 5 \text{ V}$$

Q2.



$$V_{TN} = 0.8 \text{ V}, k_n = 1 \text{ mA/V}^2$$

$$\lambda = 0.015 \text{ V}^{-1}, V_{DD} = 10 \text{ V}$$

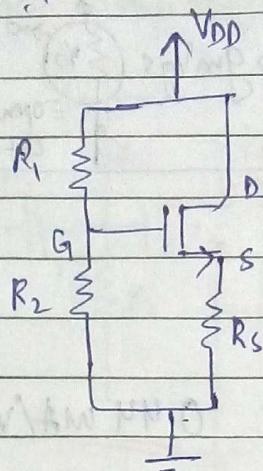
$$R_{si} = 200 \Omega, R_1 + R_2 = 400 \text{ k}\Omega$$

Find

(a) R_1, R_2

(b) A_v

Soln:- DC analysis :-



$$* V_{DD} - V_{DSQ} - I_{DQ} R_S = 0$$

$$\Rightarrow [R_S = 3.33 R_D]$$

$$* I_{DQ} = k_n (V_{GSQ} - V_{IN})^2$$

~~Max value of drain current~~

$$(V_{GS} - V_{IN})^2 = \frac{I_{DQ}}{k_n} = 1.5$$

$$V_{GS} = V_{IN} \pm \sqrt{1.5} > 0$$

$$\Rightarrow V_{GS} = V_{IN} + \sqrt{1.5}$$

$$V_{GS} = 2.025V.$$

$$V_S = I_{DQ} R_S = 5V$$

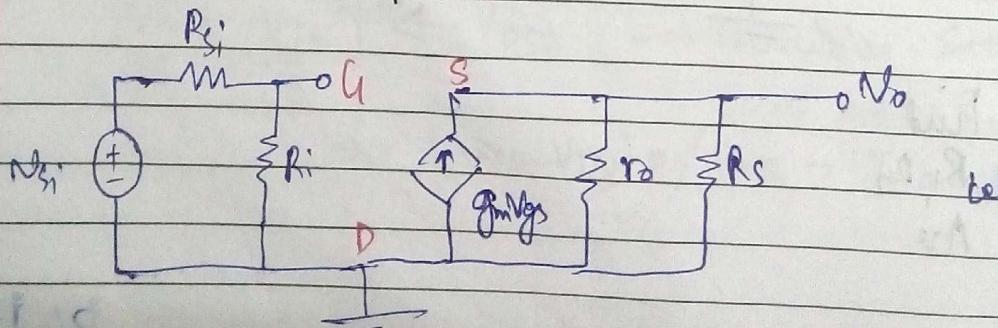
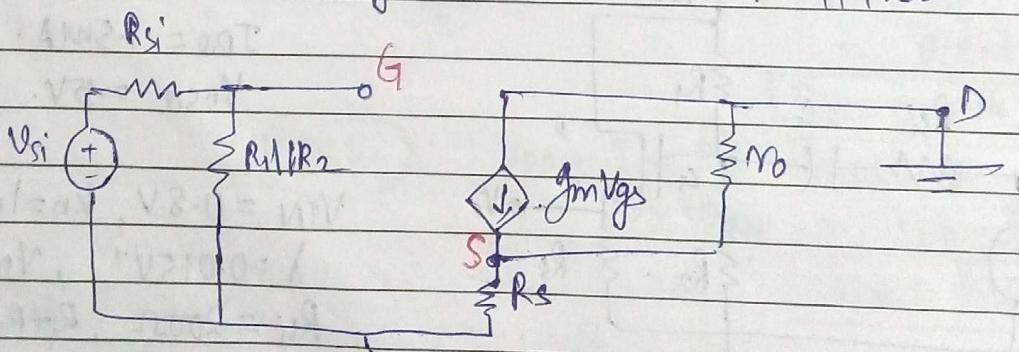
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{R_2 (10)}{(100k\Omega)} = 0.025 R_2 \xrightarrow{\text{Value in k}\Omega}$$

$$2.025 = V_G - V_S = 0.025 R_2 - 5$$

$$R_2 = 281 k\Omega.$$

Small Signal \rightarrow Ground DC Voltage Sources.

$$R_1 = 119 k\Omega.$$



$$ter R_i = R_1 || R_2$$

$$R_{in} = R_{Si} + R_i$$

$$\star V_o = g_m V_{gs} (R_s \parallel r_o)$$

$$g_m = 2 \sqrt{k_n I_{DQ}} = 2.45 \text{ mA/V}$$

$$V_o = 2 \sqrt{k_n I_{DQ}} V_{gs} \left(\frac{R_s V_o}{R_s + r_o} \right)$$

$$r_o = \frac{1}{k_n I_{DQ}} = 44.44 \text{ k}\Omega$$

$$= 2.45 V_{gs} \left(\frac{3.33 \times 44.44}{41.71} \right) \checkmark$$

$$= (2.45) V_{gs} (3.091)$$

$$= 7.59 V_{gs}$$

$$\star V_{in} - V_{gs} - V_o \xrightarrow{g_m V_{gs} (R_s \parallel r_o)} = 0$$

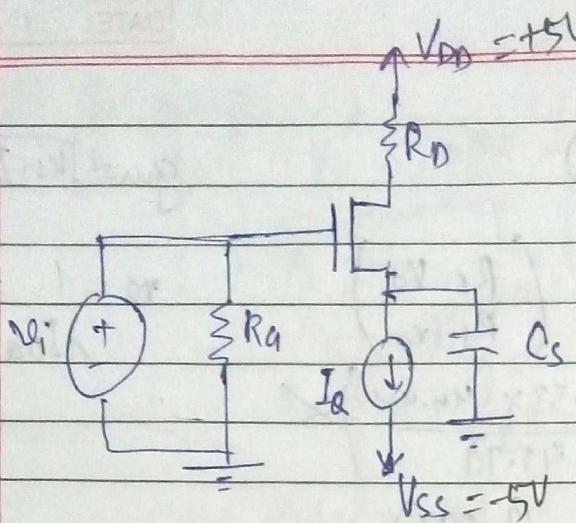
$$\Rightarrow V_{gs} = \frac{V_{in}}{1 + g_m (R_s \parallel r_o)}$$

$$V_{in} = \frac{R_i}{R_s + R_i} V_i$$

$$V_{gs} = \left(\frac{R_i}{R_s + R_i} \right) - \frac{V_i}{1 + g_m (R_s \parallel r_o)}$$

$$\star \frac{A_v \Delta V_o}{V_i} = \frac{g_m (R_s \parallel r_o) \left(\frac{R_i}{R_s + R_i} \right)}{1 + g_m (R_s \parallel r_o)} = 0.884.$$

Q3.



$$R_g = 200k$$

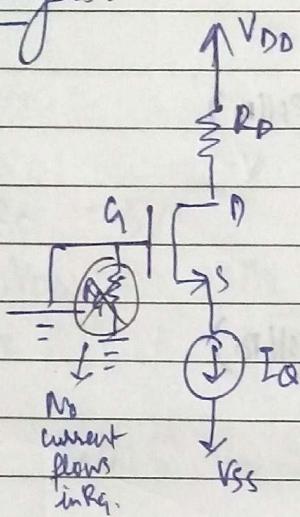
$$R_d = 7k$$

$$I_a = 0.5 \text{ mA} \quad I = 0$$

$$V_{TN} = 0.8 \text{ V} \quad k_n = 1 \mu \text{A/V}^2$$

Find Ans.

Soln:

DC Analysis:-

$$I_{DQ} = I_a = 0.5 \text{ mA}$$

$$V_{DSQ} = -V_S$$

$$I_{DQ} = k_n (V_{DSQ} - V_{TN})^2$$

$$0.5 = 1 (V_{DSQ} - 0.8)^2$$

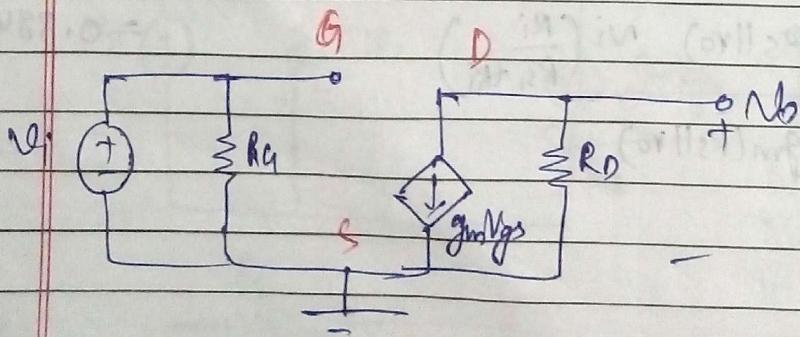
$$V_{DSQ} = \pm \sqrt{0.5} + 0.8$$

$$V_{DSQ} = 1.51 \text{ V.}$$

$$V_{DSQ} = V_{DD} - I_a R_D - V_{DSQ} - (V_S + V_{SS}) = 0.$$

$$V_{DSQ} = V_{DD} - I_a R_D - V_S \\ = 5 - 3.5 + 1.51$$

$$V_{DSQ} = 3.01 \text{ V}$$



$$Av = \frac{V_o}{V_i}$$

Vi

$$V_o = -g_m V_{GS} R_D$$

$$V_i = V_{GS}$$

$$g_m = 2 \sqrt{k_n I_{DQ}} = 2 \sqrt{1 \mu \text{A/V}^2 \cdot 0.5 \text{ mA}} =$$

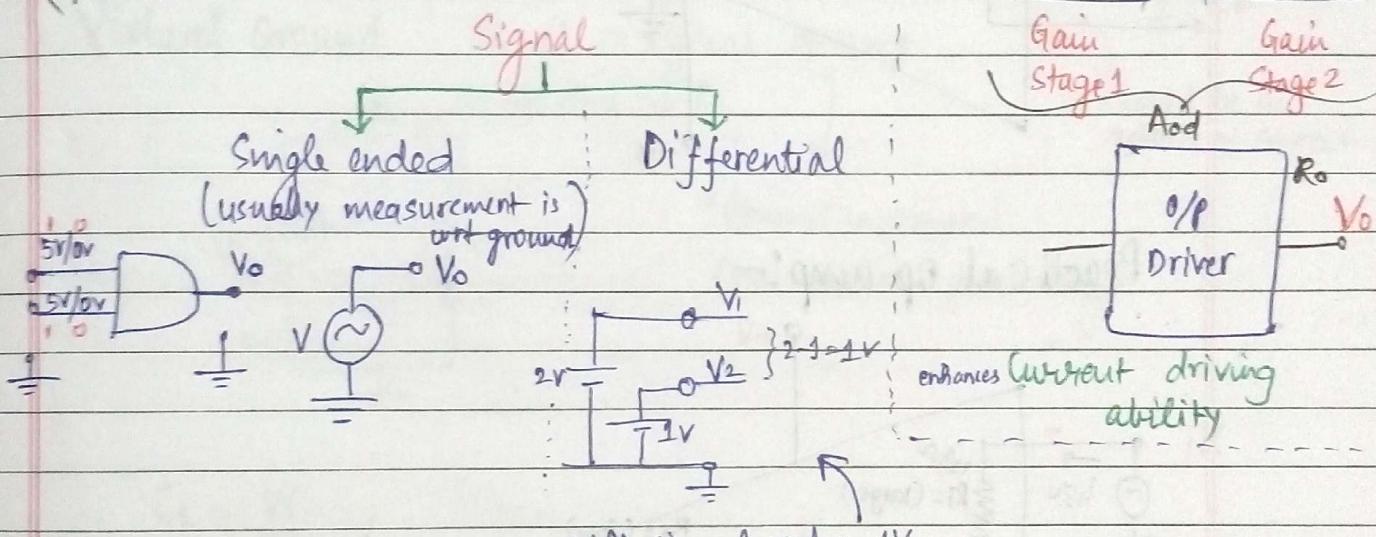
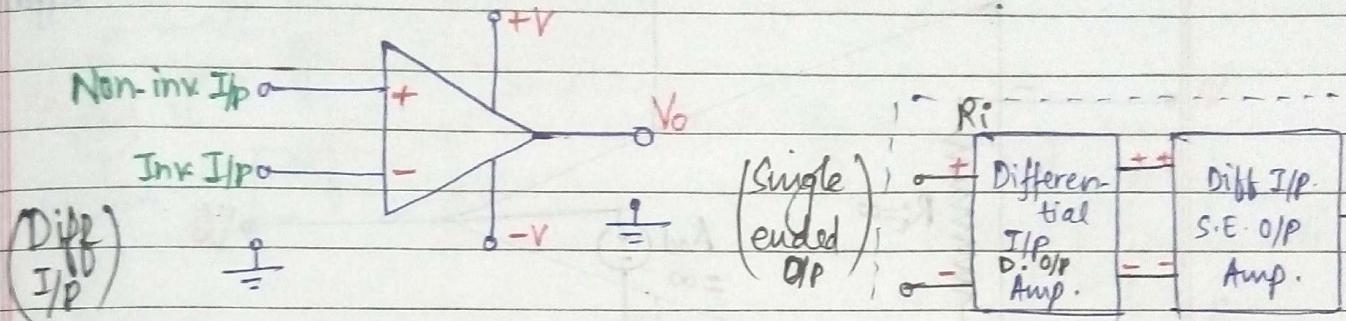
$$\Rightarrow Av = \frac{-g_m R_D V_{GS}}{V_{GS}} = -g_m R_D = -9.9$$

Op-Amps

Operational Amplifiers

(Use MOSFET, BJT, R, Diodes inside)

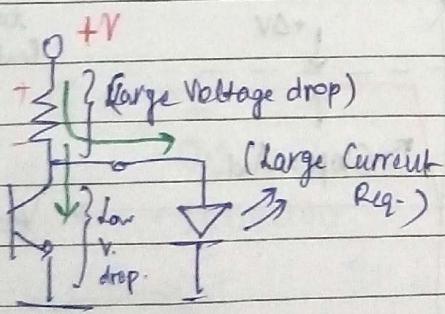
→ V-sensitive component



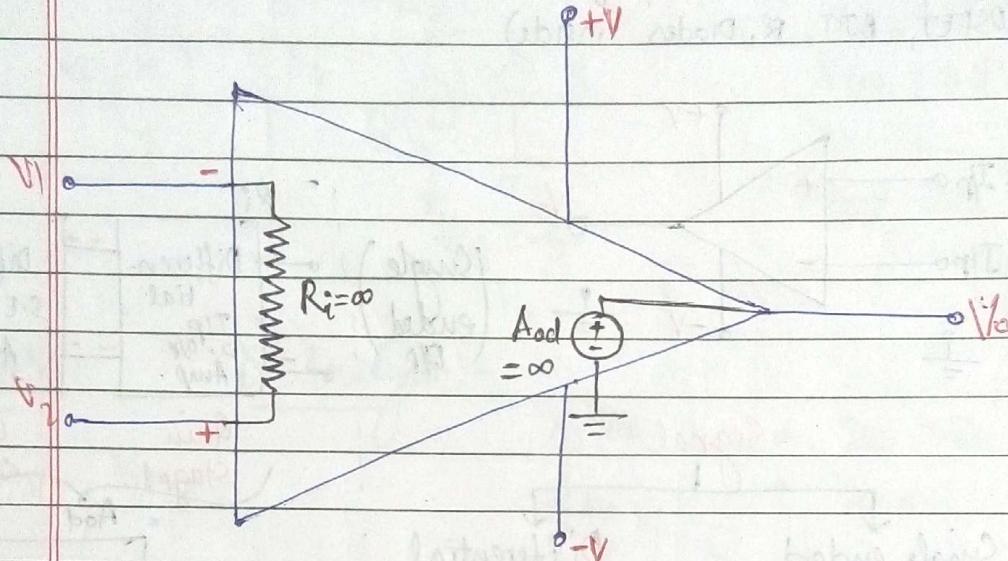
Difff. Signal value = 1V
(Voltage)

but absolute voltages
are diff.

even then, we get
same output!

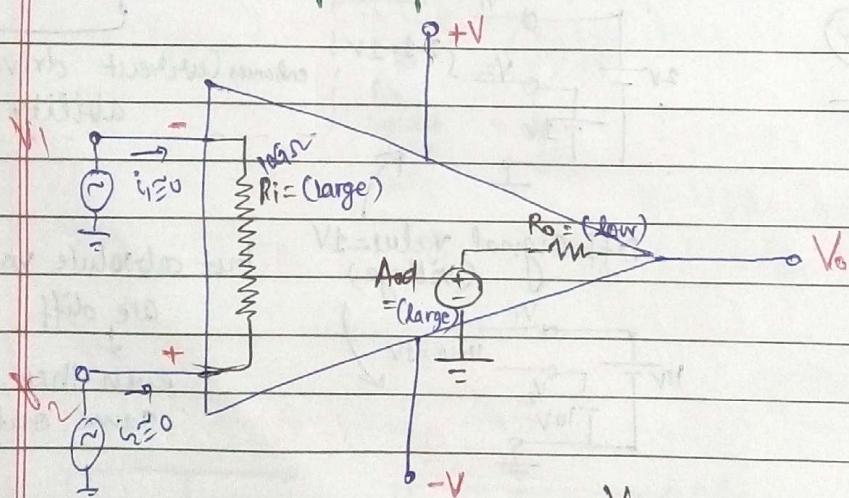


Equiv. ckt and ch. of an ideal op-amp



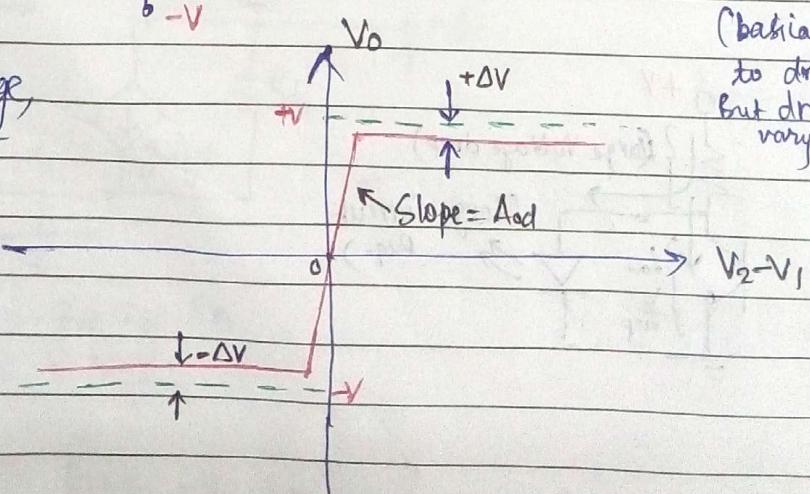
* $A_{od} = \text{Open-Loop Differential Gain}$

Practical op-amp!:-



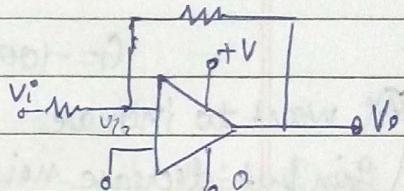
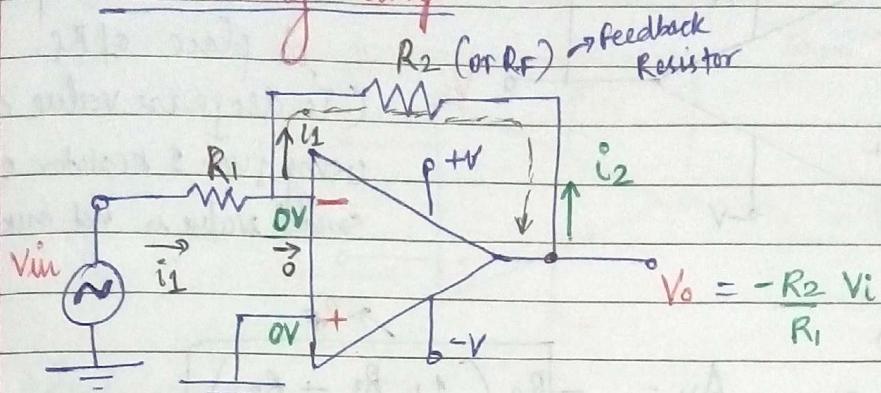
Since R_i is very large,
only negligible current
flows through it
 $\Rightarrow V_{Ri} \approx 0$

$\Delta V = \text{fixed}$
(basically arises due
to drop across R_o)
But drop across R_o may
vary acc. to load.

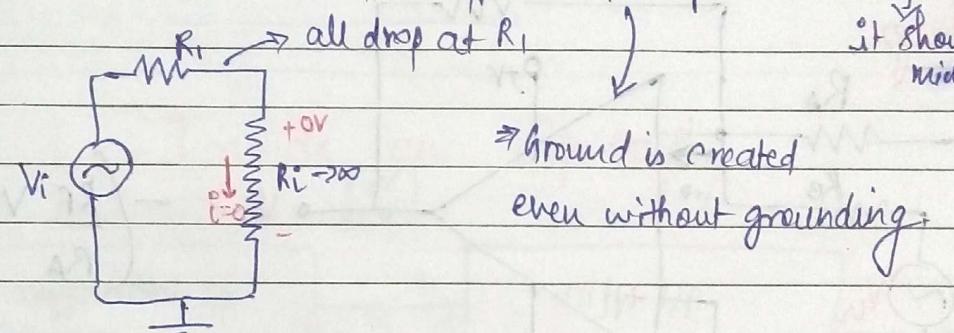


(180°)

Inverting amp



Virtual Ground : Ch. of a typical op-amp.



it should be in middle of source V.

$$i_1 = \frac{V_i}{R_1} \quad \left\{ \text{Taking } 0V \text{ of inv. br as ref.} \right\}$$

$$i_2 = \frac{V_o}{R_2}$$

Clearly, $i_1 = -i_2 \Rightarrow \frac{V_i}{R_1} = -\frac{V_o}{R_2} \Rightarrow \boxed{\frac{V_o}{V_i} = -\frac{R_2}{R_1}} = A_{cl}$ (Closed-loop gain)

$$G = -1$$

$$-0.1$$

$$-1000000$$

20/10/16

Noise

* Thermal Noise

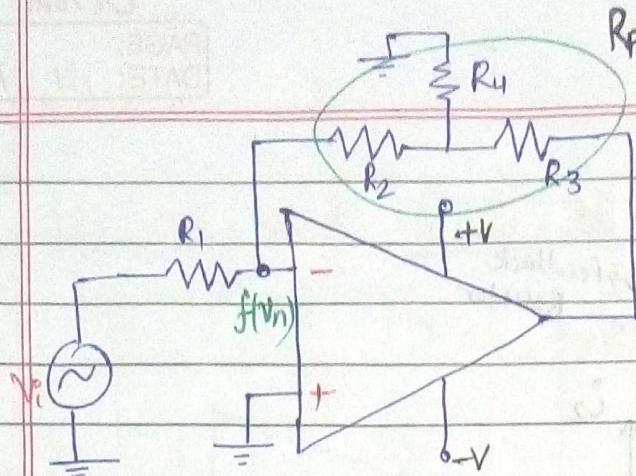
(R)

due to Resistor

$$V_n = \sqrt{4k_B T R_A f} \quad \begin{matrix} \text{abs. Temp(K)} \\ \text{noise Voltage} \\ \text{Band of freq.} \end{matrix}$$

High R is not preferred
ANUBHAU JAIN NOTES

It is not suggested to have high gain ($> 10^6$) using inverting conf.



To decrease noise,
T-network is pre-
in place of R_F .

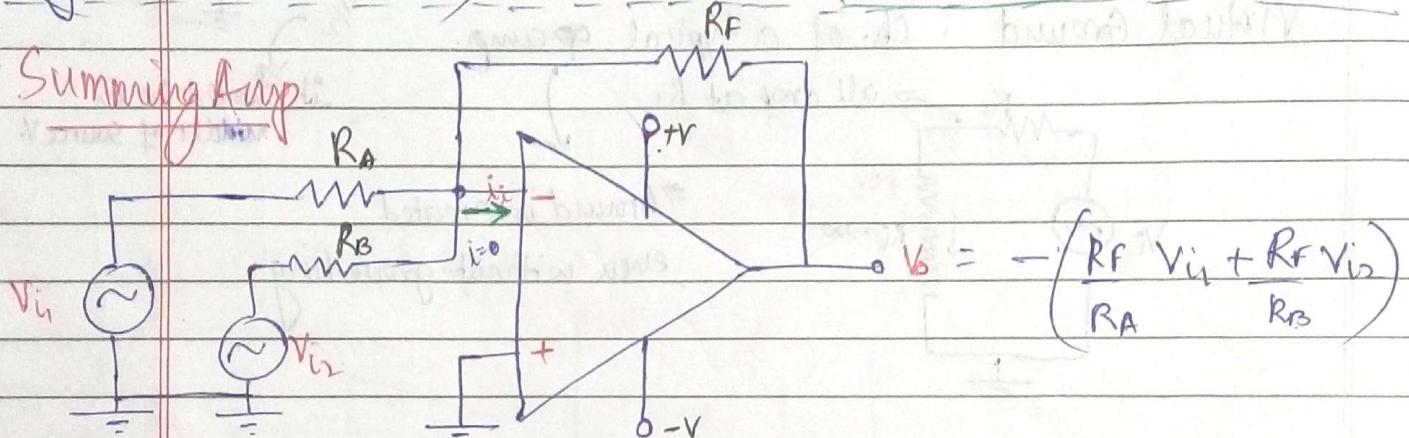
(To decrease value of R_F)
using just 1 resistor of
small value is not much efficient

$$G = -1000$$

We want to increase
(gain but decrease noise)

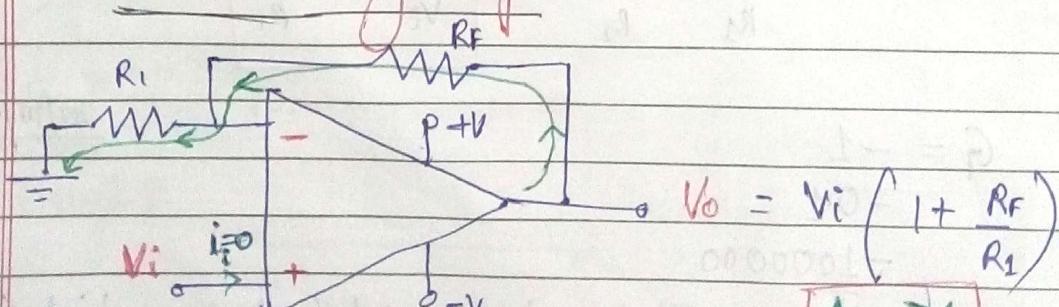
$$A_V = -\frac{R_2}{R_1} \left(1 + \frac{R_3}{R_4} + \frac{R_3}{R_2} \right)$$

Summing Amp.



And, R_i , R_o , I/P Offset current (i_{io}) \rightarrow fA to mA.
 (Good) (Bad)
 $\cdot \mu A, \mu A \checkmark$

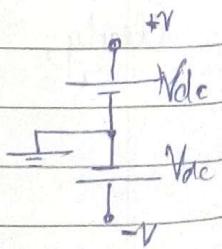
Non-Inverting Amp.



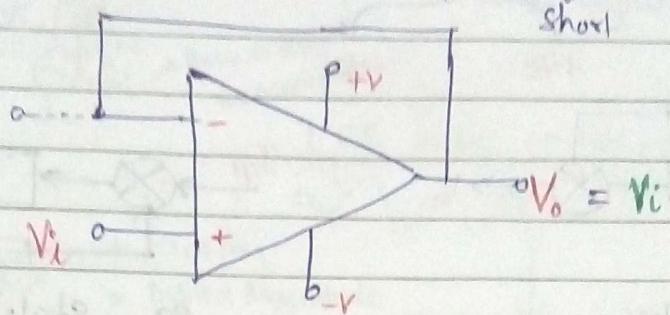
$$[A_V \geq 1]$$

$$\frac{V_o}{V_i} = \frac{R_1 + R_F}{R_1}$$

$$V_i = V_o \frac{R_1}{R_1 + R_F} \Rightarrow \frac{V_o}{V_i} = \frac{R_1 + R_F}{R_1} = 1 + \frac{R_F}{R_1}$$



If we want $A_v = 1$, we can put $R_F = 0$, $R_1 = \infty$.
 Short open.

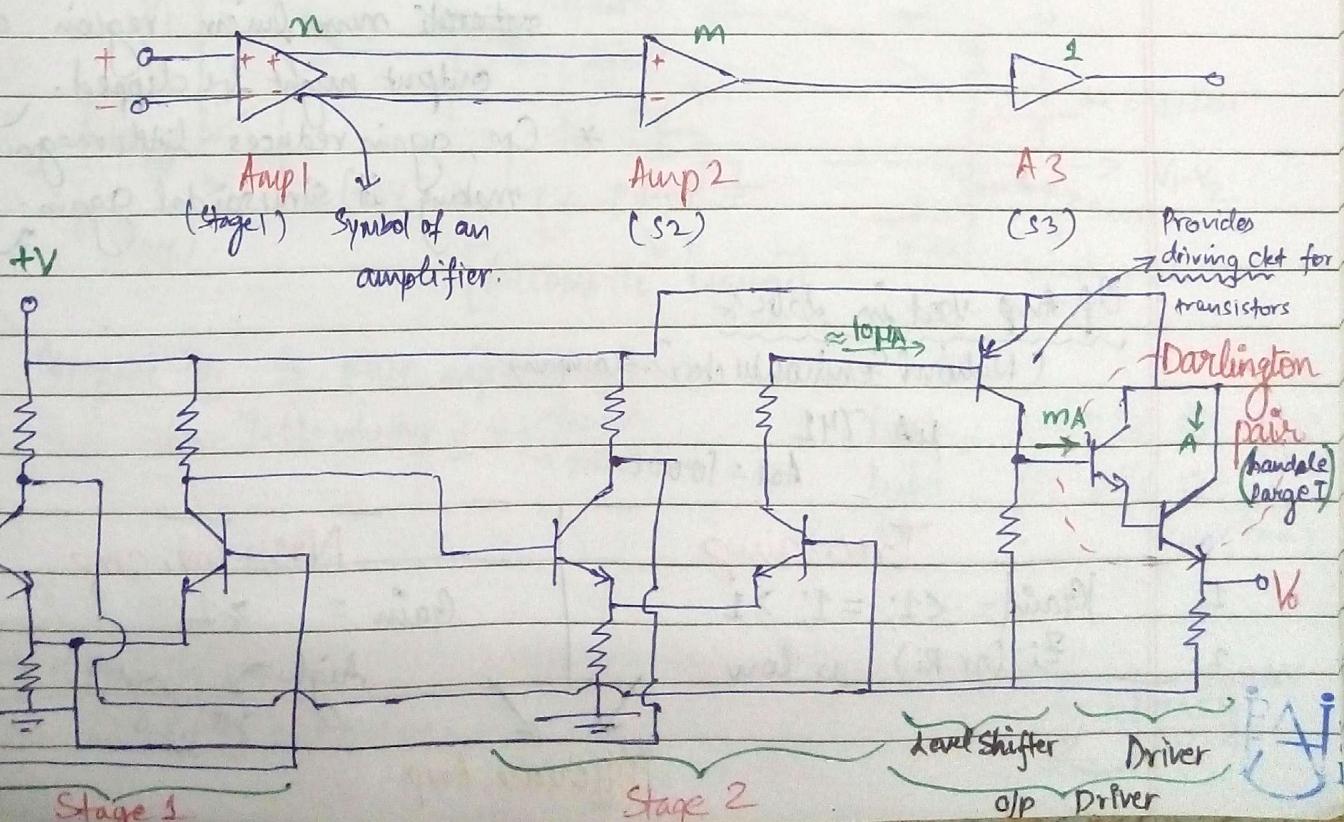
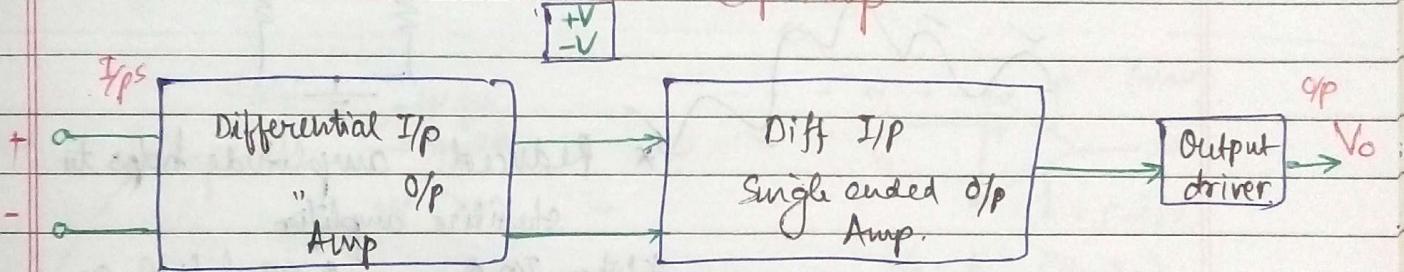


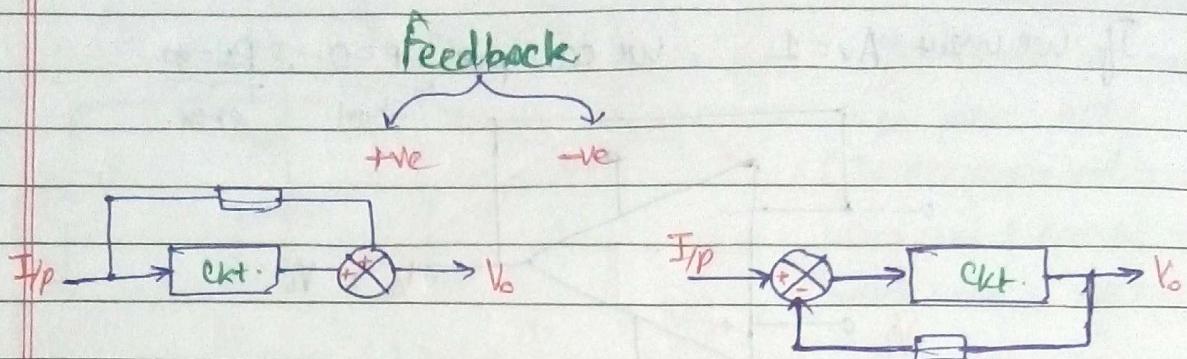
Application:-

In case of Inverting Amp, we can replace V_{in} with this circuit,
 voltage follower
 op-amp.

Inside an Op Amp.

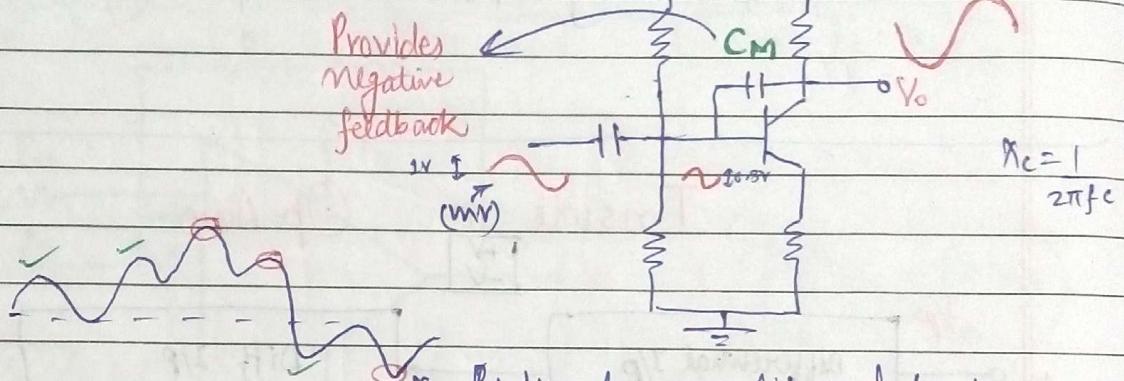
21/10/16.





eg. Oscillator

eg. stabilized Amp.



- * Reduced amplitude helps to stabilize amplifier
- * When I/P rises, the amplifier goes into ~~saturated~~ non-linear region and output might be clipped.
- * C_M again reduces little magnitude, making it sinusoidal again.

Op-amps used in labs:-

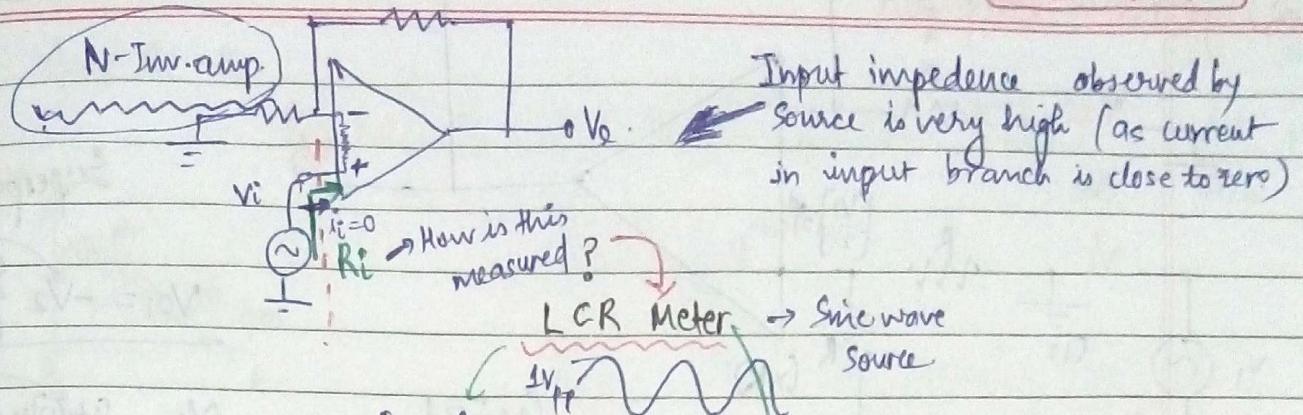
(National Semiconductor) - company

$\mu A 741$

$A_{od} = 10000$

	Inv. amp	Non-inv. amp
1.	$ Gain = <1; = 1; >1$	$Gain = >1$
2.	Z_i (or R_i) is low	high \rightarrow input current $i_{in} \neq 0$

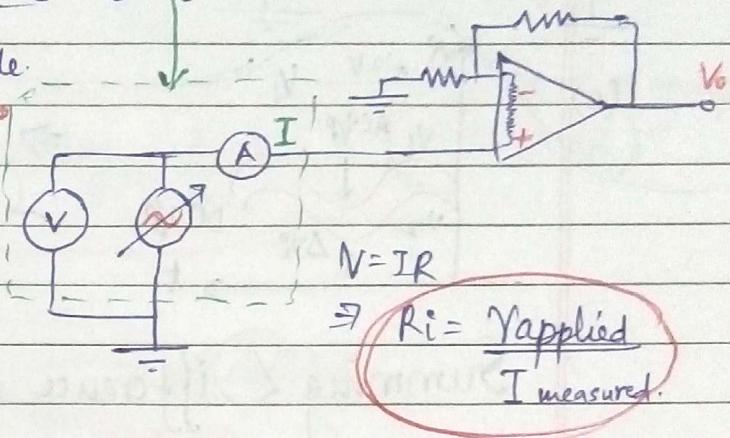
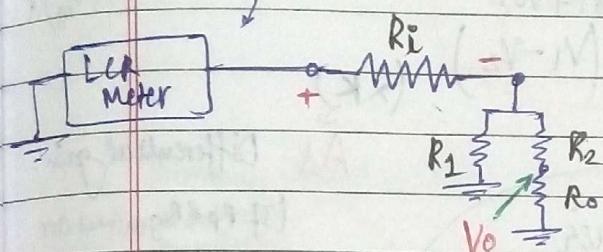
Difference Amp.



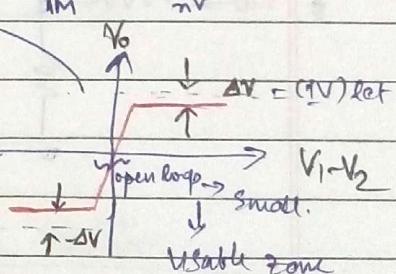
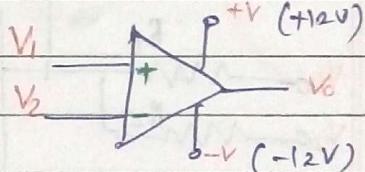
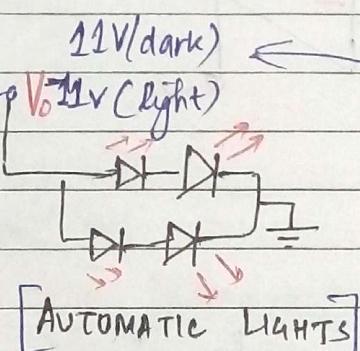
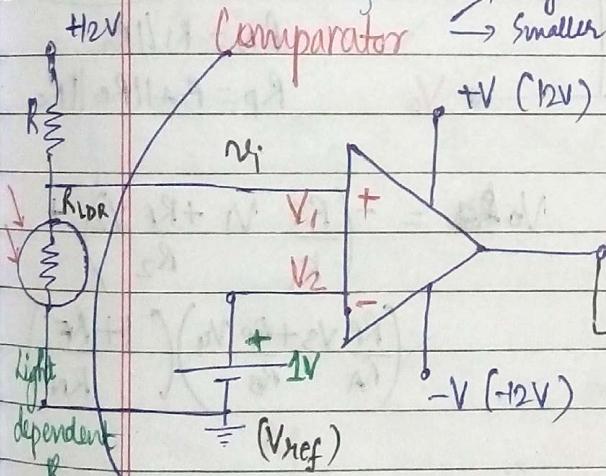
Source Measuring Unit

- * Fixed freq.
- * Desired Magnitude.

Eq. Circ.



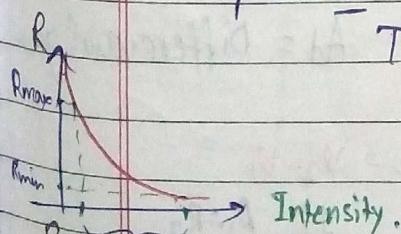
Voltage
Comparator



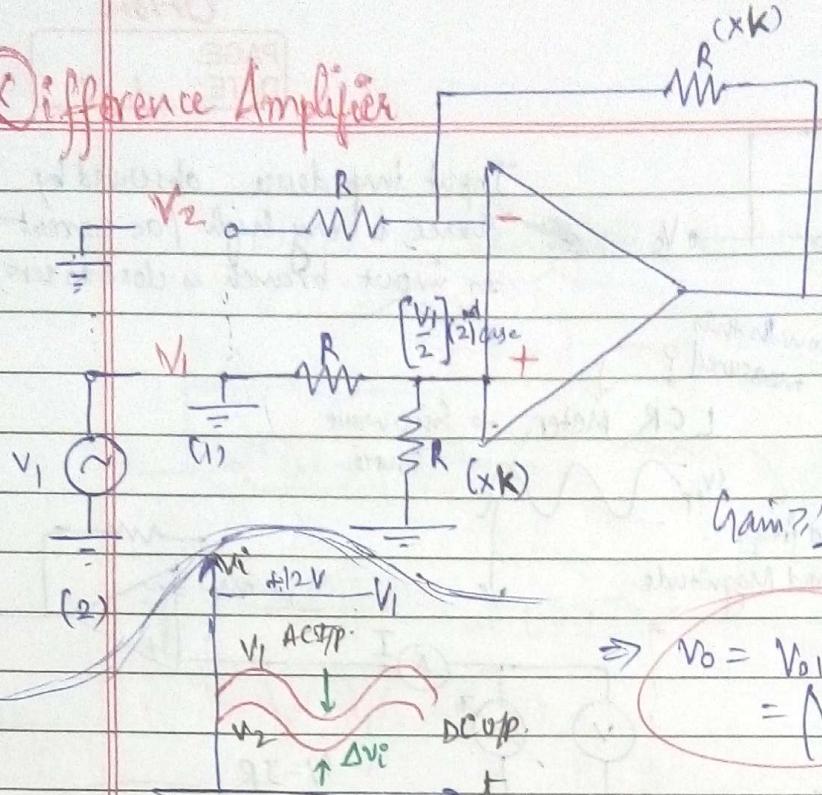
Compare V_i to other input voltage.

Tells whether it is \rightarrow larger
 \rightarrow smaller.

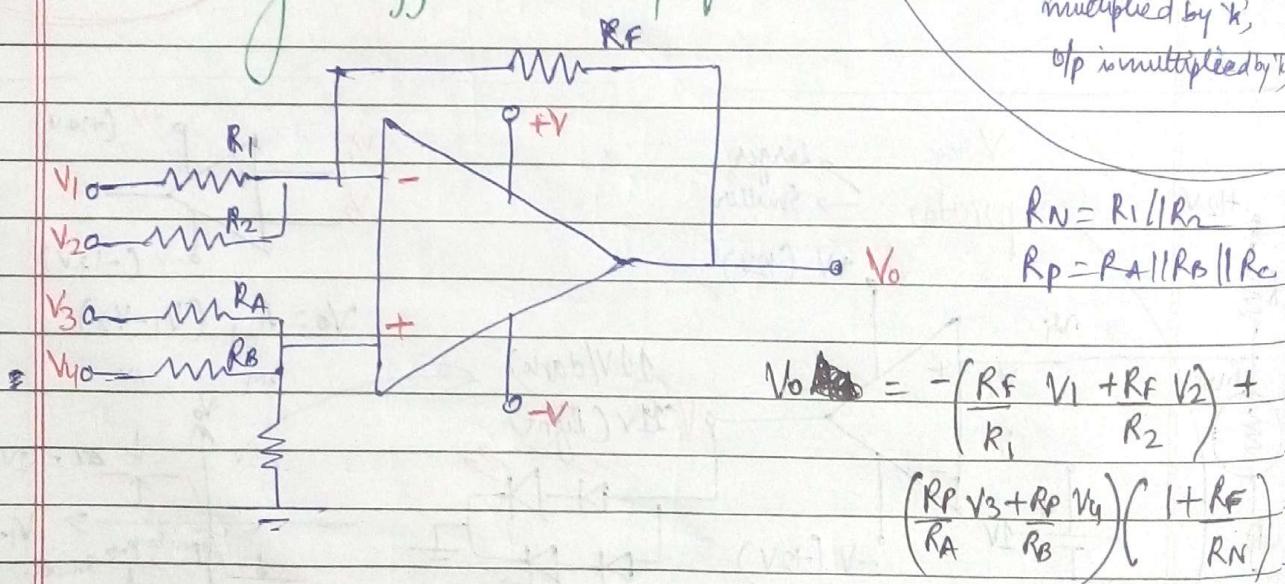
Dark, $V_i > 1V \Rightarrow 1V$ (max)
light, $V_i < -1V \Rightarrow -1V$ (min)



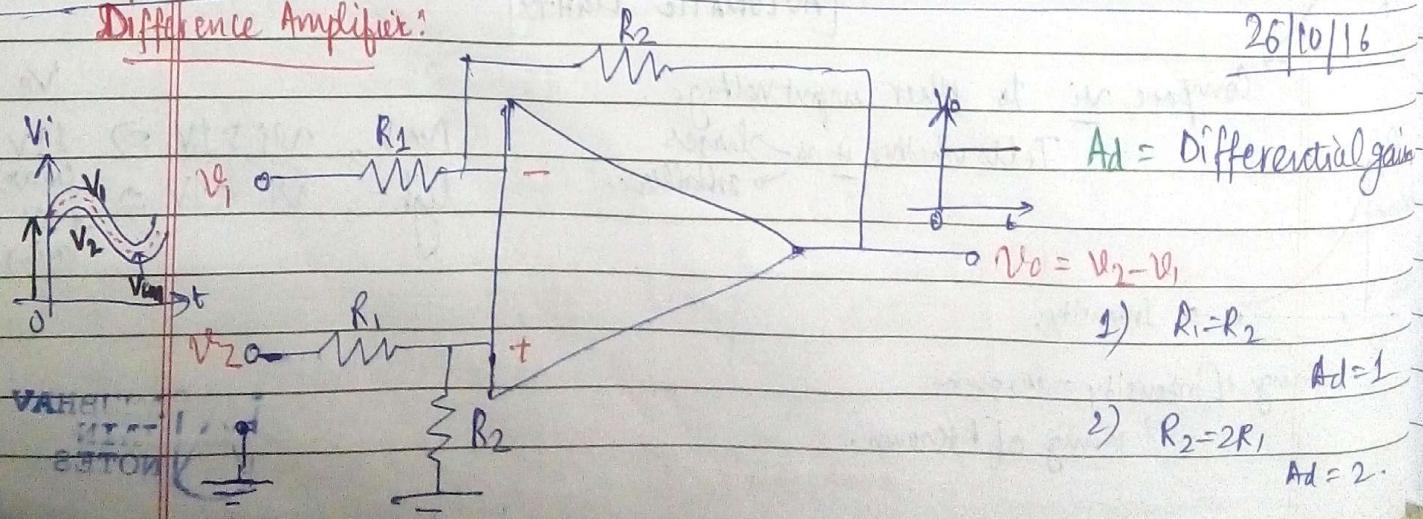
Difference Amplifier



Summing Difference Amplifier



Difference Amplifier:



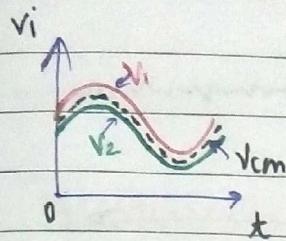
26/10/16

 $Ad = \text{Differential gain}$

Ad, Ri, Ro,

Ideal

$$\text{CMRR (Common Mode Rejection Ratio)} = \frac{Ad}{A_{cm}} = \infty \text{ dB}$$



$$V_{cm} = \frac{V_1 + V_2}{2}$$

$$A_{cm} = \frac{V_0}{V_{cm}}$$

(Common Mode gain)

$\text{CMRR}_{\text{dB}} = 20 \log_{10} \left(\frac{Ad}{A_{cm}} \right) \rightarrow (80 \text{ to } 110 \text{ dB})$

for good practical opamp

Humming sound $\approx 50 \text{ Hz}$

(Both subjected to noise)

(Only one with noise)

230V 50Hz

Aggressor

Noise +V gets amplified

x100 x500

O/P

Victim

electrostatic field lines

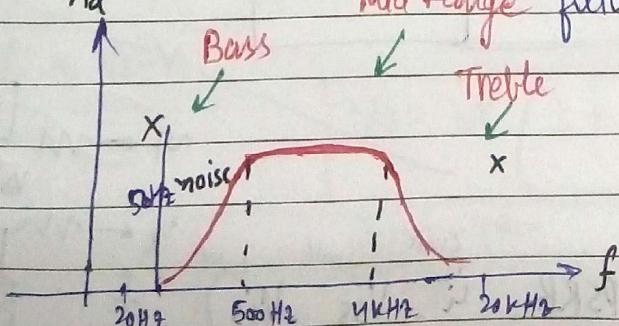
Ad

Mid Range filtered to pass in amplifier.

Bass

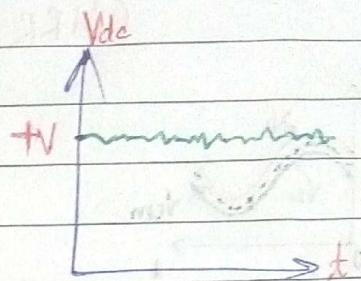
Treble

noise



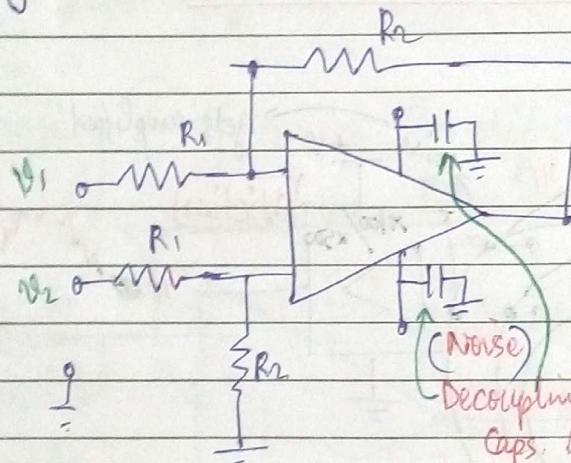
PSRR (Power Supply RR)

Ability of opAmp to reject the noise in power supply.



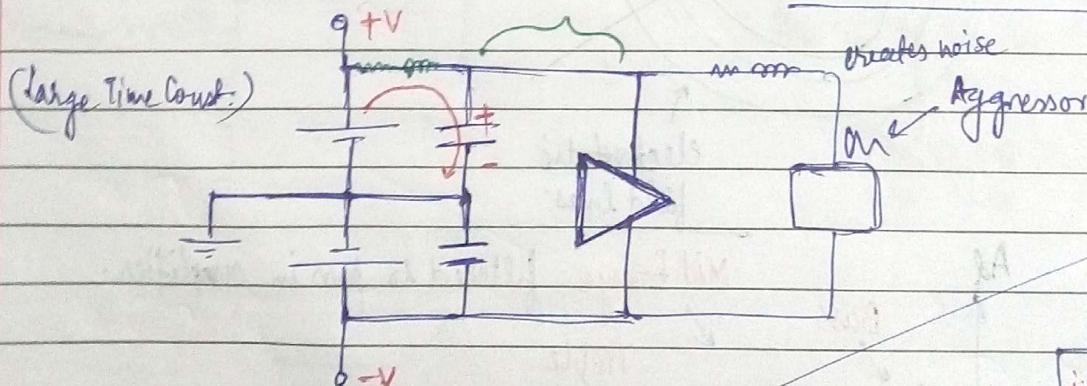
$$\text{PSRR}_{\text{dB}} = 20 \log_{10} \left(\frac{\Delta V_s}{\Delta V_o} \cdot A_v \right)$$

Ideally $\rightarrow \infty$
Practically $\sim 60 \text{ dB}$



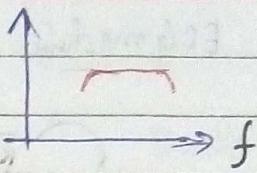
$$V_o = V_1 - V_2$$

Absolute necessity for sensitive circuits.



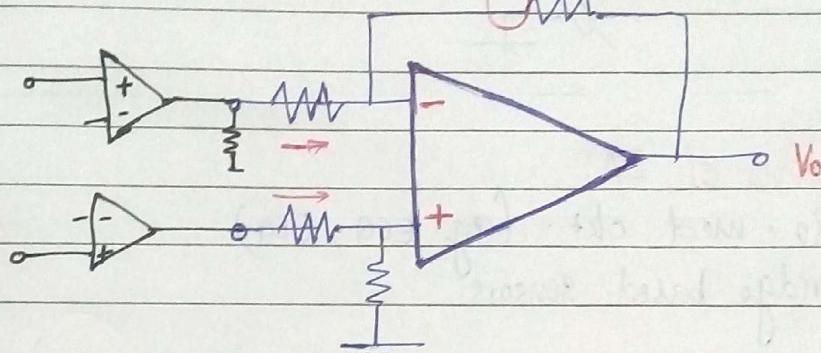
(A_{od} , R_i , R_o , CMRR, PSRR, i_o , V_{os} , V_{is})

$$\begin{aligned} & \text{input offset current} \quad \text{output offset current} \quad \text{input offset} \\ & \downarrow \\ & \left\{ \begin{array}{l} V_b = V_1 - V_2 \\ \text{if } V_1 = V_2, V_b = V_{os} \end{array} \right. \end{aligned}$$

Noise density ($\text{mV}/\sqrt{\text{Hz}}$)

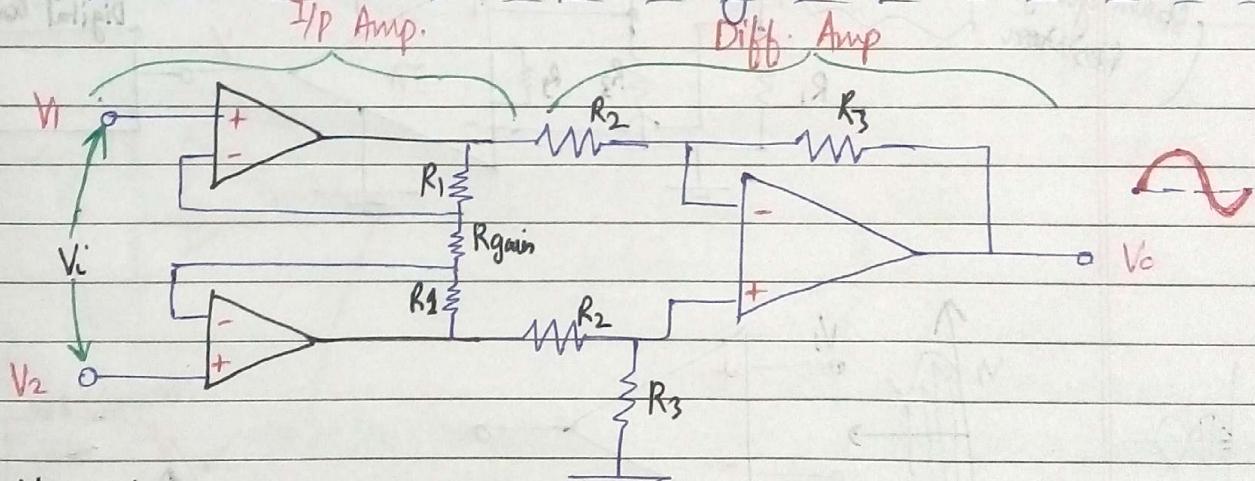
27/10/16

Instrumentation Amp. using Op-amps.



Drawback of difference amp:-

→ Takes current \Rightarrow Source should be strong.



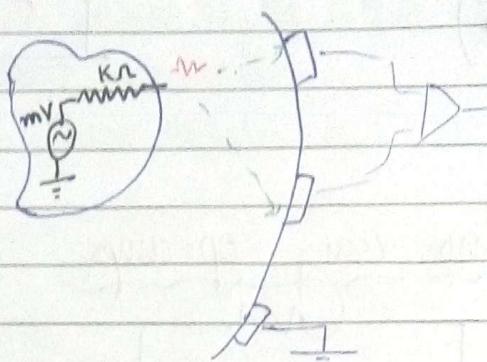
$$V_i = V_2 - V_1$$

$$V_o = V_i \left(1 + \frac{2R_1}{R_{\text{gain}}} \right) \frac{R_3}{R_2}$$

Instrumentation (Op-Amp)	IA	(Diff. Amp) DA
I/P Res.	$R_i = \text{V. high}$	$R_i = \text{low to mid}$
IC fabrication	IC fab	IC fab/Manual
Gain	2-stage (1 to 16,000)	1-stage (1 to 100)
Gain Range	Higher	Lower
Noise		

ECG machine

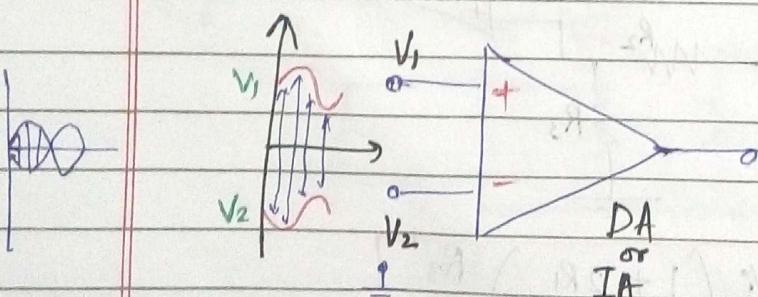
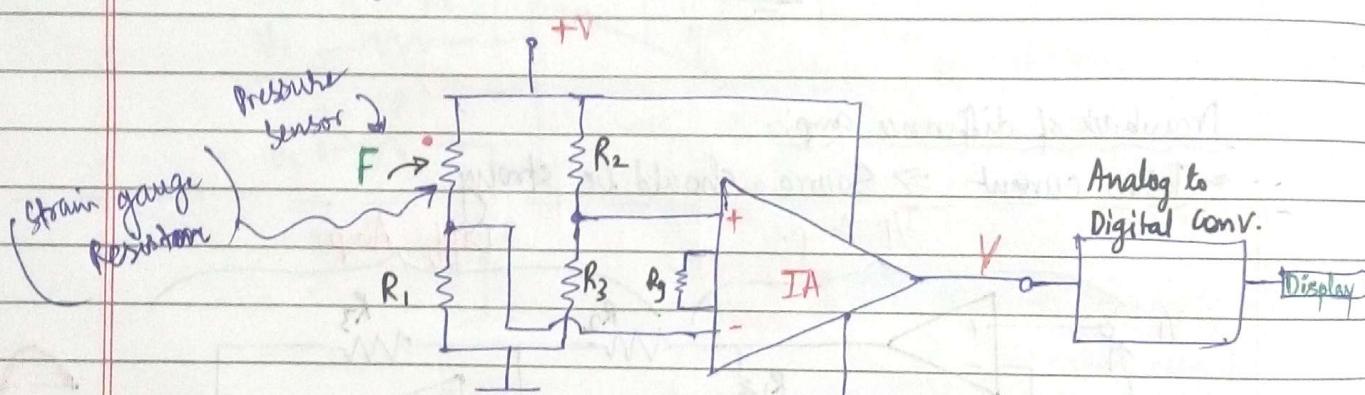
High R \Rightarrow Significant attenuation / loss



INA 128 → TI

Applications of IA:-

1. Bio-med ckt. (eg ECG, EEG)
2. Bridge based sensors.



Truly SIP Differential Signal

$$V_i = V_1 \cup V_2$$

$$N_1 - V_2 = 2R_1 -$$

ВАШИ
ЗАМЕТКИ

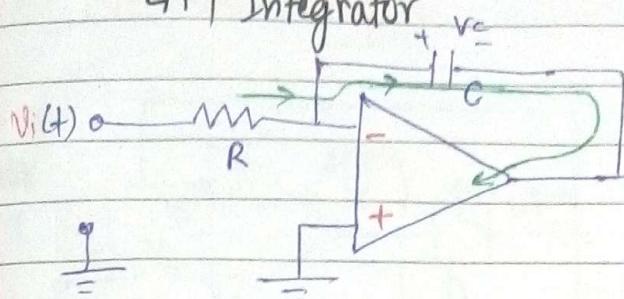
Op-Amp filters.

Op-Amp filters. / Active filters

RC HP filter.

brain + filter

LPF / Integrator

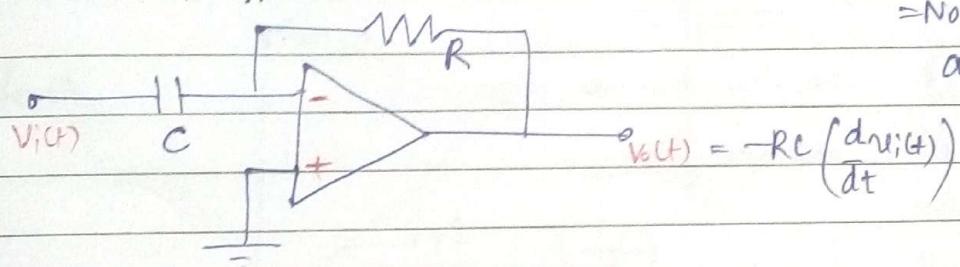


Correction

$$V_c = -\frac{1}{RC} \int V_i(t) dt$$

$$\tau = RC$$

HPF / Differentiator



Order of filter

= No. of Time Constants
available in ch.1st order filters $\rightarrow \tau_1 = RC$.(In all 4 ch. discussed, τ same)

Stage 1

Stage 2

$$\tau_1 = R_1 C_1$$

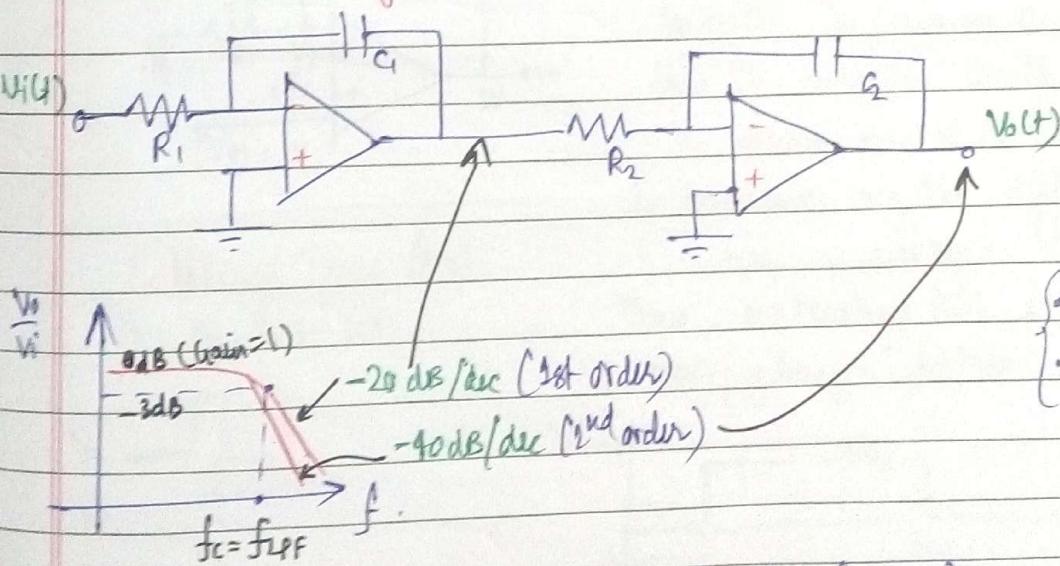
$$\tau_2 = R_2 C_2$$

$$\tau_1 \approx \tau_2$$

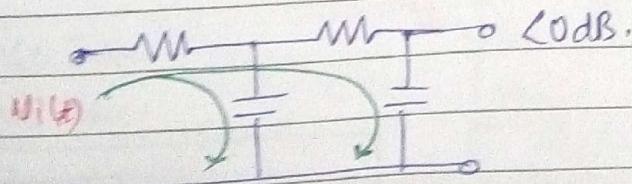
Advantages:

• More opamps

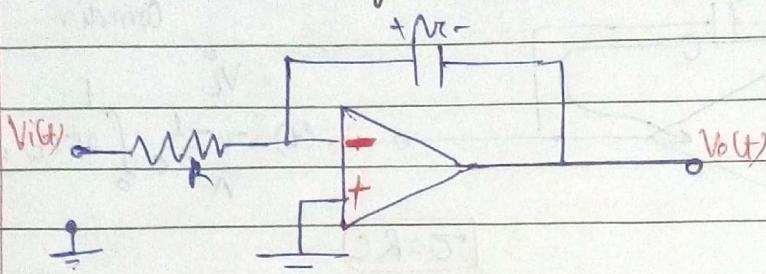
• More power consumed



Why we need active filters?



Correction (LPF/Integrator)

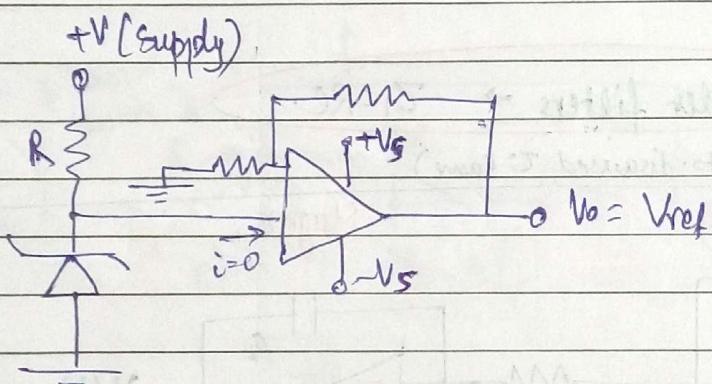


$$V_o(t) = V_c - \frac{1}{RC} \int_0^t V_i(t) dt$$

Voltage Reference Generator

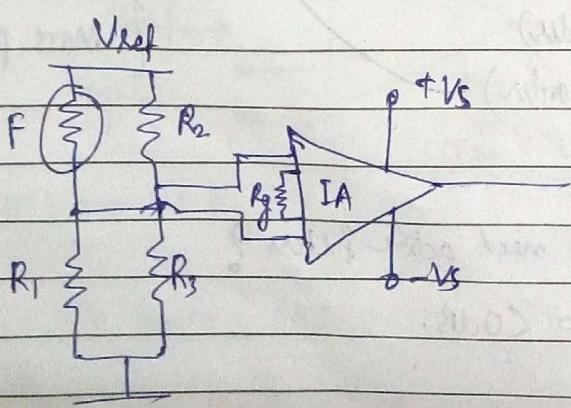
(DC Voltage generator) ($\pm 1\%$ to 5%)

- Higher accuracy (than V_r-generator) ($\pm 0.1\%$)
- Lower o/p Current Sinking/Sourcing ability.



(One can get a required voltage by adjusting the gain)

Voltage Regulator using diode circuit + Non inverting op-amp



Op-Amp Circs.

Linear

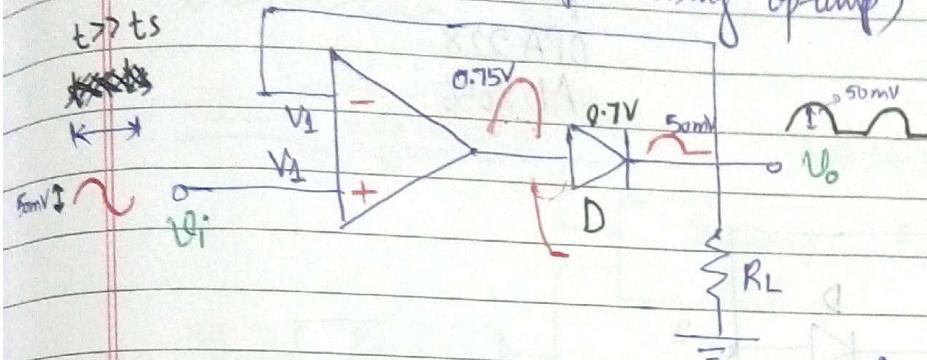
Non-linear

Precision Rectifier

(Active Rectifier using op-amp)

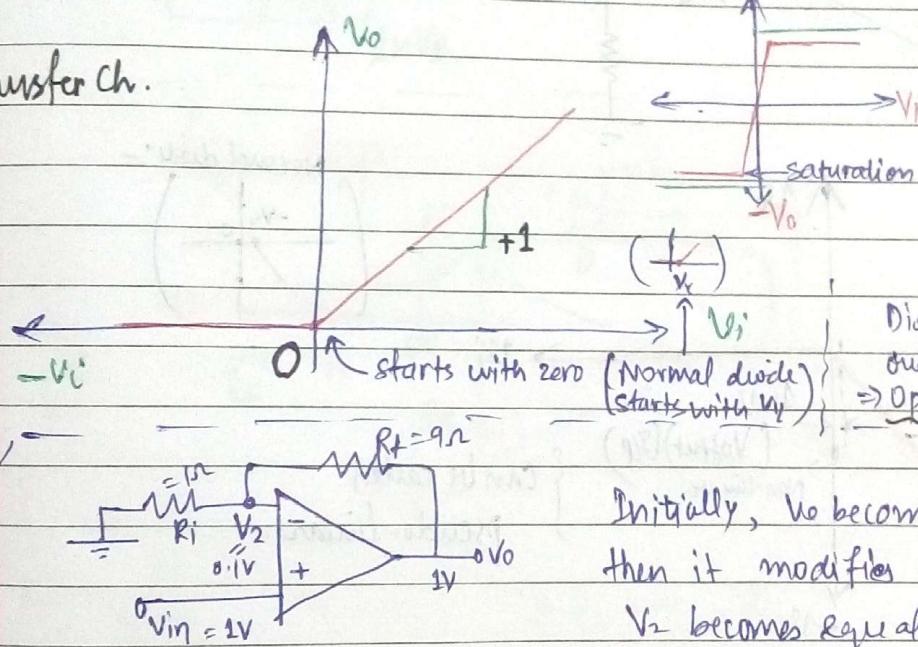
{ Diode: $V_D = 0.7V$.

$\therefore V_{in} > 0.7V$ for conduction}



- V_o is adjusted in such a way that both O/P voltages become equal.
- ⇒ O/P automatically becomes $V_i + 0.7V$. (for si diode)

Transfer Ch.



In negative half cycle,
O/P at opamp tries to
increase its magnitude
(Give) but reaches saturation.

Diode being Rev. biased has no effect,
output V_o remains 0.
⇒ Opamp fails to maintain input
voltages equal.

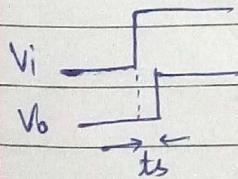
Initially, V_o becomes equal to V_{in} ,
then it modifies itself such that
 V_2 becomes equal to V_{in}

In this case, V_o Yes still V_2 becomes 1V.
till 10V. (happens in t_s time)

Settling Time (t_s)

ps - ns - μ s.

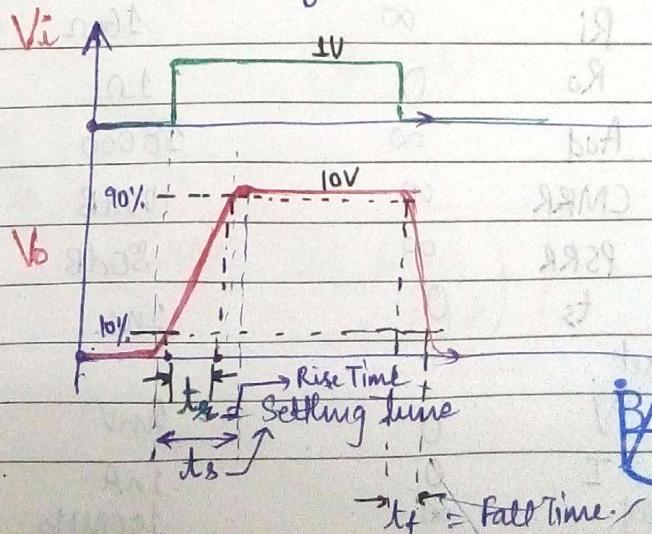
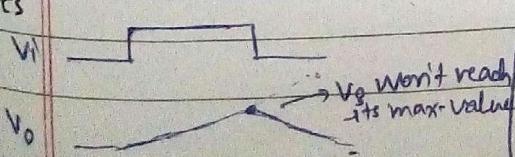
Then, on reaching 10V, it stabilizes, do
not change further.



* Rise Time

* fall Time.

not
presented
if tects

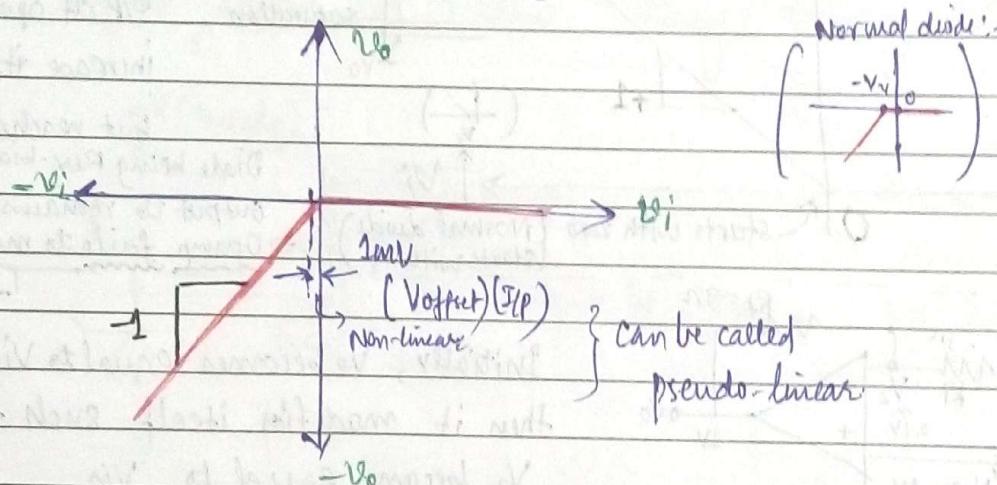
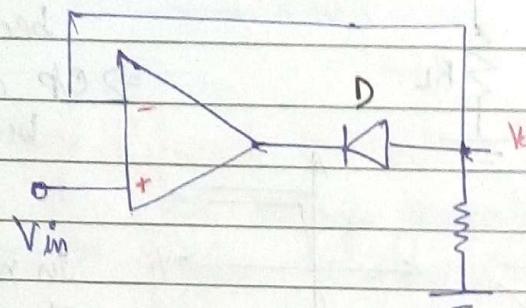


Gain Bandwidth Product
GBW (Speed) (performance) \rightarrow related to t_s .

μA741

OPA228

AD8656



Op Amp Ch.

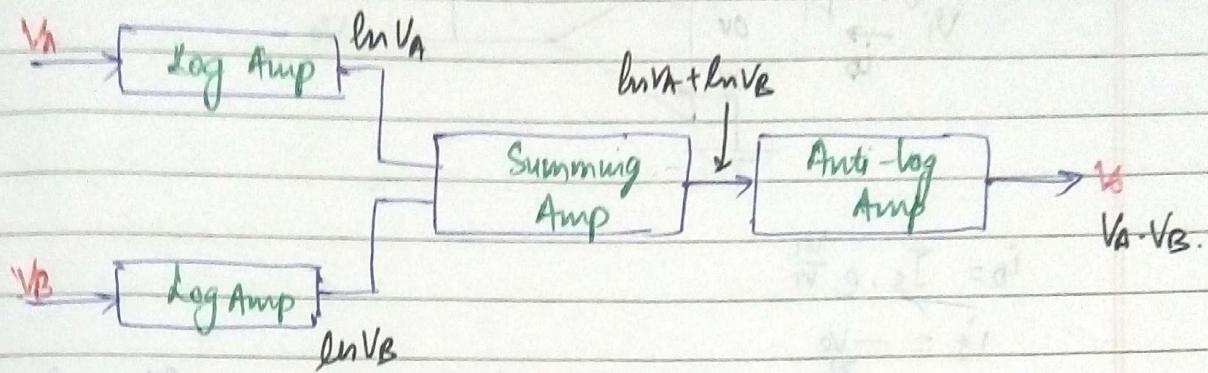
Ideal Practical

R_i	∞	$1G\Omega$
R_o	0	1Ω
A_{od}	∞	10000
CMRR	∞	100dB
PSRR	∞	80dB
t_s	0	1ns.

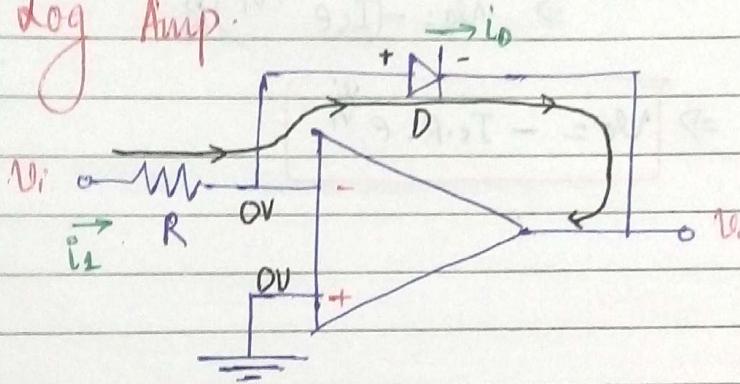
D/P offset

V	0	1mV
I	0	1nA
freq / Speed	∞	100MHz

- * Vadder \rightarrow Summing amp
- * V subtractor \rightarrow Diff. amp or IA.
- * V Multiplier:-



Log Amp.



$$\textcircled{1} \quad i_D = \frac{V_i}{R}$$

$$\textcircled{2} \quad i_D = I_s (e^{\frac{V_o}{V_T}} - 1)$$

$$\textcircled{3} \quad V_T = \frac{kT}{e} = 26 \text{ mV} @ 27^\circ\text{C}$$

$$\Rightarrow i_D \approx I_s e^{\frac{V_o}{V_T}}$$

$$\textcircled{4} \quad \eta = 1 \text{ or } 2$$

$$\text{Also, } i_D = i_o$$

$$\frac{V_i}{R} = I_s e^{\frac{V_o}{V_T}}$$

$$\Rightarrow \frac{V_i}{R \cdot I_s} = e^{-\frac{V_o}{V_T}}$$

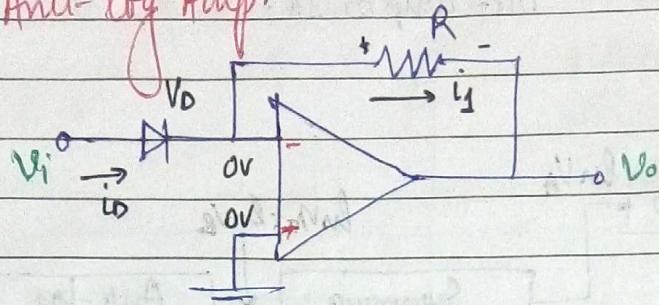
Take ln

$$\ln\left(\frac{V_i}{R \cdot I_s}\right) = -\frac{V_o}{V_T}$$

$$(V_D = -V_o)$$

$$\Rightarrow V_o = -V_T \ln\left(\frac{V_i}{I_s \cdot R}\right)$$

Anti-log Amp.



$$i_D = I_s \cdot e^{\frac{V_i}{V_T}}$$

$$i_I = -\frac{V_o}{R}$$

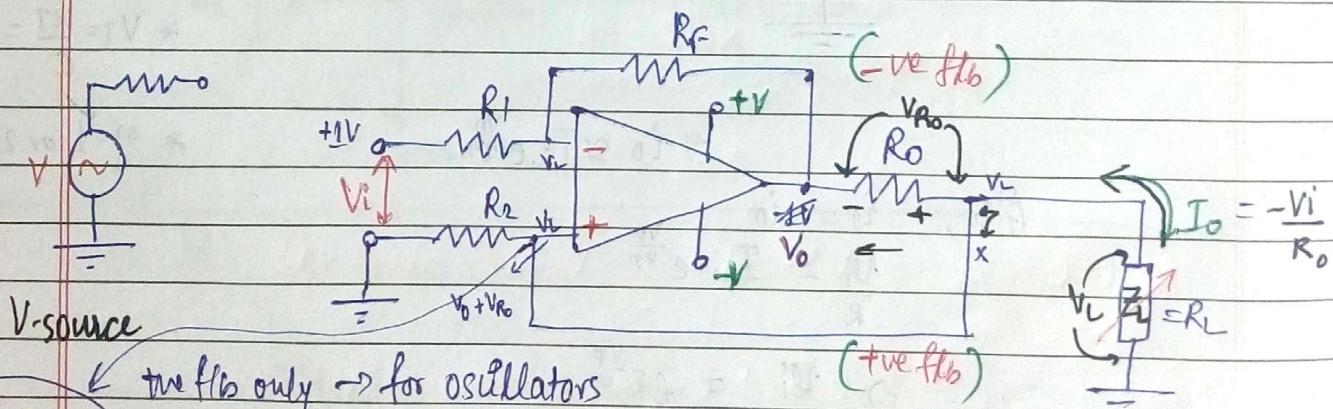
$$\Rightarrow V_o = -i_I R \quad (i_I = i_D)$$

$$\Rightarrow V_o = -\left(I_s e^{\frac{V_i}{V_T}}\right) R$$

$$\Rightarrow V_o = -I_s \cdot R \cdot e^{\frac{V_i}{V_T}}$$

02/11/16

V-I converter

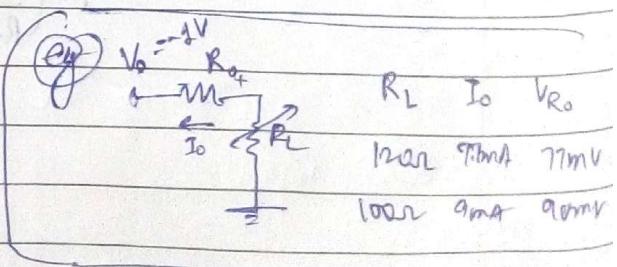
the f/b only \rightarrow for oscillators

$$R_1 = R_2 = R_f = \text{large value}$$

(So that no current in +ve f/b)

R_o = small value.

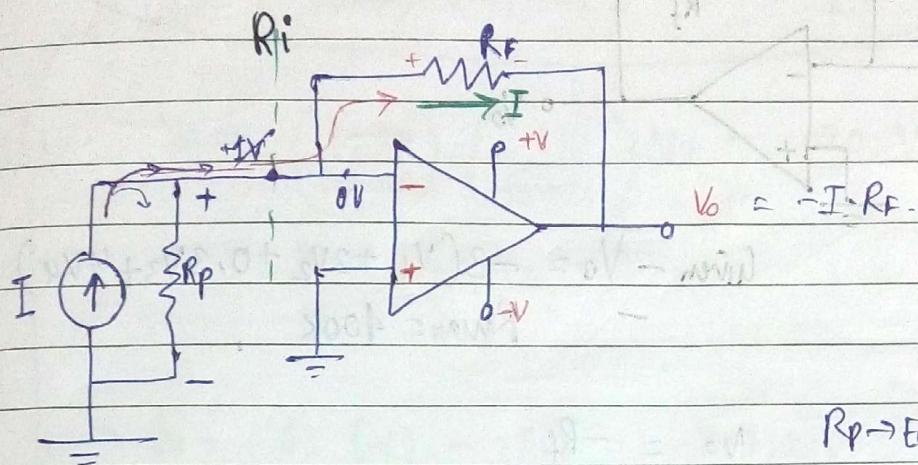
$$R_L \uparrow \rightarrow I_o \downarrow V_{R_o} \downarrow$$



Will come back tomorrow :P

Stay tuned!

I-V Converter

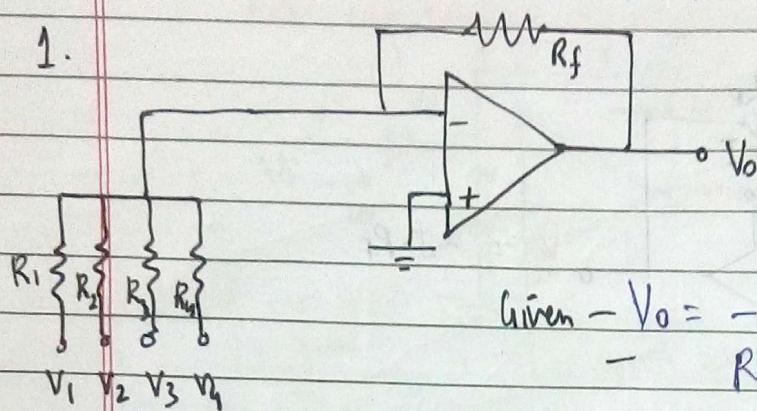


$$R_f = R_p = M \Omega$$

$R_p \rightarrow$ Eq. Resistance (Not Physical Resistance).

Tut on OpAmp.

1.



$$\text{Given} - V_0 = -3(V_1 + 2V_2 + 0.3V_3 + 4V_4)$$

- $R_{\max} = 400k$

$$V_o = -R_f$$

$$V_i \quad R_i$$

$$\rightarrow \frac{R_f}{R_1} = 3 \quad \frac{R_f}{R_2} = 6 \quad \frac{R_f}{R_3} = 0.9 \quad \frac{R_f}{R_4} = 12$$

$$\rightarrow \frac{R_1}{3} = R_f \quad R_2 = \frac{R_f}{6} \quad R_3 = \frac{10}{9} R_f \quad R_4 = \frac{R_f}{12}$$

Max-Resistance

$$\Rightarrow R_3 = R_{\max} = 400k = \frac{10}{9} R_f$$

$$\Rightarrow R_f = 360k$$

$$R_1 = 120k$$

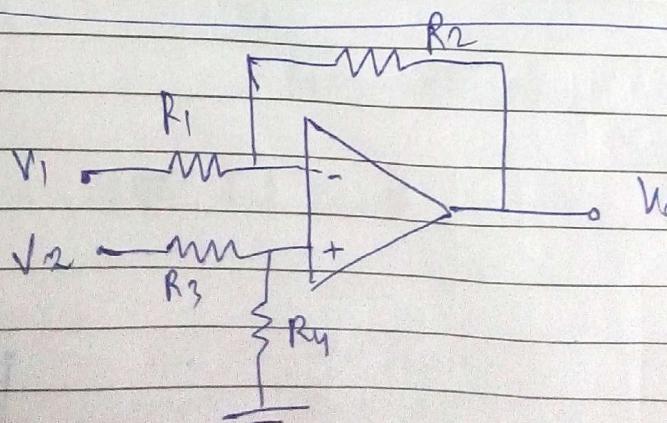
$$R_2 = 60k$$

$$R_4 = 30k$$

$$\text{Given} - V_1 = 0.1V \quad V_2 = -0.2V \quad V_3 = -1V \quad V_4 = 0.05V$$

$$V_o = -3(0.1 - 0.4 - 0.3 + 0.2) = +1.2V$$

2.



$$R_1 = R_2 = 10k$$

$$R_3 = 20k \quad R_4 = 21k$$

$$(a) V_o = ?$$

where (i) $V_1 = 1V, V_2 = -1V$

$$(ii) V_1 = V_2 = 1V$$

$$(iii) A_{vM}, CMRR (dB)$$

$$V_o = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_4}{R_3 + R_4}\right) V_2 - \frac{R_2}{R_1} V_1$$

(i) $V_o = \left(1 + \frac{20}{10}\right) \left(\frac{21}{10+21}\right) V_2 - \frac{20}{10} V_1$

$$V_o = \frac{63}{31} V_2 - 2 V_1$$

$$\rightarrow V_o = \frac{63}{31} (+) - 2(1) = -4.032 V$$

(ii) $V_2 = V_1 = 1V$

$$V_o = \frac{63}{31} - 2 = 0.03 V$$

(iii) $A_{CM} = \frac{V_o}{V_{CM}} = \frac{0.03}{1} = 0.03$

$$V_{CM} = \frac{1+1}{2} = 1$$

V_{CM} \rightarrow Common Mode
 \downarrow
 $V_1 \rightarrow 1V$
 $V_2 \rightarrow 1V$

$$\frac{V_1 + V_2}{2} \quad \begin{matrix} \text{Common mode voltage} \\ \text{of } V_1 \text{ & } V_2 \end{matrix} \quad \begin{matrix} \text{Differential gain} \\ \text{of differential pair} \end{matrix}$$

$$CMRR = 20 \log_{10} \left(\frac{A_d}{A_{CM}} \right)$$

$$A_d = \frac{V_o (i)}{V_d} = -4.03 \times \frac{1}{1} = -4.03$$

$$V_d = \frac{V_1 - V_2}{2} = \frac{(-)(-)}{2} = 1$$

$$CMRR = 20 \log_{10} \left(\frac{-4.03}{0.03} \right)$$

$$V_1 = V_{CM} - \frac{V_d}{2}$$

$$V_2 = V_{CM} + \frac{V_d}{2}$$

$$\frac{V_d}{2} = V_2 - V_1$$

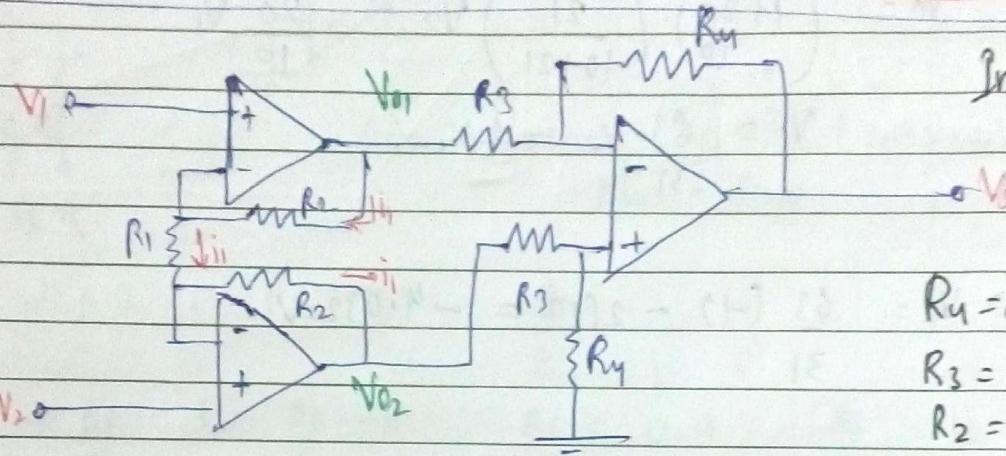
~~$$V_o = A_{CM} V_{CM} + A_d V_d$$~~

$$\frac{63}{21} V_2 - 2 V_1 = (A_{CM}) \left(\frac{V_1 + V_2}{2} \right) + A_d (V_2 - V_1)$$

$$A_{CM} = 0.03 \quad \Rightarrow \quad \frac{63}{21} = A_{CM} - A_d \quad (-2 = \frac{A_{CM}}{2} + A_d)$$

$$\text{CMRR} = 20 \log_{10} \left(\frac{A_d}{A_{an}} \right) = 20 \log_{10} \left(\frac{4.03}{0.03} \right) \approx 35.9 \text{ dB.}$$

3.



Instru Amp.

$$R_4 = 90\text{k}$$

$$R_3 = 30\text{k}$$

$$R_2 = 50\text{k}$$

 $R_1 \rightarrow \text{combination.}$

$$(a) \text{ Range of } A_d \quad \left. \begin{array}{l} R_1 = \\ \qquad \qquad \qquad \left. \begin{array}{l} 2k = R_{fix} \\ 100k = R_{pot} \end{array} \right. \end{array} \right\}$$

$$\left. \begin{array}{l} R_{fix} = 2k \\ R_{pot} = 100k \\ \text{series} \end{array} \right\}$$

(b) Determine $I_{max.}$ in R_1 .HP range $\rightarrow -25\text{mV}$ to $+25\text{mV}$

$$\left. \begin{array}{l} V_{01} = V_1 + i_1 R_2 \\ V_{02} = V_2 - i_1 R_2 \\ i_1 = \frac{V_1 - V_2}{R_1} \end{array} \right\} V_o = \frac{R_y}{R_3} \left(1 + \frac{2R_2}{R_1} \right) (V_2 - V_1)$$

(i) Diff gain A_d

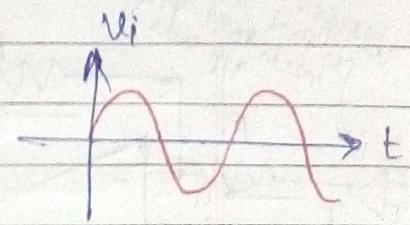
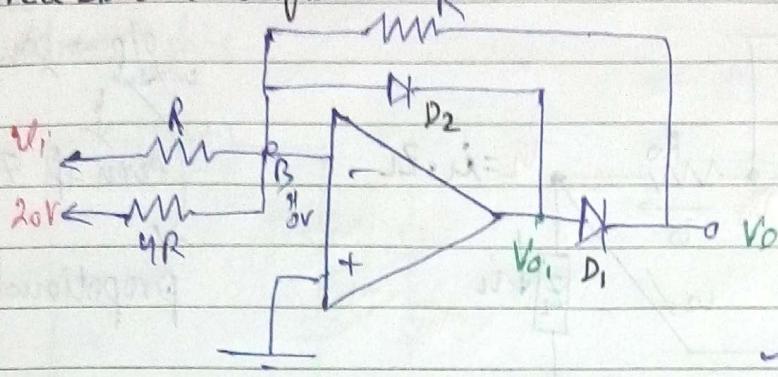
$$R_1 = R_{fix} = 2k \quad A_{d1} = \frac{V_o}{V_2 - V_1} = \frac{R_y}{R_3} \left(1 + \frac{2R_2}{R_1} \right) = \frac{90}{30} \left(1 + \frac{2 \times 50}{2} \right) = 153$$

$$R_1 = R_{fix} + R_{pot \ max} = 102k \quad A_{d2} = \frac{R_y}{R_3} \left(1 + \frac{2R_2}{R_1} \right) = \frac{90}{30} \left(1 + \frac{2 \times 50}{102} \right) = 5.2 \text{ (out of range)}$$

$$i_1 = \frac{V_1 - V_2}{R} = \frac{25 - (-25)}{2k} = 25\text{mA}$$

4.

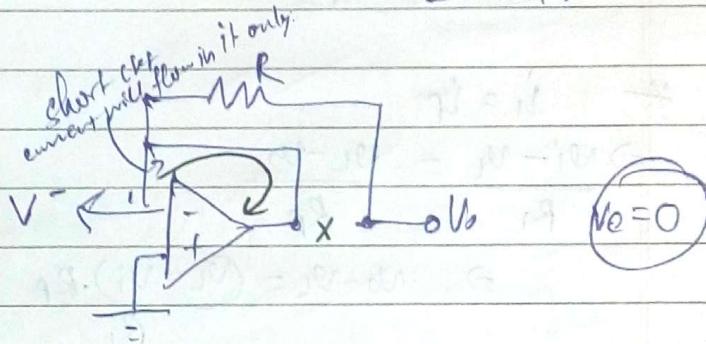
Precision Rectifier:-



+ve half cycle $\rightarrow D_2 \text{ is}$

$$\begin{aligned} V_d &= A(V^+ - V^-) \\ &= -AV^- \end{aligned}$$

$$(i) V_{d1} = -AV^-$$



$$(ii) V_d = -V-$$

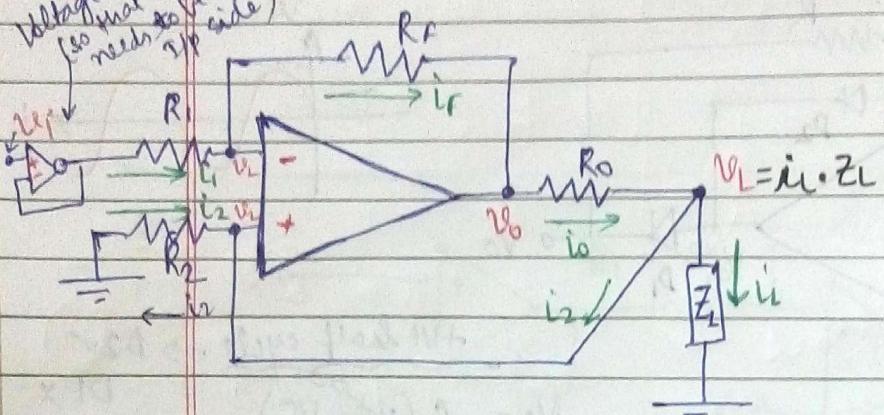
$$V_d = -A(-V^-) = AV^+$$

$D_2 \times D_1 \text{ is}$

$$\frac{0 - 20}{UR} + \frac{0 - V_i}{R} + \frac{0 - V_o}{R} = 0$$

$$V_o = -5V_i$$

Voltage follows current
(so that less current
needs to be applied on
side)



V-I Converter

constant or

O/p \rightarrow controlled current source
even if Z_L is variable.

proportional to input voltage

$$R_1 = R_2 = R_F$$

* $i_1 = i_F$

$$\Rightarrow \frac{Vi - V_L}{R_1} = \frac{V_L - V_o}{R_F}$$

$$\Rightarrow V_o - V_L = \frac{(V_L - Vi) \cdot R_F}{R_1}$$

* $i_o = i_L + i_2$

$$\Rightarrow \frac{V_o - V_L}{R_o} = i_L + \frac{V_L}{R_2}$$

$$\Rightarrow \frac{(V_L - Vi) R_F}{R_1 \cdot R_o} = i_L + \frac{V_L}{R_2}$$

$$\Rightarrow \frac{(i_L \cdot Z_L - Vi) R_F}{R_1 \cdot R_o} = i_L + \frac{i_L Z_L}{R_2}$$

$$\Rightarrow i_L \left[\frac{R_F \cdot Z_L - 1 - Z_L}{R_1 \cdot R_o} \right] = \frac{Vi}{R_1 \cdot R_o} \frac{R_F}{R_2}$$

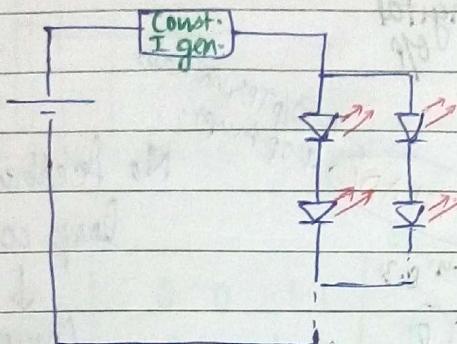
If $\frac{R_F}{R_1 \cdot R_o} = \frac{1}{R_2}$

then $i_L = -\frac{Vi R_F}{R_1 \cdot R_o} \Rightarrow$

$$i_L = -\frac{Vi}{R_o}$$

Applications:-

* LED Street lights.

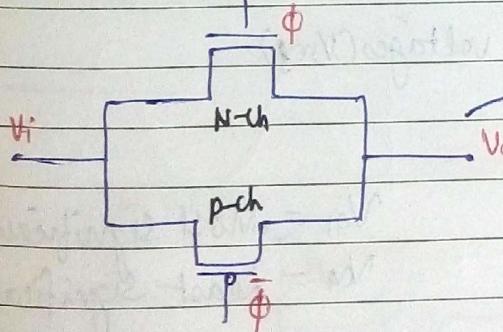


Data Converters

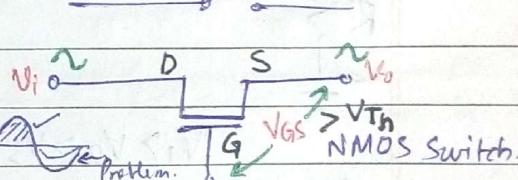
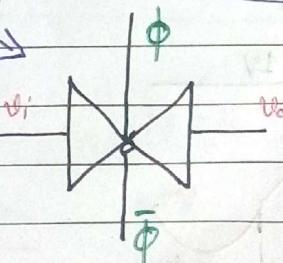
1. Analog to Digital (ADC)
2. Digital to Analog (D-A) (DAC)

Switches.

Digital controlled SW
Transmission Gates.

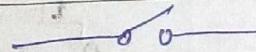


Symbol.

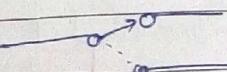


Problem.

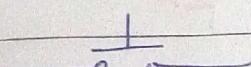
SPST



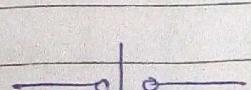
SPDT



Push to
ON

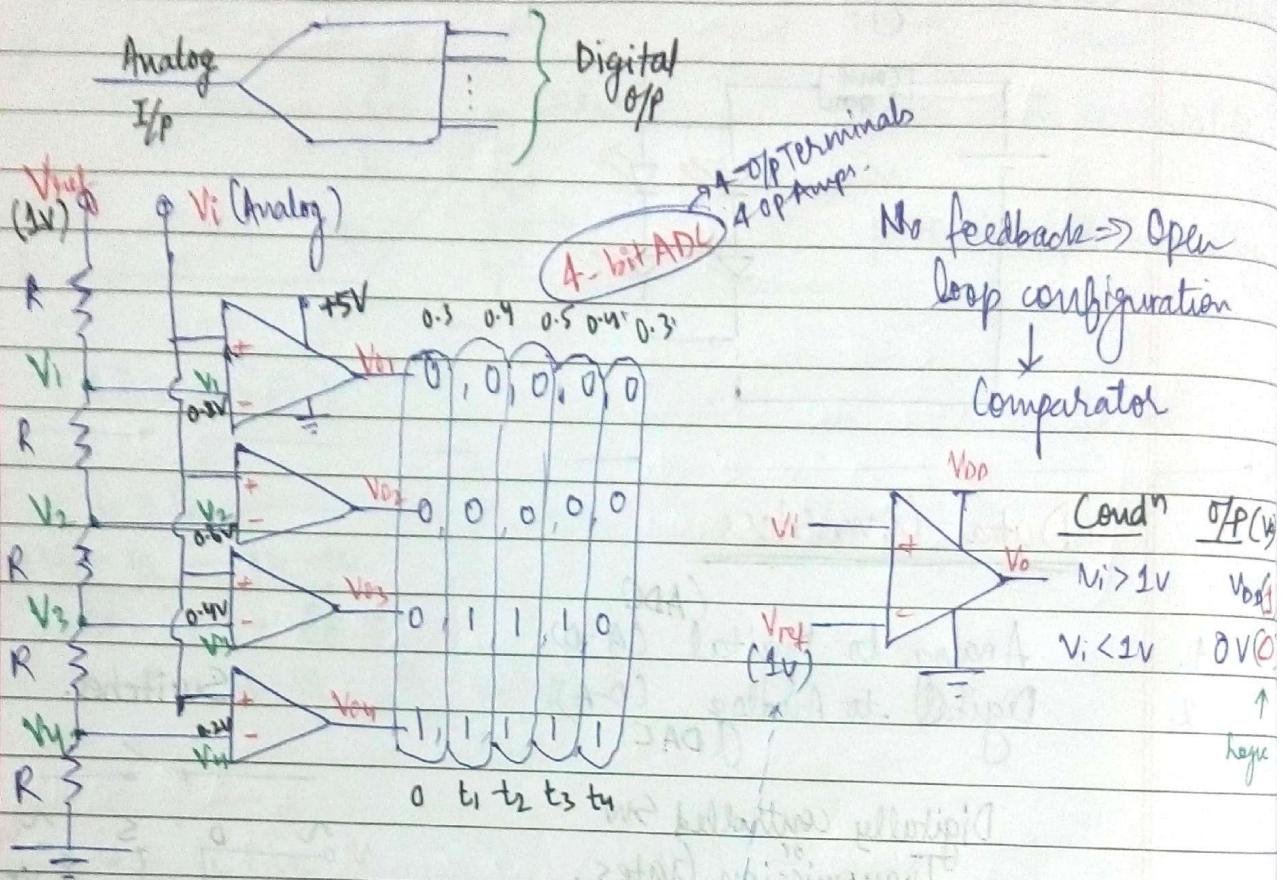


Push to
OFF

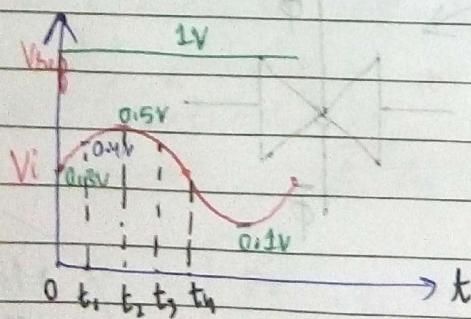


* At least 1 ques
on Digital Out in
End sem.

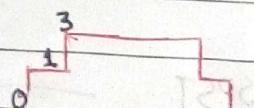
A-D converter (ADC)



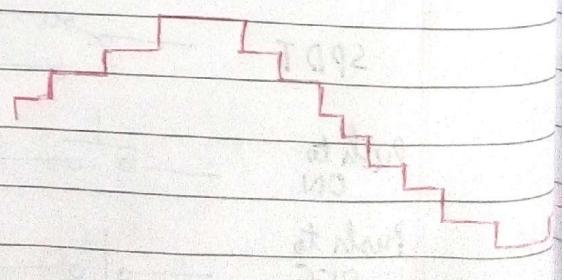
$V_1 > V_2 > V_3 > V_4$
All op-amps have diff reference voltages (V_{ref})

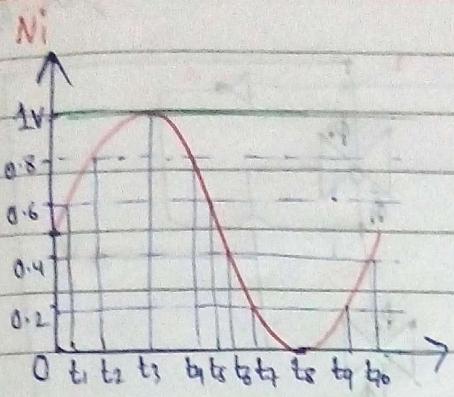


V_{o1} = Most Significant Bit (MSB)
 V_{o4} = Least Significant Bit (LSB)



On increasing
no. of op-amps:



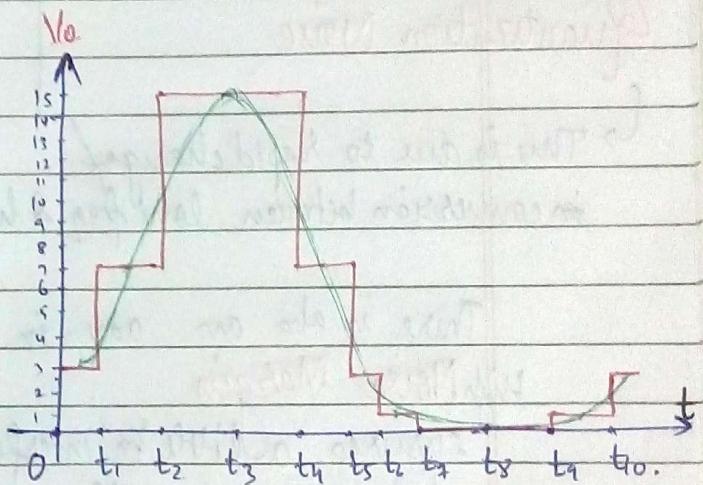


Decreasing t_{out} , $V_i < 0.5V$, $V_o = 0$.

DIGITAL DATE: / /

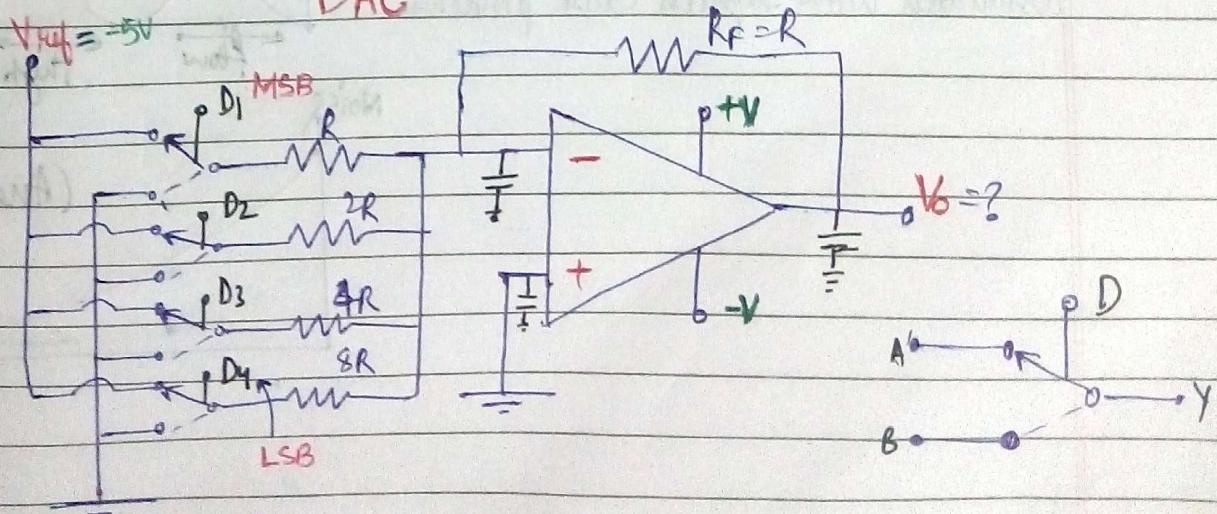
	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
V_{o1}	0	0	1	1	0	0	0	0	0	0
V_{o2}	0	1	1	1	1	0	0	0	0	0
V_{o3}	1	1	1	1	1	1	0	0	0	1
V_{o4}	1	1	1	1	1	1	1	0	0	1

			Decimal values
t_0	0 0 1 1		3
t_1	0 1 1 1		7
t_2	1 1 1 1		15
t_3	1 1 1 1		15
t_4	0 1 1 1		7
t_5	0 0 1 1		3
t_6	0 0 0 1		1
t_7	0 0 0 0		0
t_8	0 0 0 0		0
t_9	0 0 0 1		1
t_{10}	0 0 1 1		3



Distorted Sin wave

DAC



Dig. Value : $D_1 D_2 D_3 D_4$ (MSB) (LSB)

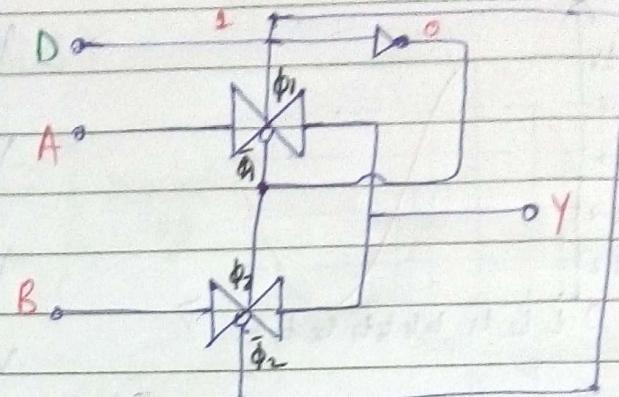
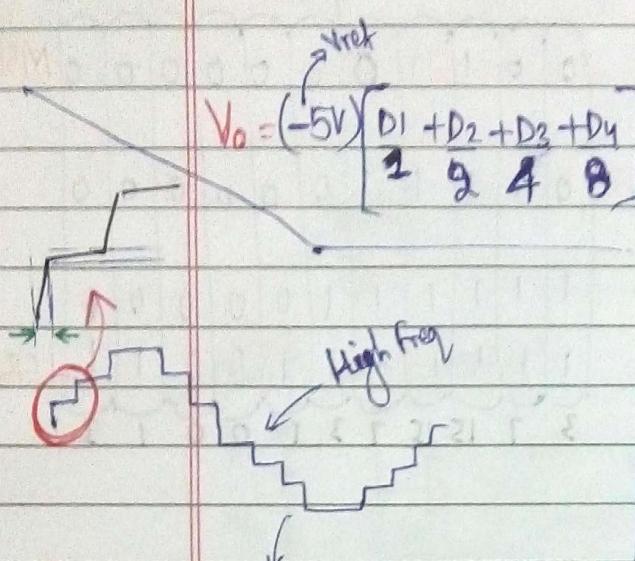
BAJANU HAV PTO.
JAIN NOTES

CT \rightarrow MOSFET, CD, CG, Optamp.
(Postmodem) Drain gate

Orion

PAGE: / /
DATE: / /

$D_1 \rightarrow$ Bubble
 $\hat{D}_1 = \text{PMOS}$.



$$D=1, \phi_1=1 \text{ and } \bar{\phi}_1=0$$

$\uparrow \text{NMOS}=1 \Rightarrow \text{ON} \quad \uparrow \text{PMOS}=0 \Rightarrow \text{ON.}$

$$\phi_2=0 \text{ and } \bar{\phi}_2=1$$

$\uparrow \text{NMOS}=0 \Rightarrow \text{OFF} \quad \uparrow \text{PMOS}=1 \Rightarrow \text{OFF.}$

Quantization Noise

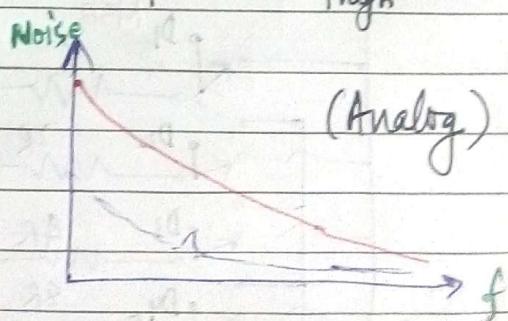
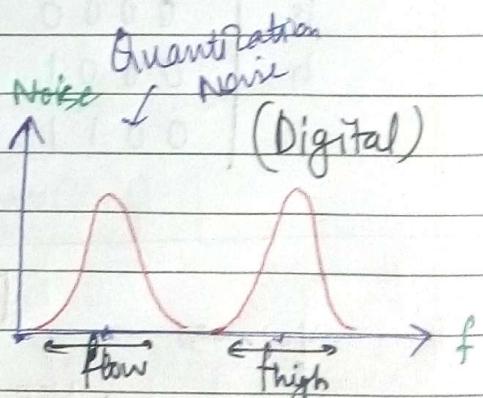
This is due to rapid changes in conversion between low freq & high freq.

There is also an adv. in dig. communication! -

High Noise Margin

ensures a little in interfering noise doesn't cause problems.

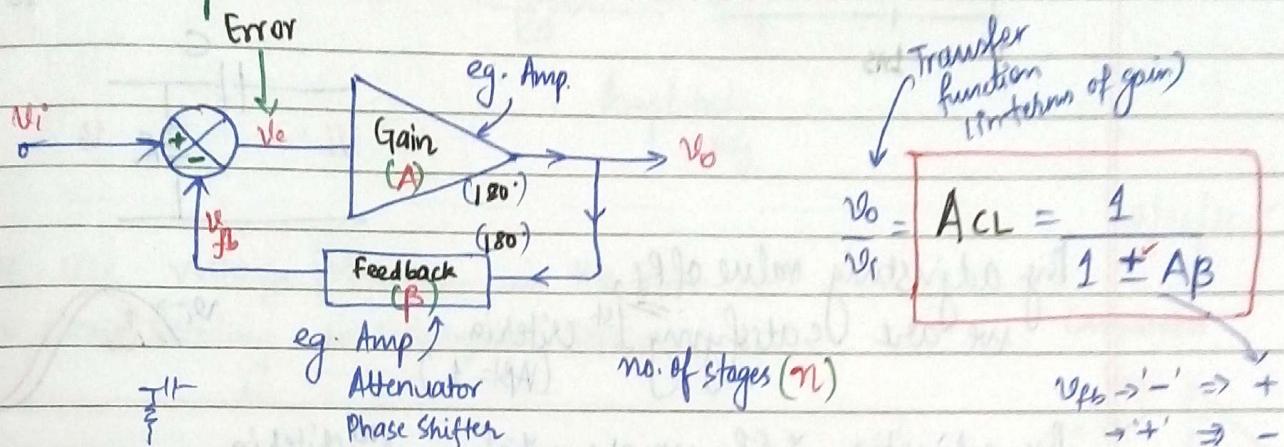
At high freq, the stray capacitance associated with supplies cause problems.



Oscillator.

Sine wave.

Closed Loop Ckt.



- * To make it an oscillator, conditions have to be imposed on closed loop ckt!:-

Barkhausen criteria for oscillation (*Necessary Condⁿ*)

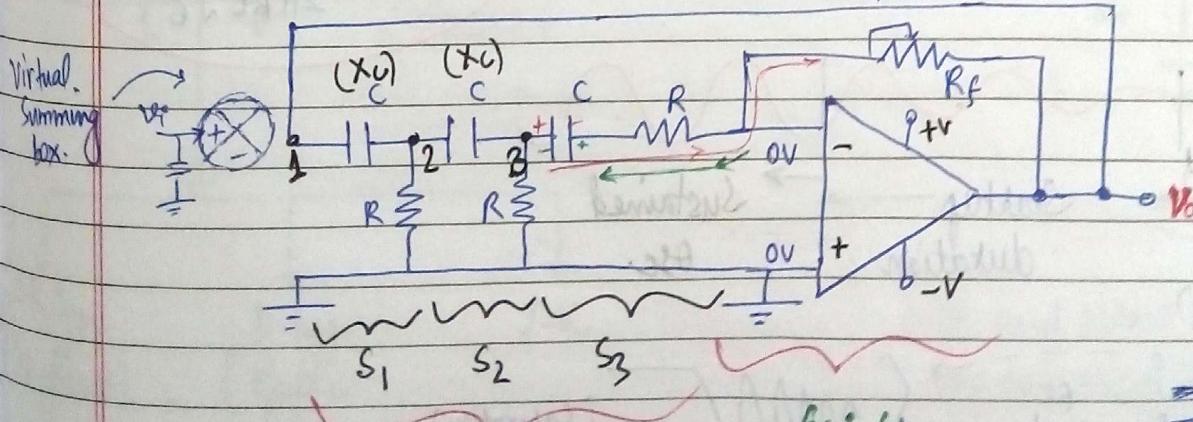
$$1. AB = -1 \quad \text{or} \quad |AB| = 1$$

$$2. \angle AB = 2n\pi \quad \text{or} \quad 0^\circ \text{ or } 360^\circ \text{ or } n \times 360^\circ$$

Integer

$$A(s) \cdot \beta(s)$$

$$A(j\omega) \cdot \beta(j\omega)$$

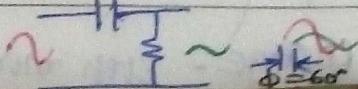


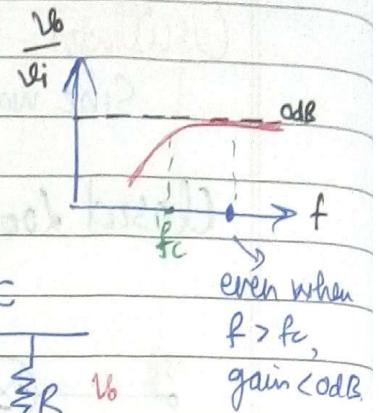
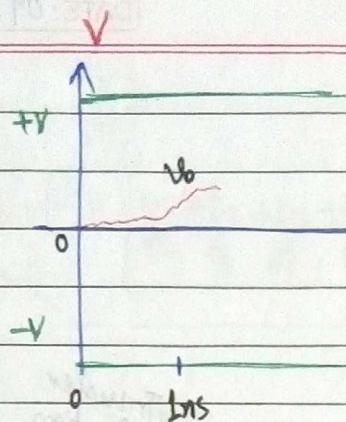
$$X_C = \frac{1}{2\pi f C}$$

$$\phi = \tan^{-1}\left(\frac{X_C}{R}\right) = 60^\circ$$

$$(60 \times 3 = 180^\circ)$$

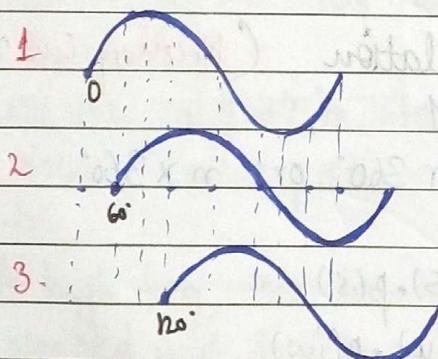
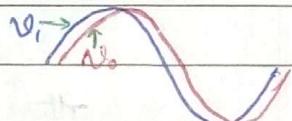
3 HPF

Gain/Amp.
(180°)Stray/fin C
very very small



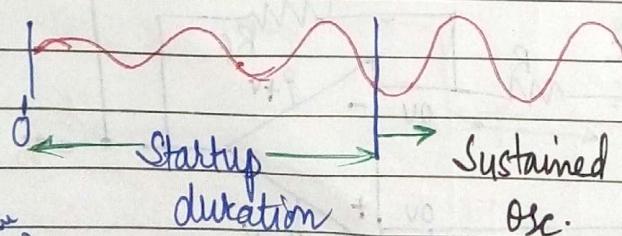
By adjusting value of R_f , we are satisfying 1st criteria. ($|AB| = 1$)

By adjusting \underline{R} , we are satisfying 2nd criteria. ($\angle AB = 2\pi$)



$$f_{osc} = \frac{1}{2\pi RC \sqrt{2 \cdot N}}$$

$$= \frac{1}{2\pi RC \sqrt{6}}$$

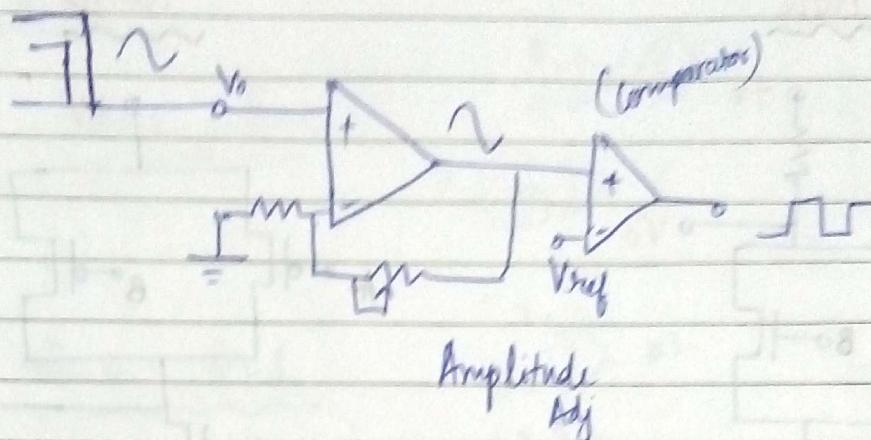


a slight change
in values of L or C
may change φ
and following may
happen.

for 2-stage - $\left\{ \begin{array}{l} \text{(Saturation)} \\ \text{(Attenuation)} \end{array} \right.$

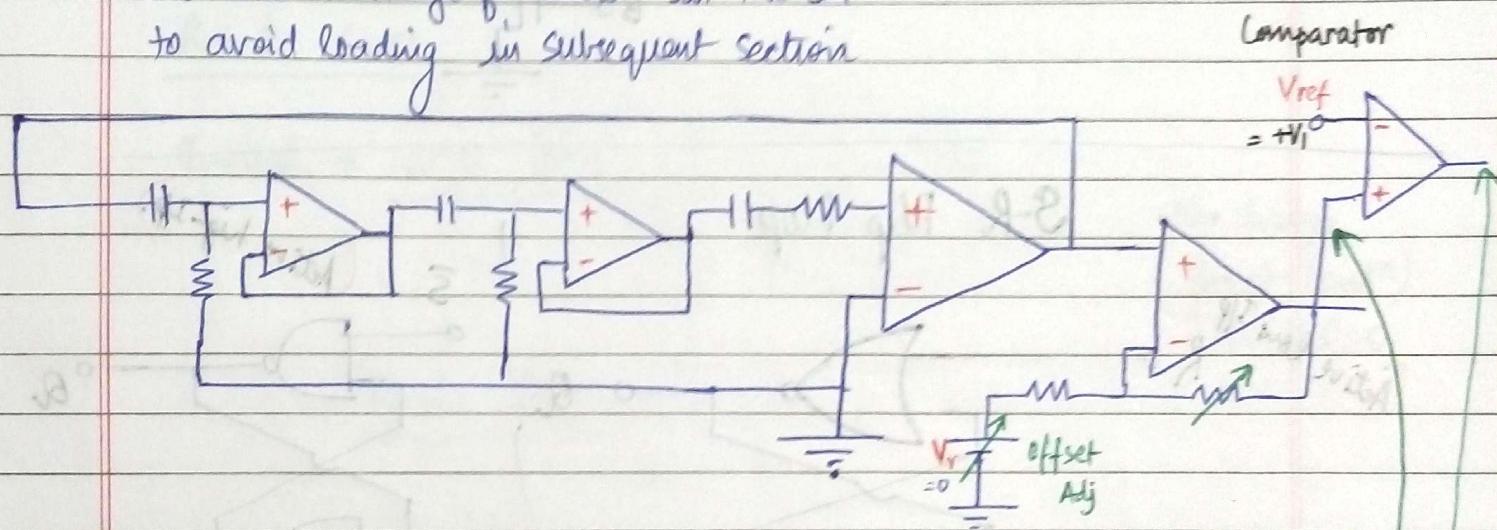
$(N=2) \rightarrow \phi=90^\circ$ (Very high)

$(N=4)$ - 4 RC stage - even more, accurate adjustment (as $\phi=45^\circ$)



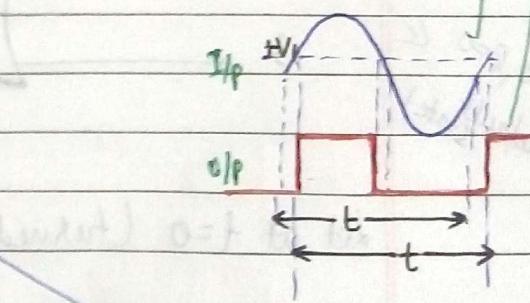
10/11/16

We use voltage followers in the ckt.
to avoid loading in subsequent section



FLIP FLOP OR **LATCHES**

1 0
↓
SR Type
(Set-Reset)
↓
D-type
(Data or Delay)
↓
JK



NOR and NAND are
two universal gates.