

Lab Report 1

Using Quartus Prime 18.1 and the De2-115 Development Board

Created by:

Group 18

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Executive Summary

Throughout this lab, we explored project creation using Intel's Quartus Prime development platform, focusing on FPGA implementation. We utilized the DE2 board's peripherals and learned to construct basic circuits, including a single bit adder, starting with an XOR logic gate. This exercise introduced hierarchical design principles for organizing logic elements into reusable blocks. Additionally, we covered the conversion of VHDL files into symbol files for representation in block diagrams. These skills will prove valuable for future projects and assignments.(work in progress)

Introduction

The objective of this lab was to utilize the Quartus Prime development platform by Intel to create a foundational project. By implementing digital circuitry on the FPGA chip and interfacing with the DE2 board's switches and LEDs, participants were introduced to the essential processes of constructing simple circuits and integrating them into functional blocks. Key components of the lab included working with logic gates, hierarchical design, and designing single bit adders. Furthermore, the lab demonstrated the conversion of VHDL files into symbol files for use in new block diagram files. Overall, this lab offered a comprehensive exploration of various techniques for analyzing and displaying logic gates using digital circuitry.

Experimental Methodology

To conduct the experiment described in Lab 1, you'll need a computer equipped with Quartus Prime 18.1 software and an Altera DE2 board connected via a USB Blaster Cable. Ensure the DE2_115_pin_assignment.csv file is downloaded to access logical connectors, inputs, and outputs. Using these components, Group 18 constructed various circuits including AND, XOR, Full-Adder, and Half-Adder circuits. The arrangement of logical connectors and inputs/outputs was guided by Lab 1 instructions, which provided images illustrating the final layout of each circuit. Group 18's schematics for these circuits are presented in the following results section. Before confirming the construction results, the circuit design file must be designated as a "top-level entity" and compiled in Quartus. To validate accuracy, Group 18 tested each gate's operation using the DE2 board and compared the results with truth tables. Results and figures were documented upon completing each lab section.

Results

Throughout Lab 1, Group 18 successfully generated schematics for an AND gate, an XOR gate, a Full-Adder circuit, and a Half-Adder circuit within the Quartus Prime software environment. Each schematic underwent rigorous testing across multiple test cases, as depicted in the corresponding truth tables below. Utilizing the DE2 board, Group 18 verified the proper

operational functionality of each schematic by observing the LED outputs aligned with the truth table inputs. A lit LED indicated a true result, while an unlit LED indicated a false result, as per the provided test cases. Notably, all circuits passed each test case with flying colors. Figures 1 through 12 showcase the schematics, compilation results, and truth tables for each circuit.

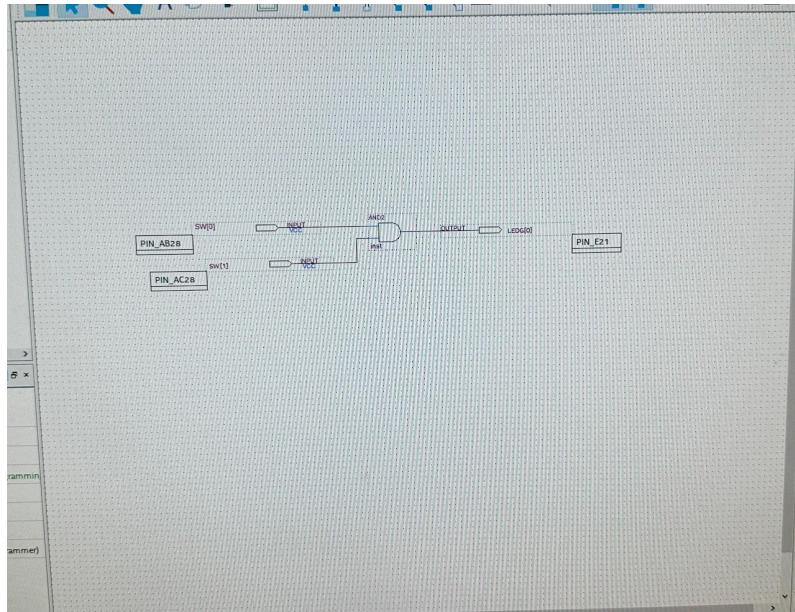


Figure 1 - AND gate schematic

A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1



Figure 2 - AND Truth Table

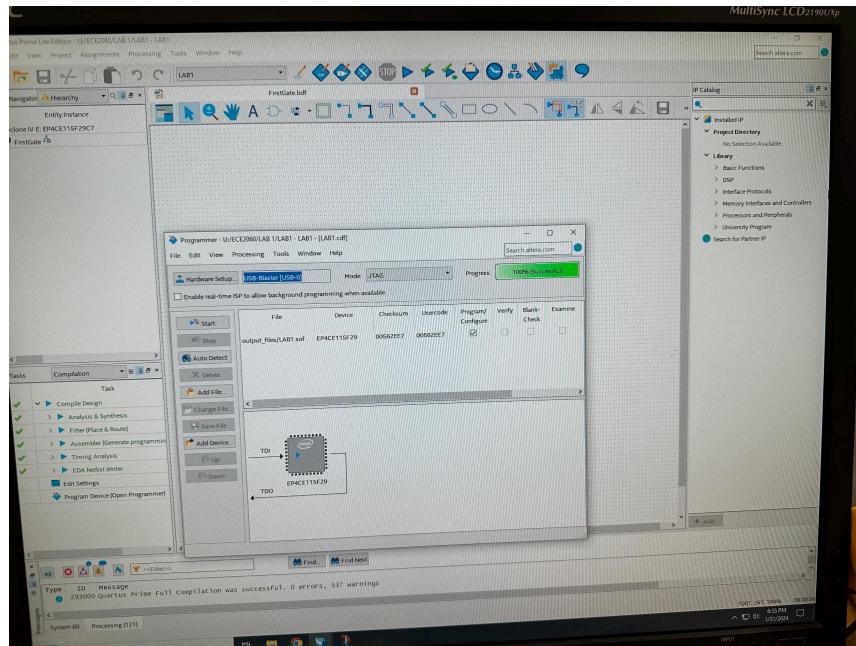


Figure 3 - AND Compilation Results

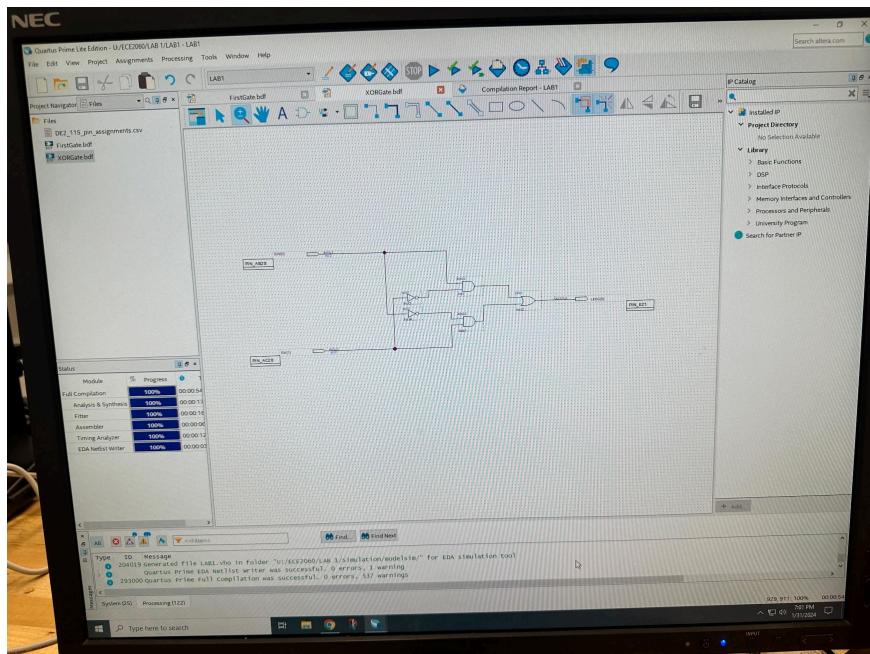


Figure 4 - XOR gate schematic

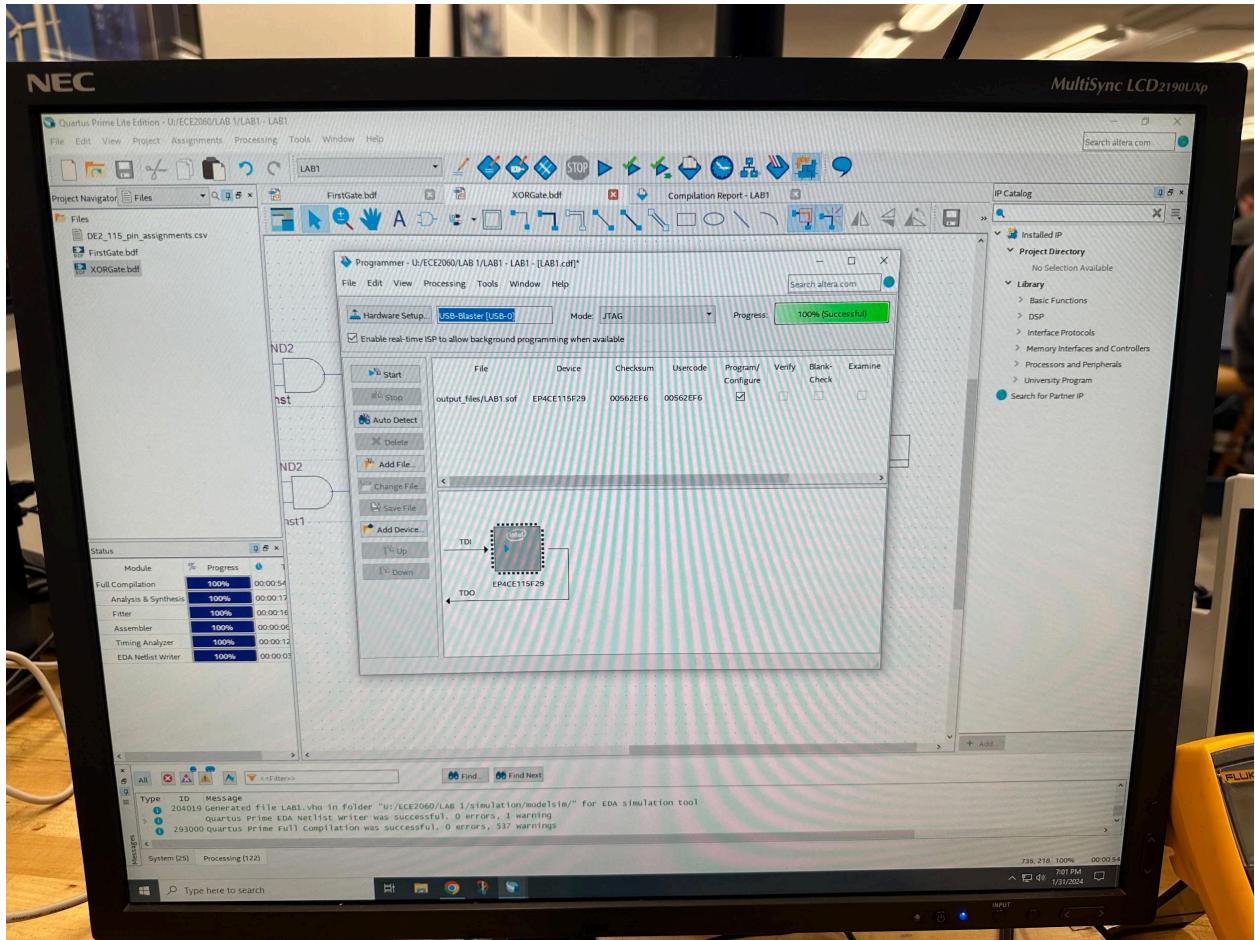


Figure 5 - XOR Gate compilation results

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

Figure 6 - XOR Gate Truth Table

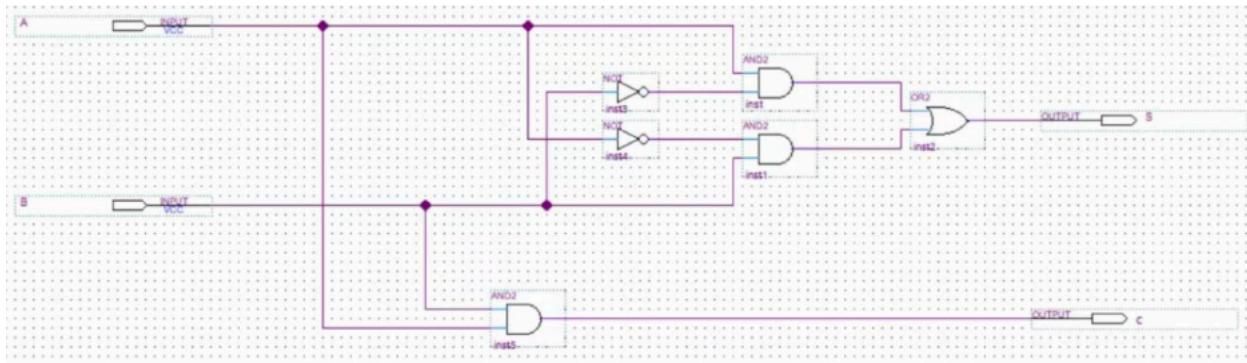


Figure 7 - Half adder Schematic

Inputs		Outputs	
SW[1] A	SW[0] B	LEDG [1] (S)	LEDG [0]
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 8 - Half Adder Truth Table

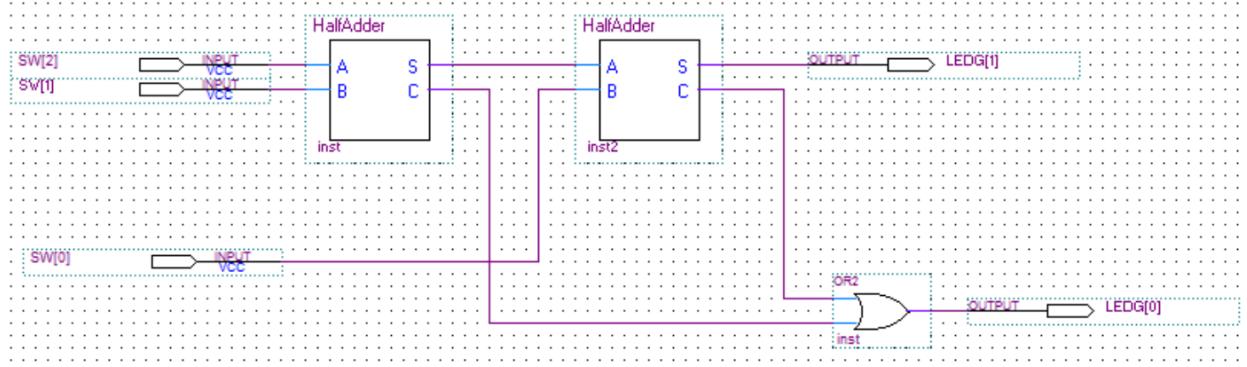


Figure 9 - Full Adder Schematic

Inputs			Outputs	
SW[2] A	SW[1] B	SW[0] C	LEDG [1] (S)	LEDG [0] (Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 10 - Full Adder Truth Table

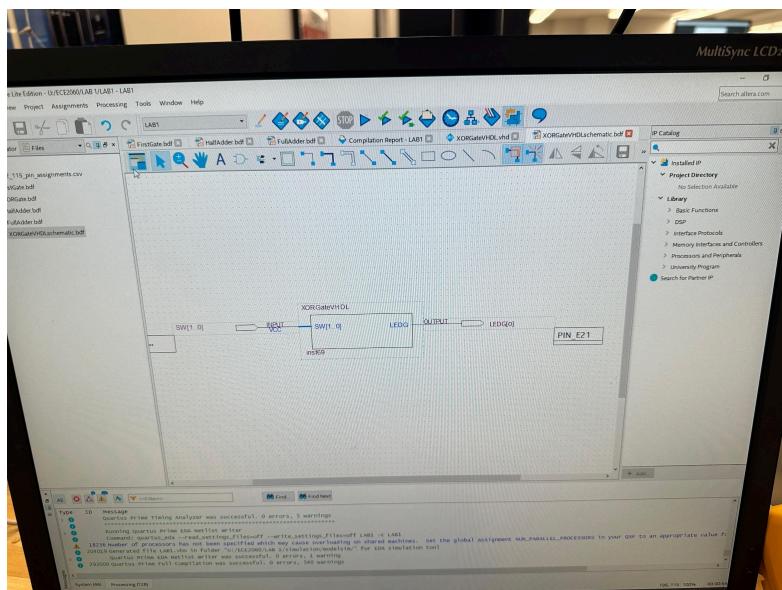


Figure 11 - XOR Gate VHDL Schematic

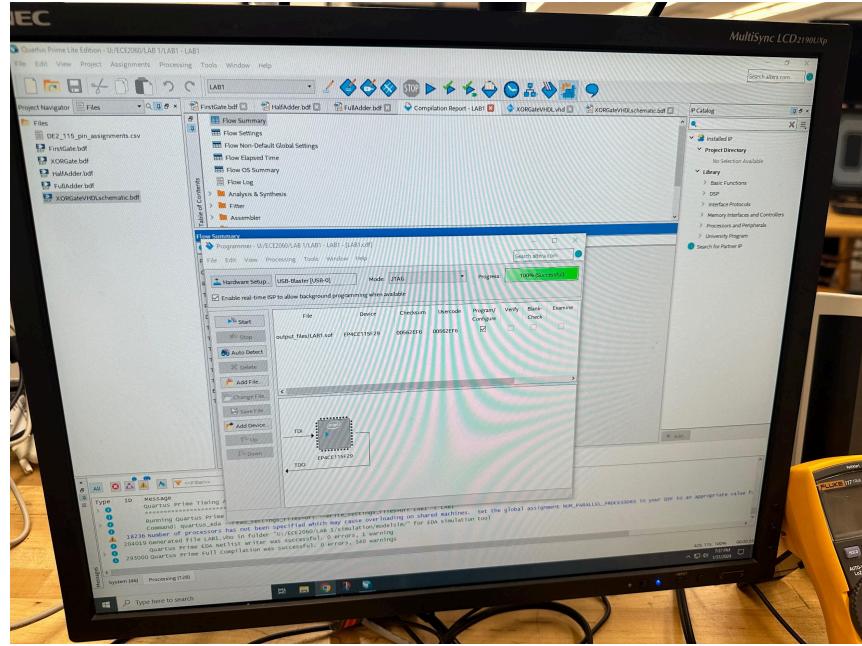


Figure 12 - XOR Gate VDHL Compilation Results

Discussion

To complete this project effectively, it's essential to create a dedicated project folder in the U:\ drive to ensure project files remain intact even after logging out of the lab computers. Organizing projects in separate folders enhances file management and facilitates tracking of associated files. FPGA, short for "Field-Programmable Gate Array," refers to an integrated circuit that can be configured post-manufacturing. Throughout the semester and for all assignments, it's advisable to keep the run/program button in the run position consistently. Regarding hierarchy, this practice enables users to reuse logical blocks multiple times. To create a hierarchical block, start by saving the current schematic. Then, navigate to the file menu, choose "create and update," and select "create symbol files for current file." Save the file and access the block through the "and" symbol in the toolbar.

Conclusion

The lab's culmination saw Group 18 successfully crafting several circuits comprising different logic gates. Each circuit was accompanied by a corresponding truth table, facilitating rigorous testing on the DE2 board to validate their construction accuracy. Quartus Prime software played a pivotal role in meticulously articulating these circuits, empowering users to construct and simulate truth tables using the DE2 board.

Overall, this lab proved highly beneficial for comprehending the design intricacies of circuits at various levels, the procedural aspects of running these circuits, and verifying their validity through DE2 board testing.

Acknowledgments

All members of Group 18 actively contributed and participated equally in all lab activities. Each team member possesses a thorough understanding of the procedures undertaken and the results obtained during Lab 1.

References

- Lab report template - [reportTemplate](#)