ELL305 Computer Architecture
Assignment 3
Implementation of a 5-stage SimpleRisc Processor

October 1, 2019

In this assignment, you have to implement a SimpleRisc processor with a *5-stage pipeline*. This assignment has to be implemented in LogiSim. We are providing you with a LogiSim circuit of the SimpleRisc *single cycle* processor. This processor runs all SimpleRisc instructions and can execute any valid SimpleRisc program to give correct outputs (provided the instructions are given in *binary/hexadecimal*). This assignment has to be done in **groups of 2**, and you will be evaluated based on the demos.

1 Description

- Download the assignment and extract it.
- The folder "assignment3" contains 2 additional files (along with this pdf):
  1. "Processor.circ": It is the LogiSim circuit file and represents the processor code.
  2. "Readme.pdf": It describes the procedure for loading the *.circ* file, and then executing your program.
- Once the basic things are working, you can start with your implementation. All your code modifications should go **only** in the Processor.circ file.
- You need to implement forwarding and consider a predict-not-taken policy.

1.1 Submitting Your Assignment

- Create a folder named as <EntryNumber> which contains modified Processor.circ file. Compress the folder and submit only the <EntryNumber>.zip archive on Moodle. For example, if your entry number is 2017EE51010, then submit as 2017EE51010.zip. No other format will be accepted. For assignment 1, we received various submissions with the incorrect format.

We will be penalizing those assignments. However, If anyone fails to comply by the prescribed format, will straightway get a zero.

To summarize, you have to do the following steps:

1. Create a folder named <EntryNumber>.
2. Copy Processor.circ file in this folder.
3. Create the .zip file
   - *For Windows*: Select the Processor.circ file, right-click and point to "Send to" and then select Compressed (zipped) folder. Name the folder as <EntryNumber>.zip
   - *For Linux:* Select the Processor.circ file, right-click and point to "Compress" and then create the zipped folder with the name as <EntryNumber>.zip
4. Submit this zip file on Moodle.

- The deadline is **November 15, 2019, 23:59 hours**.

1.2 Grading Scheme

1. Marks division: Total = 50 marks
   - Correct implementation of all stages: 38 marks
   - Correct implementation of forwarding circuitry: 12 marks
2. Late policy: 20% penalty per day (rounded to the next day, i.e. 3 hours late implies 1 day late).
3. **Plagiarism**: We will run MOSS over all submissions. If any similarity to any other source is found, you will get a zero.