

**B. E. Third Semester ( Computer Technology ) / SoE – 2018 Examination**

**Course Code : CT 2201**

**Course Name : Computer Architecture and Organisation**

Time : 3 Hours ]

[ Max. Marks : 60

**Instructions to Candidates :—**

- (1) All questions are compulsory.
- (2) All questions carry marks as indicated.
- (3) Due credit will be given to neatness and adequate dimensions.
- (4) Assume suitable data wherever necessary.
- (5) Illustrate your answers wherever necessary with the help of neat sketches.

1. (A1) Draw a diagram which shows connection between processor and main memory. Also list the steps needed to execute the machine instruction **Add R2 , R0.** 5(CO1)
- (A2) What do you mean by  $1\frac{1}{2}$  addressing method explain with example. 3(CO1)
- (A3) Draw single bus structure of a computer and write its advantages and disadvantages. 2(CO1)

**OR**

- (B1) Write the set of instruction for solving the execution :  
 $Z = (A * (B + C - D)) / ((E + F * G) * (B + C + D))$  using :
    - (i) Zero operand instruction
    - (ii) One operand instruction 4(CO1)
  - (B2) How sign number, characters and machine instructions can be represented in **32** – bit word information in memory ? 3(CO1)
  - (B3) What is the purpose of **MAR , MDR** and **IR** registers ? 3(CO1)
2. (A1) Draw signal bus organization of a processor ? Also write control step for execution of an complete instruction. **MOV R3 , R1.** 5(CO2)

- (A2) Discuss the following assembler directives with example  
(1) **EQU** (2) **DATAWORD** 2(CO1)

- (A3) Explain immediate, register and indexed addressing mode with example.  
3(CO1)

**OR**

- (B1) What do you mean by big-endian and little-endian assignment. Also solve if registers **R1** and **R2** of a computer contain the addresses **1200** and **4600** respectively. What is the effective address of the memory operated and the addressing modes in each of the following instructions ?

**Move 20 (R1), R5**

**Add – (R2), R5** 5(CO1)

- (B2) Write control sequence for complete instruction **ADD R4, R5, R6** using three bus organization of a processor. 3(CO2)

- (B3) Explain subroutine Linkage with example. 2(CO1)

3. (A1) 'Explain "microinstruction with next address field" with suitable diagram. What is the significance of "next address" field ? 5(CO2)

- (A2) Compare vertical and horizontal organization w. r. to microprogrammed control. 3(CO2)

- (A3) Write short note on emulation. 2(CO2)

**OR**

- (B1) Discuss grouping of control signal in detail. 5(CO2)

- (B2) Define the term w. r. to microprogrammed control

(1) Control Word

(2) Control Store

(3) Microroutine 3(CO2)

- (B3) Why microinstructions are prefetched ? What are its organizational difficulties ? 2(CO2)

4. (A1) Describe array multiplication of positive binary operands. 5(CO2)  
 (A2) Compute  $(+21) \times (-9)$  using Booth's algorithm. 3(CO2)  
 (A3) Write advantages and disadvantages of Booth's algorithm. 2(CO2)

**OR**

- (B1) Compute  $16 \times 12$  using sequential multiplication algorithm. 5(CO2)  
 (B2) What is the disadvantage of ripple carry adder ? How it is overcome ? 3(CO2)  
 (B3) Compute  $-8 \times -9$  using fast multiplication. 2(CO2)
5. (A1) Solve  $12 \div 4$  using restoring division algorithm. 5(CO2)  
 (A2) Fit the number  $100_{10}$  in IEEE Single precision formats. 2(CO2)  
 (A3) Compare cache memory, main memory and secondary memory w. r. to size, speed and cost per bit. 3(CO3)

**OR**

- (B1) Discuss internal organization of semiconductor RAM memory chips. 5(CO3)  
 (B2) Draw block diagram for designing  $64 \text{ K} \times 8$  memory using  $8 \text{ K} \times 1$  memory chips. 3(CO3)  
 (B3) State the use of flash cards and flash drives. 2(CO3)

6. Solve any **Three** :—

- (A1) Consider a computer with a **4** – ways set – associative mapped cache of the following characteristics : a total of **1 MB** of main memory, a word size of **1** byte a block size of **128** words and a cache size of **8 KB**. While accessing the memory location **0C795H** by the CPU, the contents of the **TAG** field of the corresponding cache line is :

- A**     **000011000**  
**B**     **110001111**  
**C**     **00011000**  
**D**     **110010101**

5(CO3)

(A2) Compare DMA and interrupt. 2(CO2)

(A3) Explain RAW hazards with example. 3(CO2)

**OR**

(B1) Discuss different data hazard in detail. 5(CO2)

(B2) Write a note on interrupts. 3(CO4)

(B3) Write advantages and disadvantages direct – mapping technique. 2(CO3)