Team Details

Team Name: ChipVision

SR. NO	ROLE	NAME	ACADEMIC YEAR
1	**Team Leader**	*Abhinav Sharma*	2nd Year
2	Member 1	Anshuman Dutta	2nd Year
3	Member 2	Rajat Kumar	2nd Year

COLLEGE NAME

Vivekananda Institute of Professional Studies – Technical Campus

TEAM LEADER CONTACT NUMBER

8800288158

TEAM LEADER EMAIL ADDRESS

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Problem Statement Addressed

Selected the problem statement your idea addresses

DESCRIPTION / DETAILS

- Tiny defects in wafers/dies cause failures and reduce yield.
- Manual or cloud inspection is slow, costly, and not scalable.
- Build an Edge-AI system to detect and classify defects from images.
- Enable real-time, low-latency inspection at the manufacturing line.
- Improves production yield, reduces cost, and increases reliability.
- Current systems fail in real-time inline fab deployment.

Idea Description - Describe your Idea/Solution/Prototype

Provide a brief summary of your idea, including the key concept and approach. Provide a brief overview of your solution and how it addresses the problem statement.

KEY CONCEPT & APPROACH

- Edge-AI detects and classifies wafer/die defects in real time at the tool
- Confidence-aware decisions with adaptive learning on-device
- Maps defects → process root cause and enables feedback to manufacturing

SOLUTION OVERVIEW

- Edge-AI runs directly at inspection tools → real-time defect detection, no latency or cloud dependency
- Lightweight model enables fast, scalable analysis across high-volume wafer image streams
- Defect insights mapped to process causes → supports yield improvement and inline process control

Proposed Solution - Describe your Idea/Solution/Prototype

Describe your idea in detail. Include the methodology, technologies involved, and how it addresses the chosen problem statement.

SOLUTION DETAILS

- **Methodology:** Build CNN-based model for defect detection + classification, add confidence scoring, map defects → process root causes, enable continual learning at edge
- **Technologies:** Python, PyTorch/TensorFlow, OpenCV preprocessing, ONNX conversion, NXP eIQ for edge deployment
- **Implementation:** Dataset creation → model training & validation → optimization for low latency → edge porting → real-time inference + feedback to process control

Innovation and Uniqueness

Highlight what makes your idea unique or innovative compared to existing solutions.

KEY INNOVATION

- Edge-deployed AI enabling real-time inline defect intelligence (novel application in fab workflow)
- Defect → process root-cause mapping for yield improvement (novel process integration)
- Confidence-aware, adaptive edge learning for changing fab conditions (advanced implementation innovation)

COMPETITIVE ADVANTAGE

- Real-time edge inference → faster decisions, no cloud latency
- Lower bandwidth and infrastructure cost vs centralized systems
- Adaptive, confidence-aware model improves accuracy, usability, and yield impact

Impact and Benefits

Explain how your solution will make an impact, such as improving performance, reducing costs, increasing efficiency, or solving other challenges.

Primary Impact

- Real-time defect intelligence at the tool → faster manufacturing decisions
- Higher yield and reliability through early defect detection + root-cause insight
- Reduced cost and downtime via edge deployment and process feedback

Quantifiable Outcomes

- 2–5× faster real-time defect detection at the edge
- 20–30% improvement in yield through early defect identification
- 40–60% reduction in bandwidth and inspection infrastructure cost

Technology & Feasibility/Methodology Used

Describe the technologies, methodologies, or tools you plan to use to implement your idea.

IMPLEMENTATION STRATEGY

- Dataset collection & labeling (defect classes)
- Model training + validation (CNN)
- Optimization for low-latency edge deployment
- ONNX conversion → NXP eIQ porting
- Real-time inference + process feedback integration

Software Architecture

- Image preprocessing (OpenCV)
- CNN defect detection + classification
- Confidence scoring + root-cause mapping
- ONNX conversion → edge inference pipeline

Hardware Components

- NXP i.MX RT edge platform
- Fab inspection image inputs (Optical/SEM datasets)
- On-device compute for real-time inference

Development Tools

- Python, PyTorch/TensorFlow
- OpenCV, NumPy
- ONNX, NXP eIQ toolkit
- GitHub for version control

GitHub Link

GitHub Repository

https://github.com/anshuman9468/Chips_Hackers

Research and References

References & Citations

List key papers, articles, or data sources.

Ref 1: Inspection and Classification of Semiconductor Wafer Surface Defects Using CNN Deep Learning Networks
URL: https://doi.org/10.3390/app10155340

Ref 2: Defect detection and classification on semiconductor wafers using two-stage geometric transformation-based data augmentation and SqueezeNet lightweight convolutional neural network
URL: https://doi.org/10.1016/j.cie.2023.109549