Implementation of Low Voltage Floating Gate MOSFET based Current Mirror Circuits using 180nm technology

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***Abstract*— The paper discusses implementation of low voltage (LV) basic current mirror (CM) and cascode current mirror (CCM) circuits using Floating Gate MOSFET (FGMOS) devices. The performance parameters such as output resistance, minimum output voltage requirement and power dissipation are compared for basic CM and double CCM circuits. The current mirror circuits are implemented with 180 nm technology using Cadence Virtuoso and simulated with Spectre RF. The simulation results are in good agreement with theory. The FGMOS based basic CM and double CCM circuits exhibited 52.4% and 40% power reduction as compared to gate driven current mirror circuits.**

Keywords— Floating Gate MOSFET, Current mirror, Cascode Current mirror.

I. INTRODUCTION

In analog circuits, low voltage and low power operations are main issues of concern due to increasing demand for portable electronic applications. Current mirror is one of the most frequently used analog circuit where power utilization is influenced by supply voltage. Hence it is a challenging task to design low voltage (LV), low power (LP) and high performance current mirror circuits.

Floating gate transistors provide an optimal way of tuning the threshold voltage of MOSFET by applying appropriate bias voltage [1]. The main advantage of using floating gate transistor is to decrease the headroom voltages. However, use of floating gate transistors has some disadvantages like increased area requirement and reduced gain bandwidth parameter.

II. FLOATING GATE MOSFET

The fabrication trend followed in modern day VLSI is to create smaller and faster transistors. However, reducing size may lead to dielectric breakdown. This issue can be reduced by operating the transistor with low voltage power supply [2]-[6].

The structure of Floating-Gate MOSFET (FGMOS) is similar to a conventional MOSFET except that FGMOS has two gates i.e. control gate(s) and floating gate (FG). The FGMOS is fabricated using a standard double-polysilicon CMOS process, where the first polysilicon layer forms the floating gate (FG) over the channel and the second polysilicon layer forms the multiple-input control gates (MIG) over the FG. The secondary gates or inputs are electrically isolated from FG and are only capacitive connected to FG [5]. The FG inserted between the transistor channel and MIG provides indirect control over the operation of MOSFET.

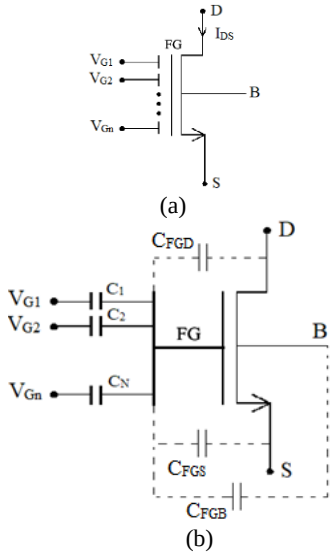


Fig. 1 The n-input n-channel FGMOS transistor (a) Symbol, (b) Equivalent circuit model

Let V_i (for i =1, 2,... N) are the control input voltages. The effective input capacitance $C_{i,eff}$ associated with these inputs is given in (1a) as the summation of input capacitances between control gates and floating gate. The total capacitance C_T of the floating-gate is given by

$$C_{i,eff} = \sum_{i=1}^{N} C_i = C_1 + C_2 + .. + C_N \quad (1a)$$

$$C_T = \sum_{i=1}^{N} C_i + C_{FGD} + C_{FGS} + C_{FGB} \quad (1b)$$

where $C_{FGD,}$ C_{FGS} and C_{FGB} are the parasitic capacitance of floating gate with drain, source and bulk respectively.
The voltage on its floating gate (V_{FG}) is given by

$$V_{FG} = \sum_{i=1}^{N} \left(\frac{C_i}{C_T} V_{Gi}\right) + \frac{C_{FGD}}{C_T} V_{DS} + \frac{C_{FGS}}{C_T} V_{SS} + \frac{C_{FGB}}{C_T} V_{BS} + \frac{Q_{FG}}{C_T} \quad (2a)$$

where
Q_{FG} is charge trapped in FG during fabrication
V_{DS} is drain-source voltage
V_{SS} is source voltage
V_{BS} is bulk-source voltage
From (2a) it follows that the voltage on floating gate is linear sum of all input voltages (drain-source voltage, source voltage and bulk-source voltage) weighted by capacitive scaling factors.
As $C_i \gg C_{FGD}, C_{FGS}, C_{FGB}$ V_{FG} would only depend on the voltages at the control inputs as

$$V_{FG} = \sum_{i=1}^{N} \left(\frac{C_i}{C_T} V_{Gi}\right) \quad (2b)$$

In case of a two input FG-MOSFET in Fig. 2(a), a bias voltage V_{bias} is applied to one of the control gates through C_1 and the input signal is applied to second gate through C_2. Assuming zero initial voltages and neglecting parasitic capacitances of FG in comparison with C_1 and C_2, the floating gate voltage is given by

$$V_{FG} = \frac{C_1}{C_T} V_{bias} + \frac{C_2}{C_T} V_{in} \quad (2c)$$

Assuming $(C_1 + C_2) \gg C_{FGD}, C_{FGS}, C_{FGB}$, the expression for drain current for n-channel FGMOS in saturation region is shown to be

$$I_{DS} = \frac{\beta}{2}\left\{\left(\frac{C_2}{C_T} V_{in} + \frac{C_1}{C_T} V_{bias}\right) - V_{th}\right\}^2 \quad (3a)$$

The equation (3a) can be written as

$$I_{DS} = \frac{\beta}{2}\left(\frac{C_2}{C_T}\right)^2 \left\{V_{in} - \left(V_{th}\left(\frac{C_T}{C_2}\right) - V_{bias}\left(\frac{C_1}{C_2}\right)\right)\right\}^2 \quad (3b)$$

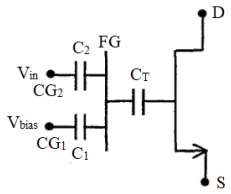
From (3b) the effective threshold voltage for the FGMOS is shown as

$$V_{th,eff} = V_{th}\left(\frac{C_T}{C_2}\right) - V_{bias}\left(\frac{C_1}{C_2}\right) \quad (3c)$$

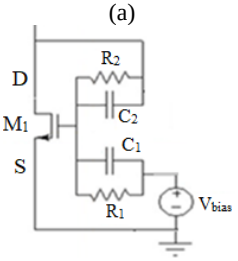
Alternately $V_{th,eff}$ is expressed as

$$V_{th,eff} = V_{th} + \frac{C_1}{C_2}(V_{th} - V_{bias}) \quad (3d)$$

From (3c)-(3d) it is evident that $V_{th,eff}$ can be made smaller than V_{th} by appropriate selection of C_1, C_2 and dc bias voltage V_{bias}. As the simulation tool does not support floating gate node, resistances are placed in parallel to each capacitors C_1 and C_2 in the simulation model of Fig. 2 (b) to provide the dc path.



(a)



(b)

Fig. 2 Two-input FGMOS with control gate voltages (a) Equivalent circuit model (b) simulation model

The presence of multiple gates provides ability to control and reduce the threshold voltage of the MOSFET [7] which enable circuits to work with low supply voltage and with lesser power.

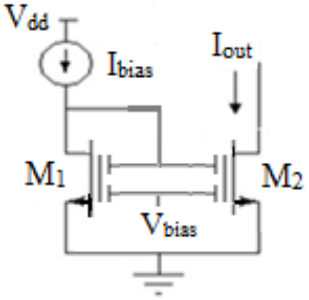
The performance of the floating gate is affected by process variations as some charges may get locked during fabrication leading to dc offset [7]. The amount of charges on FG can be modified by electron tunneling and hot electron injection. However, Q_{FG} can be eliminated by the method proposed [8].

III. FGMOS BASED CURRENT MIRROR (CM)

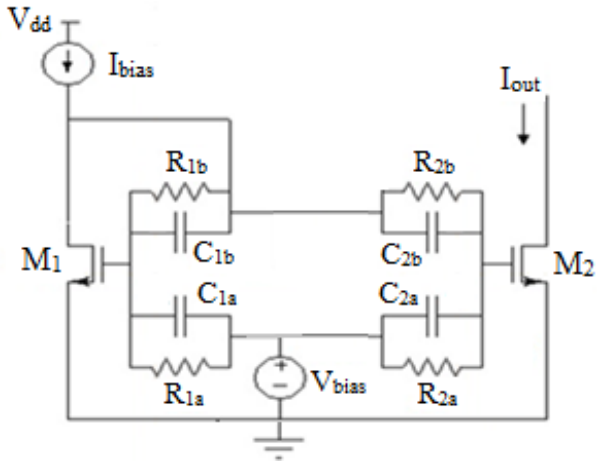
Current mirror circuits are one of the most fundamental blocks in analog circuit design. The current mirror circuit copies the current flowing in one active device to another, keeping the output current constant regardless of load variations [9]. Important areas of applications for current mirror circuits are current biasing, current amplification and current copyng. The desirable characteristics of current mirror circuits are high output resistance, minimum output voltage and high voltage swing [9]. The current mirror circuits are designed using FGMOS, in order to operate with reduced supply voltage [2]-[6].

A. FGMOS based basic Current Mirror (CM)

The configuration of FGMOS based CM is same as that of conventional gate driven CM except the use of two input FGMOS. The circuit of basic current mirror using FGMOS is shown in Fig. 3.



(a)



(b)

Fig. 3 FGMOS based basic current mirror (a) schematic circuit (b) equivalent circuit

The two input FGMOS transistors M_1 and M_2 form the current mirror. In the two input FGMOS one gate is used as conventional input terminal and the second gate is applied with a DC biasing voltage V_{bias} which is used to lower the threshold voltage there by reducing $V_{o,min}$ of the current mirror. The resistances R_{1a}, R_{1b} and capacitances C_{1a}, C_{1b} are part of the macro model of FGMOS. The output resistance of the basic current mirror in Fig. 3 is given as

$$R_{out} = r_{ds2} \tag{4}$$

B. FGMOS based double Cascode Current Mirror (CCM)

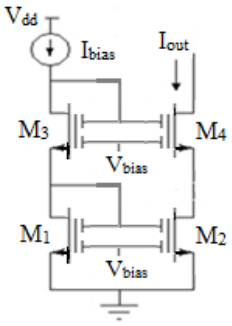
In general, CCM require higher voltage headroom as compared to a simple CM, but provides higher output impedance. The FGMOS based low voltage CCM is shown in Fig. 4. All the MOS devices are two input FGMOS. The current mirrors M_1-M_2 and M_3-M_4 are stacked to form a double CCM. All the MOS devices are operated in saturation region.

The output resistance of FGMOS based double cascode current mirror is given as

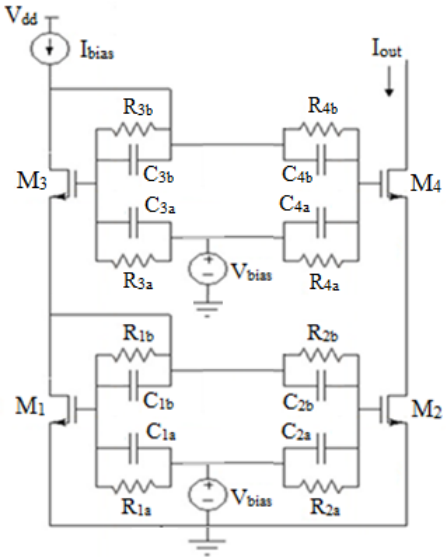
$$R_{out} = rds_4\{1 + (g_{m4} + g_{mb4}) * rds_2\} + rds_2 \tag{5a}$$

$$R_{out} \cong g_m * rds^2 \tag{5b}$$

The R_{out} is $g_m * r_{ds}$ times more than the basic current mirror.



(a)



(b)

Fig. 4 FGMOS based double cascode current mirror (a) schematic circuit (b) equivalent circuit

IV. IMPLEMENTATION AND RESULTS

The basic and double cascode current mirror circuits are implemented in Cadence design environment for 180 nm technology. The design parameters used for the implementation of current mirror circuits are given in Table I.

Table I Design parameters used for FGMOS based basic CM and double CCM implementation

Parameters	Basic CM	Double CCM
V_{dd}	+0.4 V	+0.4 V
V_{ss}	-0.4 V	-0.4 V
I_{ref}	10 µA	10 µA
$(W/L)_{1,2}$	2 µm/180nm	2 µm/180 nm
$(W/L)_{3,4}$	-	2 µm/ 180 nm
R_{1a}, R_{2a}	1 MΩ	1 MΩ
C_{1a}, C_{2a}	1 pF	1 pF
R_{1b}, R_{2b}	1 kΩ	1 kΩ
C_{1b}, C_{2b}	4 pF	4 pF
R_{3a}, R_{4a}	-	1 MΩ
C_{3a}, C_{4a}	-	1 pF
R_{3b}, R_{4b}	-	1 kΩ
C_{3b}, C_{4b}	-	4 pF

CM-Current Mirror, CCM-Cascode Current Mirror

From (3d) it is evident that V_{th} can be lowered by choosing appropriate values of C_1 and C_2. A plot showing the variation of V_{th} with respect to the bias voltage for FGMOS based CM obtained from dc simulation is given in Fig. 5.

The plots of I_{out} versus V_{out} for FGMOS based basic current mirror and double cascode current mirror for different values of V_{bias} are respectively given in Fig. 6 an Fig. 7. The increase in V_{bias} reduces the threshold voltage and the transistors will be in saturation for a reduced output voltages. The comparison of basic CM and double CCM circuits with FGMOS and without FGMOS for different performance parameters are given in Table II and Table III respectively.

Table II Comparison of simulated results for basic current mirror with FGMOS and without FGMOS

Parameter	Basic CM without FGMOS	Basic CM with FGMOS
Process Technology (nm)	180	180
V_{dd}	+1 V	+0.4 V
V_{ss}	-1 V	-0.4 V
V_{omin} (V)	0.5 V	0.2 V
R_{out} (Ω)	0.133 MΩ	1.66 MΩ
Power (µW)	55.3 µW	26.3 µW

Table III Comparison of simulated results for double cascode current mirror with FGMOS and without FGMOS

Parameter	Double CCM without FGMOS	Double CCM with FGMOS
Process Technology (nm)	180	180
V_{dd}	+1 V	+0.4 V
V_{ss}	-1 V	-0.4 V
V_{omin} (V)	0.6 V	0.3 V
R_{out} (Ω)	2 MΩ	3.33 MΩ
Power (µW)	66.4 µW	39.48 µW

The power consumed in gate driven and FGMOS based basic CM are respectively 55.3 µW and 26.3 µW respectively. The power consumed in gate driven and FGMOS based double CCM are found to be respectively 66.4 µW and 39.48 µW respectively.

V. CONCLUSION

The two types of current mirror circuits namely basic CM and double CCM circuits have been implemented using FGMOS in Cadence design environment and the simulation results have been analyzed and compared with gate driven current mirror circuits. The power reduction of 40% and 52.4 % are observed for double CCM and basic CM when FGMOS is used. It is evident from the simulation results that FGMOS based current mirror circuits exhibit reduced V_{omin} requirement and thus suited for low voltage and low power applications.

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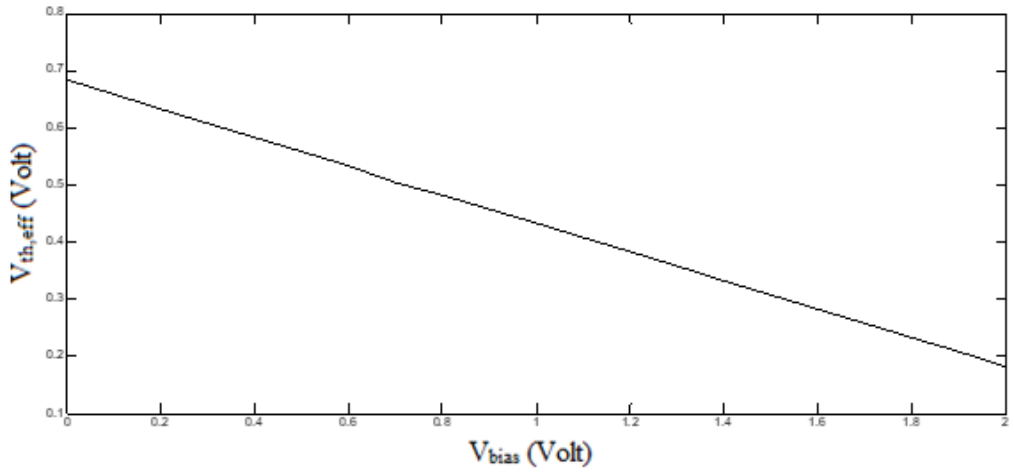

Fig. 5 Plot showing variation of $V_{th,eff}$ versus bias voltage for FGMOS based basic current mirror

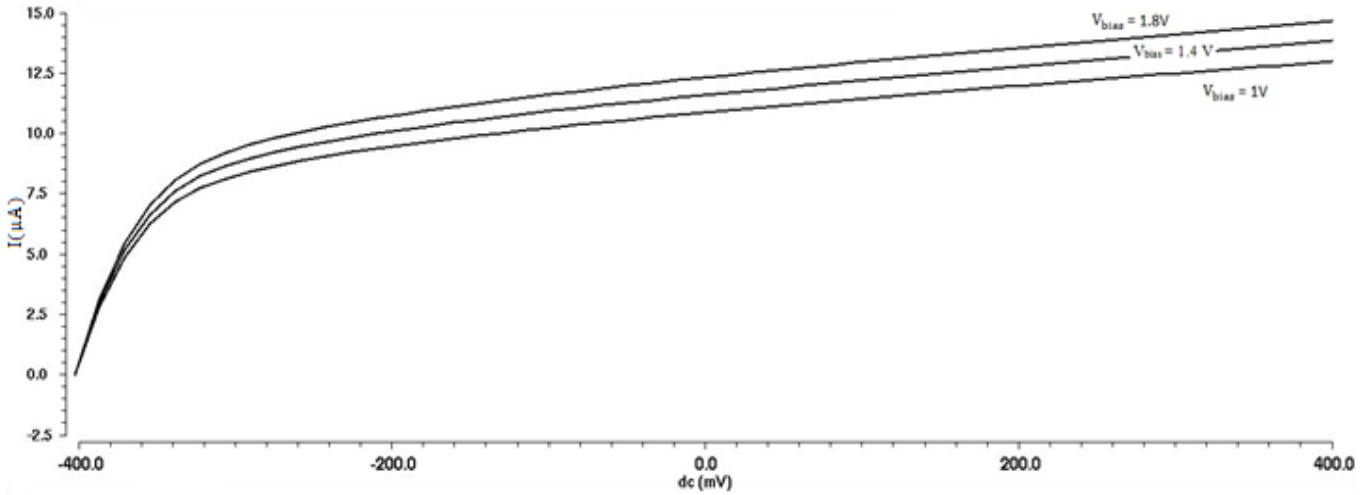

Fig. 6 Plot of I_{out} versus V_{out} for FGMOS based basic current mirror

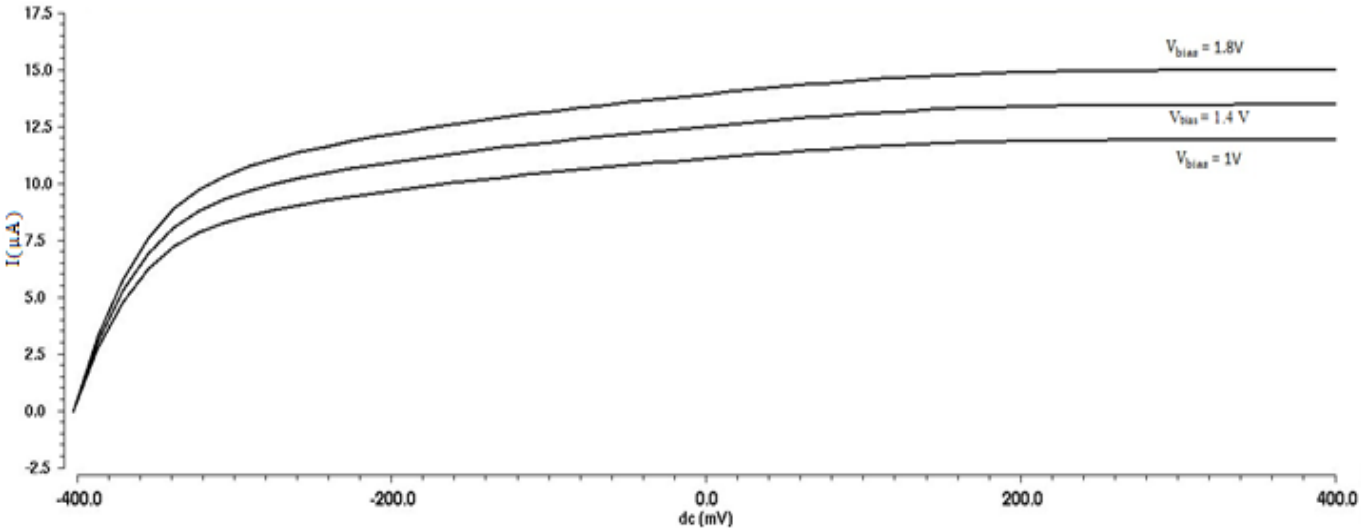

Fig. 7 Plot of I_{out} versus V_{out} for FGMOS based cascode current mirror