Computer-Aided VLSI System Design, Fall 2015

Verilog Homework 5 – **Testbench Writing in Verilog**

1. Objective

請完成Testbench來Debug計算對數(Exponential Function)之硬體設計

- 必需依照Specification完成 testbench (EXP_tb.v) 來測試有bug的 EXP.v
- 請修正這些錯誤，並於Console中顯示要求的資訊

2. Description of Exponential Function

「指數函數」為數學中重要的函數，數學表示為e^x也可寫作exp(x)。這裡的e是歐拉數，就是自然對數的底數，近似等於2.718281828，然而此無理數之運算是很難以硬體實現的。泰勒展示的發明給了無理數的運算一個契機，透過逐漸冪級數逼近來趨近e^x之值，e^x的泰勒級數展開為:

$$e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!} = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \frac{x^5}{5!} + \frac{x^6}{6!} + \cdots\cdots$$

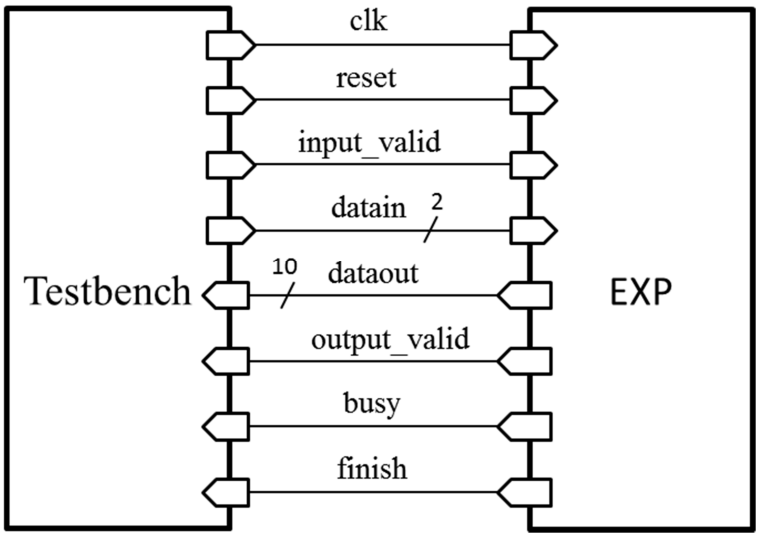
本設計再實現一個計算e^x之硬體，令硬體疊代輸出y為:

$$y^k = \sum_{n=0}^{k} \frac{x^n}{n!} = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \cdots\cdots + \frac{x^k}{\mathrm{k!}}$$

其支援的輸入$x \in (0,1,2,3)$，計算之$k \in (0,1,2,3,4,5,6,7,8,9)$，輸出y為5個bit整數+5個bit小數。

3. Hardware Specification

3.1 Block Diagram of System



圖一、Block Diagram

3.2 Input Signals and Output Signals

表一、Input/ Output Signal

Signal Name	I/O	Width	Simple Description
clk	I	1	The clock of system, all signal timing are related to the rising edge of clk.
reset	I	1	The reset is an **active high asynchronous signal**.
input_valid	I	1	Input data enable signal: input_valid=0(disable) input_valid=1(enable)
datain	I	2	2-bit input data of x. $x \in (0,1,2,3)$
busy	O	1	The busy signal of system. busy=0 (Host can input new data) busy=1 (Host cannot input new data)
dataout	O	10	10-bit output data of y. **dataout[9:5] → integer part** **dataout[4:0] → fractional part**
output_valid	O	1	Output control signal: output_valid=0 (invalid output data) output_valid=1 (valid output data)
finish	O	1	When system finish output y^0~y^9, finish signal should be sent. finish=1(accomplished) finish=0(processing)

3.3 Software Simulation

本次作業提供e^x運算之軟體模擬(Matlab檔)，軟體模擬已經對輸出y做fix-point analysis，可以當作design的golden value。軟體中預設是產生x=3之golden value，可以自行修改產生x=0,1,2之golden value。模擬之輸出為:

********** x=3 **********

k=0, exp_x_bin=0000100000

k=1, exp_x_bin=0010000000

k=2, exp_x_bin=0100010000

k=3, exp_x_bin=0110100000

…

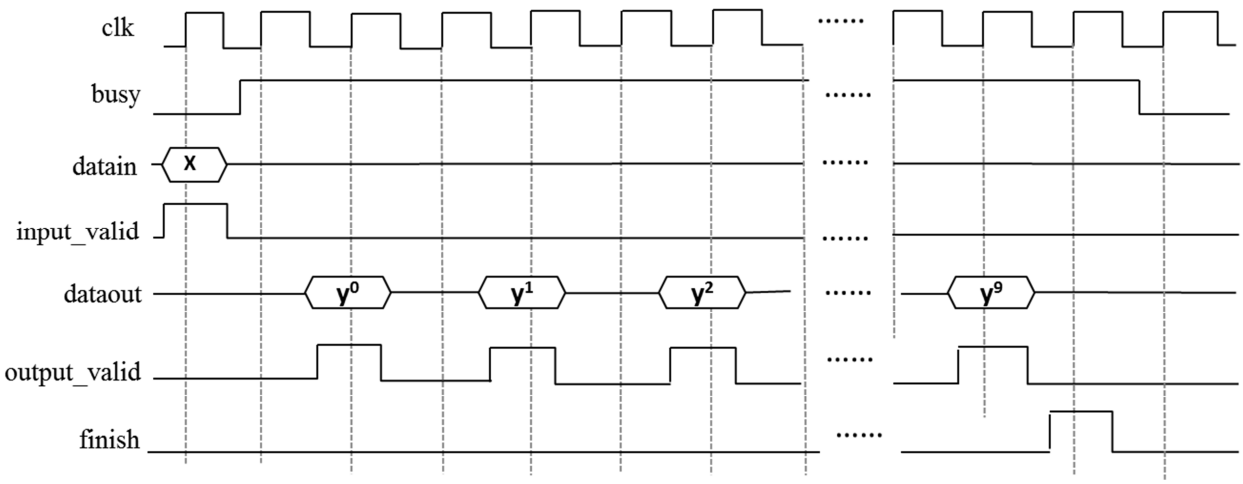
…

k=7, exp_x_bin=1001111011

k=8, exp_x_bin=1010000000

k=9, exp_x_bin=1010000010

3.4 Timing Diagram



圖二、訊號時序圖

- 當Testbench偵測到busy訊號為零時，將會讓input_valid=1’b1，並輸入datain。
- 於讀入datain後將busy訊號拉成1’b1，系統開始運算。
- 開始運算時，系統每隔2個cycle輸出一筆output (請自行看verilog中的Finite State Merchine來了解design控制)，並在輸出dataout時將output_valid=1’b1。
- 當電路輸出至y^9完成後，於下個cycle給finish=1’b1訊號，並將busy設成1’b0。
- 當Testbench偵測到busy訊號為零時，將輸入下一筆新的x。

請完成Testbench撰寫來控制Design完成上述時序，比較輸出與golden value相同與否來debug

3. Testbench Requirement

需於 Testbench 中顯示下列字串:

- 測試 x=3:

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                          x = 3

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Pass ! k=   0 ;Dataout=  0000100000 ; ANS= 0000100000
Pass ! k=   1 ;Dataout=  0010000000 ; ANS= 0010000000
Pass ! k=   2 ;Dataout=  0100010000 ; ANS= 0100010000
Pass ! k=   3 ;Dataout=  0110100000 ; ANS= 0110100000
Pass ! k=   4 ;Dataout=  1000001100 ; ANS= 1000001100
Pass ! k=   5 ;Dataout=  1001001100 ; ANS= 1001001100
Pass ! k=   6 ;Dataout=  1001101100 ; ANS= 1001101100
Pass ! k=   7 ;Dataout=  1001111001 ; ANS= 1001111001
Pass ! k=   8 ;Dataout=  1001111110 ; ANS= 1001111110
Pass ! k=   9 ;Dataout=  1001111111 ; ANS= 1001111111
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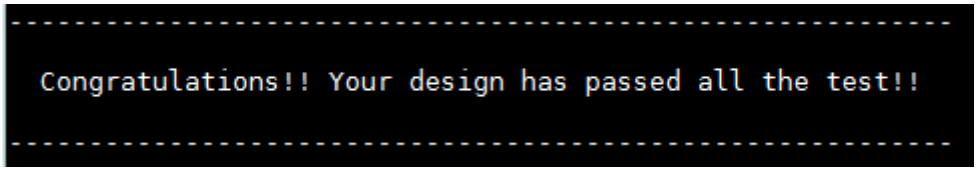
- 所有 x=0,1,2,3 測資都正確:



4. Grading Policy

(70%) For correctness on Testbench control
(20%) For correctness on EXP.v
(10%) For showing of Testbench requirement

5. Submission Requirements

File submission: **1.EXP.v (no errors)**, **2.EXP_tb.v**

Please submit your design in one file with the naming convention:
StudentID_HW5_vk.zip *(k is number of version, k=1,2,…).*
Please follow the electronic submission guideline (available on website).

6. Submission Deadline: 12/08 18:00

Appendix: 檔案說明

檔名	說明
EXP_tb.v	空的測試樣本檔，需完成此測試樣本來測試 EXP.v。
EXP.v	有錯之 Verilog 檔。
exp.m	Matlab 模擬檔，此檔提供正確的輸出資料(golden value)。