(b) Each stage requires one clock cycle;

(c) All memory references hit in cache;

(d) The following program segment should be processed :

```
    //ADD TWO INTEGER ARRAYS
    LW R4# 400
L1 : LW R1, 0 (R4)        ; Load first operand
     LW R2, 400 (R4)      ; Load second operand
     ADDI R3, R1, R2      ; Add operands
     SW R3, 0 (R4)        ; Store result
     SUB R4, R4, #4       ; Calculate address of next
                            element
     BNEZ R4, L1          ; Loop if (R4) ! = 0
```

(i) Calculate how many clock cycles will take execution of this segment on the regular (no pipelined) architecture. Show calculations.

(ii) Calculate how many clock cycles will take execution of this segment on the simple pipeline without forwarding or bypassing when result of the branch instruction (new PC content) is available after WB stage.

Roll No. ..... Total Pages : 05

Sep-21-00041

B. Tech. EXAMINATION, 2021

Semester III (CBCS)

COMPUTER ARCHITECTURE & ORGANIZATION

(CSE, IT)

CS-303

Time : 2 Hours *Maximum Marks : 60*

The candidates shall limit their answers precisely within 20 pages only (A4 size sheets/assignment sheets), no extra sheet allowed. The candidates should write only on one side of the page and the back side of the page should remain blank. Only blue ball pen is admissible.

Note : Attempt *Four* questions in all, selecting *one* question from any of the Sections A, B, C and D. Q. No. **9** is compulsory.

Section A

1. Explain shift micro operation in detail. Also draw and explain 4-bit combinational circuit. **15**

Or

2. (a) Explain the overflow condition in arithmetic shift micro operation. **7½**

(b) Multiply 14 times -5 using 5-bit numbers using Booth's algorithm (10-bit result). **7½**

Section B

3. (a) Define a stack. How can it implemented ? Give one example use of stack. **7½**

(b) What is the difference between direct and indirect addressing modes ? How many references to memory are needed for each type of addressing to bring the operand into a processor register ? **7½**

Or

4. (a) Discuss the relative advantages of CISC processor and RISC processor. **7½**

(b) What is the difference between a microprocessor and a microprogram ? Is it possible to design a microprocessor without a microprogram ? **7½**

Section C

5. (a) Explain various mechanisms of data transfer from a peripheral device. **7½**

(b) Explain Direct Memory Access. Explain *one* practical example of DMA. Why does DMA have priority over the CPU when both request a memory transfer ? **7½**

Or

6. (a) What is cache memory mapping ? Explain direct cache memory mapping in detail. **7½**

(b) Differentiate isolated I/O and memory mapped I/O. **7½**

Section D

7. Discuss Flynn's classification of parallel architecture with diagram. Enlist the differences between SISD and SIMD. **15**

Or

8. For all the following questions we assume that : **15**

(a) Pipeline contains 5 stages : IF, ID, EX, M and W;

(Compulsory Question)

9. Short answer type questions : **1½×10=15**

(i) Specify the three types of the DMA transfer techniques.

(ii) What are the registers generally contained in the processor ?

(iii) What is elapsed time of computer system ?

(iv) Write down the steps for restoring division and non-restoring division.

(v) How bit pair recording of multiplier speeds up the multiplication process ?

(vi) What are the steps required for a pipelined processor to process the instruction ?

(vii) What is big endian and little endian format ?

(viii) What is the need for adding binary 8 values to the true exponential in floating point numbers ?

(ix) What is skipping over of one's in Booth decoding ?

(x) What are the steps for execution of a complete instruction ?