[Total No. of Questions - 9] [Total No. of Printed Pages - 3]
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B. Tech 3rd Semester Examination

Computer Organisation & Architecture (NS)

CS-212

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all, by selecting at least one question from Sections A, B, C and D. Question no. 9 of Section E is compulsory.

SECTION - A

1. (a) Explain multiplication algorithm to multiply two signed binary numbers with suitable examples. (10)

   (b) (i) Explain the difference between logical shift and arithmetic shift.

   (ii) What are the characteristics of Von Neumann Model? (5+5=10)

2. (a) What is the need of multiplexing? Give logic diagram of 8-input multiplexer. (10)

   (b) The memory unit of a computer system has 256 K words of 32 bits each. The computer system has instruction format with four fields: an operation code field, a mode field to specify one of the seven addressing modes, a register field to specify one of the 60 registers and an address field. Draw the instruction word format if one instruction is stored in a memory location. Also find the number of bits in Program Counter and Instruction Register. (10)

SECTION - B

3. (a) (i) Differentiate between machine cycle and instruction cycle.

   (ii) What is the basic difference amongst branch instruction, a call subroutine and program interrupt? (5+5=10)

   (b) Write notes on:-

   (i) RISC Pipeline (ii) Vector Processing (5+5=10)

4. (a) (i) What are the various flags present in a typical CPU? Explain their importance.

   (ii) Differentiate between stack top and stack pointer. (5+5=10)

   (b) What is addressing mode? Explain different addressing modes. (10)

SECTION - C

5. (a) Explain different mapping procedures followed while designing Cache Memory. (10)

   (b) What is associate memory? Explain its use in a computer system. (10)

6. (a) (i) If cache hit ratio = 75%, cycle time of Main Memory and Cache Memory is 10 ns and 4 ns respectively, then what will be the effective memory cycle time?

   (ii) Write a note on virtual memory. (5+5=10)

   (b) (i) What is redundant array of inexpensive disks? Explain its levels.

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(ii) How the performance of main memory can be improved by using interleaved memory. (5+5=10)

SECTION - D

7. (a) Give and explain Flynn classification of computers. (10)

   (b) Explain multiprocessor cache coherence problem and its solutions. (10)

8. Write a note on:-

   (i) Instruction-Level Parallelism .

   (ii) Interconnection Networks.

   (10+10=20)

SECTION - E

9. (a) Convert $(175)_{10}$ into Hexadecimal and Binary.

   (b) Explain FIFO and Least Recently Used algorithms used in Cache operation.

   (c) What are the steps involved in the instruction execution?

   (d) What is the difference between the restoring and non restoring methods of division?

   (e) What is microprogramming?

   (f) What are the features of RISC?

   (g) Do the operation:- **32-45** using 2's complement

   (h) What is superscalar machine?

   (i) Differentiate between Static and Dynamic Memories.

   (j) Why are decoders used in digital systems? (2×10=20)