[Total No. of Questions - 9] [Total No. of Printed Pages - 3] (2125)

15332

B. Tech 7th Semester Examination

Advanced Computer Architecture (NS)

CS-412/IT-414

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Candidates are required to attempt five questions in all selecting one question from each of the section A, B, C and D of the question paper and all the subparts of the question in section E. Use of non-programmable calculator is allowed.

SECTION - A

1. Characterize the architectural operations of SIMD and MIMD computers. Distinguish between multiprocessors and multicomputer based on their structures, resource sharing, and intercrosses communications. Also, explain the differences among UMA, NUMA, and COMA, and NORMA computers. (20)

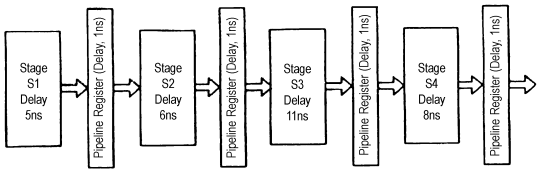
2. (a) Explain how instruction set, compiler technology, CPU implementation and control, and cache and random hierarchy affect the CPU performance. Justify the effects in terms of program length, clock rate and effective CPI. (10)

   (b) Explain the terms data dependence and resource dependence. Also, explain, how these dependencies is utilized to enhance the degree of parallelism. (10)

[P.T.O.]

SECTION - B

3. (a) Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure:



   What is the approximate speed up of the pipeline in steady slate under ideal conditions when compared to the corresponding non-pipeline implementation? (10)

   (b) Describe the architecture of a typical superscalar VLIW processor with the help of block diagram. (10)

4. Consider the non-pipelined processor introduced previously. Assume that it has a 1 ns clock cycle and it uses 4 cycles for ALU operations and branches, and 5 cycles for memory operations, assume that the relative frequencies of these operations are 40%, 20%, and 40%, respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline? (20)

SECTION - C

5. (a) Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching. (10)

   (b) Briefly compare CISC, RISC and VLIW architecture. (10)

6. (a) What do you mean by coherence property? Write down the different methods to retain this property. (10)

   (b) A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. Find the number of bits in the tag field of an address. (10)

SECTION - D

7. (a) Comment on the use of 'scatter-gather' operation and the use of vector masks in a vector processor. (10)

   (b) What are the advantages and disadvantages of software-based and hardware based speculation mechanism? (10)

8. Explain CM-5 architecture with block diagram and compare it with CM-2 architecture. (20)

SECTION - E

9. Write short note on following:

   (a) Serial versus parallel processing.

   (b) CISC.

   (c) Data flow architecture.

   (d) Cluster Computers.

   (e) Reduction Computers.

   (f) Crossbar networks.

   (g) System efficiency and speedup.

   (h) Locality of reference.

   (i) Cache coherence.

   (j) Gustafron's Law for sealed problems. (10×2=20)