

Implement the following design using Verilog HDL. Download **shifterAndALU.v** file. Modify **shifterAndALU.v** to get the desired waveform in GTKWave as shown below.

Explanation of the circuit:

The circuit basically takes two input numbers and these inputs are provided to ALU, which performs a particular arithmetic operation, described in the first column of operation table, and to Barrel Shifter, which performs a particular shift operation on 'inp1' as described in the third column of operation table. The operation to be performed is described by the 'oper' input signal. The output signal of the circuit is decided by the 2 to 1 multiplexer. Shift Amount is decided by 2 to 1 multiplexer which multiplexes 'ShiftImm' input signal and least significant three bits of 'inp2'.

Example : -

Inp1 = 80

Inp2 = 20

Oper = 001

ShiftImm = 2

selShiftAmt = 1

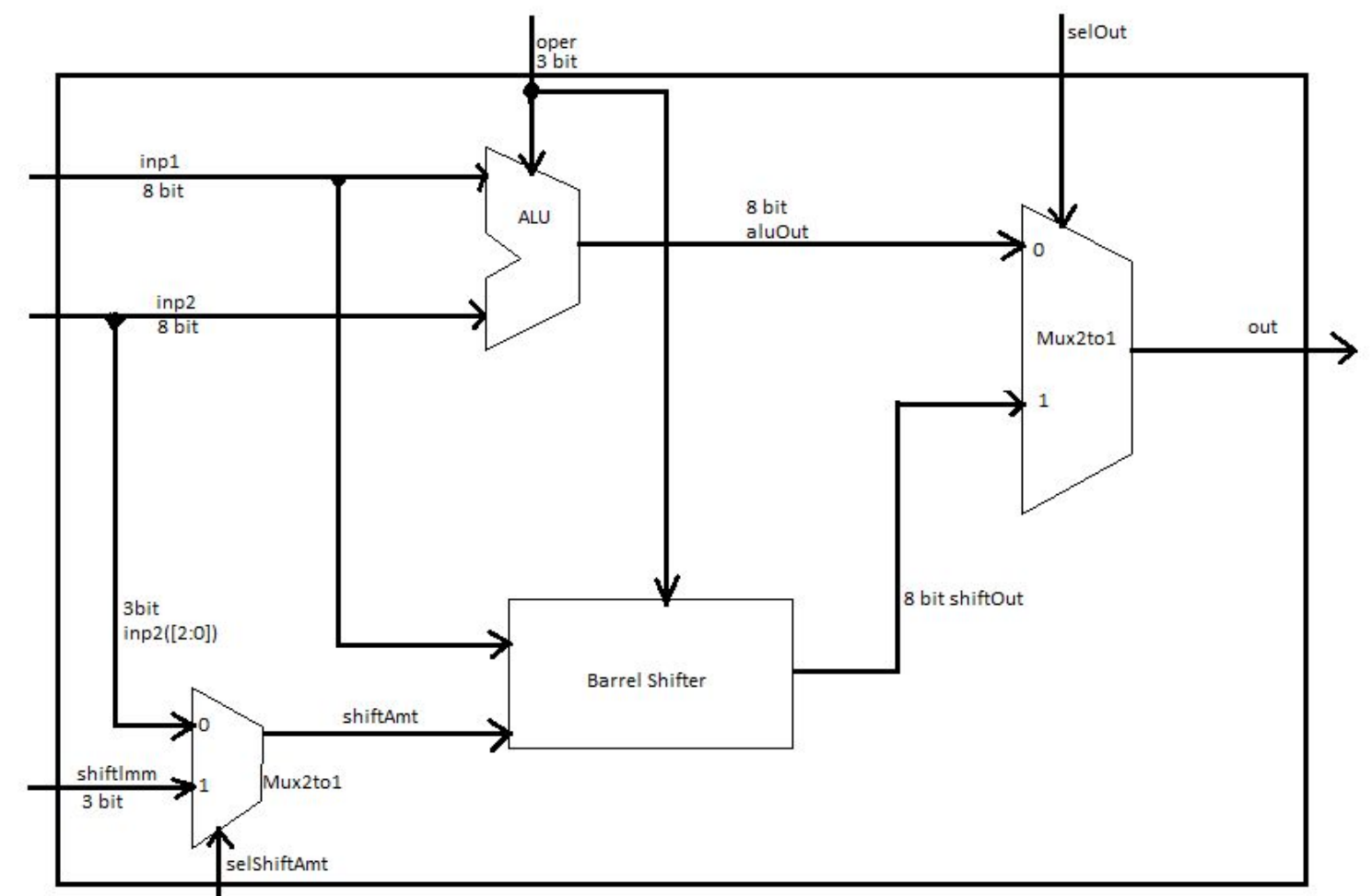
aluOut = $20 + 80 = 100$ (Add operation)

shiftOut = 20 (Arithmetic Shift right of 80 by 2 places)

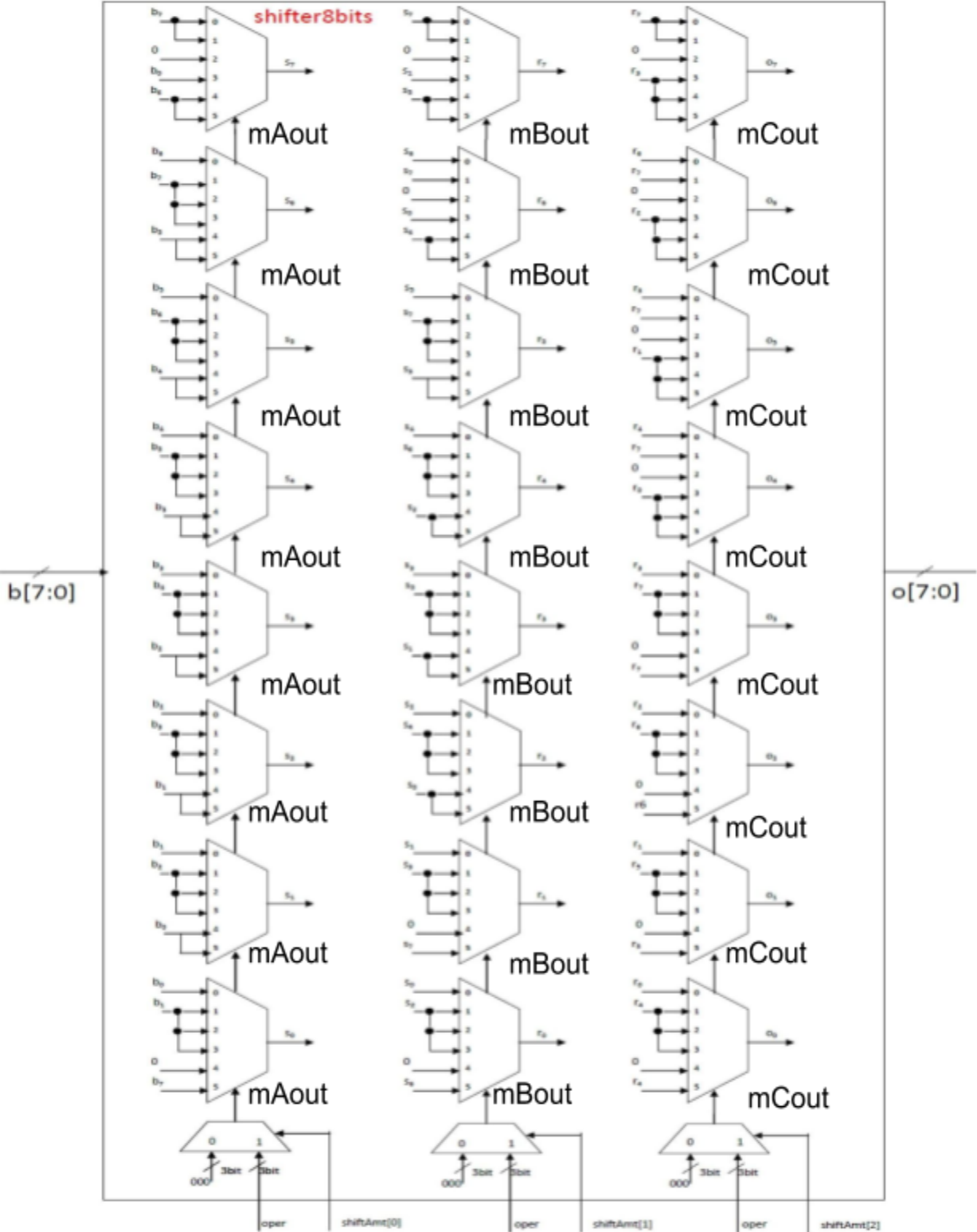
If selOut = 0 then out = aluOut

If selOut = 1 then out = shiftOut

ShifterAndALU Circuit:



Barrel shifter: <https://drive.google.com/file/d/1VXVuiHVDLFdYK9qKuFsJthJFQmJAMsgJ/view?usp=sharing>



Operations table:

oper	ALU operation	Barrel Shift Operation
000	aluOut=Reg(inp1)	NO SHIFT
001	ADD	Arithmetic shift right
010	SUB	Logical shift right
011	Bitwise AND	Circular shift right
100	Bitwise OR	Logical shift left
101	NOT(inp1)	Circular shift left

WaveForm:

<https://drive.google.com/file/d/1W6b8NIIC4Z4yKoxO17utJuCcXSkgtbef/view?usp=sharing>



Marks breakup:

- 1 mark - out signal
- 2 marks - shiftOut signal
- 1 mark - aluOut signal

Submission Method:

- 1) Save your shiftAndAlu.v file as **YourIdNo_Lab1.v** example 2017A7PS0105G_Lab1.v.
- 2) Save your gtkwave output in as **YourIdNo_Lab1.gtkw** example 2017A7PS0105G_Lab1.gtkw by using the 'save as' option in File->Write.

Submit two separate files on the two links provided on course webpage on Quanta LMS