Project- Room occupancy counter

COEN 313

Anthony Aldama

40226191

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I certify that this submission is my original work and meets the faculty expectation of originality

-anthony Aldama 11/24/2023

Contents

Introduction

In the scope of this project, the task to design, make and implement a counter was given. The use of said counter will be to keep track of the occupancy of a room and indicate trough a LED – output when the occupancy reached its maximum. the following constrain were given:

1-a register that keeps track of the maximum of occupant

2-the maximum of occupant cannot surpass the number 63

Once the design is done, we will have to provide the following:

1-a clearly identified conceptual diagram for the VHDL

2-a pertinent testbench that cover enough scenario to prove the usefulness of the VHDL program

3-a simulation and synthesis result

4-a short discussion that discusses the quality of the design

Theory

In this section I will discuss choices for the VHDL code in order to

In order to implement the design , a schematic will need to be created

The design had the following inputs in data type std_logic:x,y,clk,reset and an input max_occupency in data type unsigned(5downto0) , the reason for that is because of the limit max occupancy is 63, translating to 111111 in unsigned binary number.

It only had the output z, that when turned to 1, will produce the LED output to indicate the room is full.

Many component were created in order to accomplish this project, in this section they will be described with their use

MUX

Signal x and y will go through a mux that will determine the next operation, this mux will also have input in itself of the occupancy register. If x =1 and y=0 , this occupancy will be incremented, if x=0 and y=1 , it will be decremented, otherwise it will remain the same

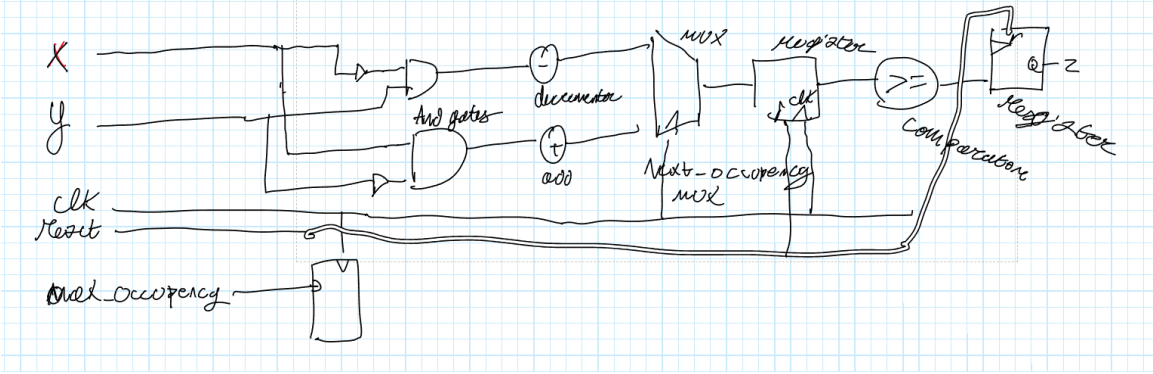
Register

2 registers will be used, on to store the maximal possible value of occupancy, while the other one will be used to store the current occupancy

Comparator

Finally a comparator will compare value stored in the max occupancy register to the current value of occupancy and will produce the output, z=1 if the occupancy is bigger than the maximum.

Figure 1- Conceptual diagram



Procedure

In order to accomplish this project , multiple step were required

<u>1-preparation</u>

1. Correctly read the assignment given while gathering ressources from the course that may be helpful
2. Determine a process that will accomplish the asked task

<u>2-execution</u>

1. Create a initial VHDL file
2. Create a testbench
3. Simulate the testbench through modelsim

<u>3-adaptation</u>

1. Identifie any potential error in the simulation from the testbench
2. Rectifies these error

<u>4_final design</u>

1. With the final code for testbench and schematic, run a simulation

2. Adapt the conceptual diagram to the final design
3. Run the synthesis and implementation of the project on Xilinx

Result

A VHDL process and a corresponding testbench were successfully created. This section will cover the result generated.

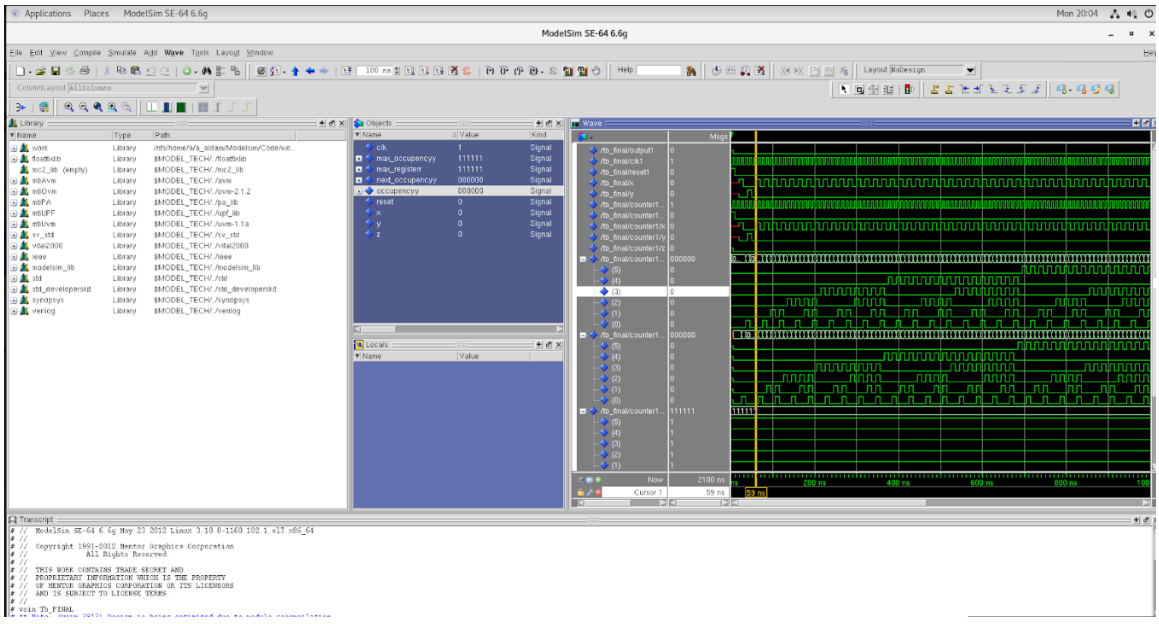
Modelsim simulation

In order to ensure the code was working properly, we ran modelsim simulation with the testbench file created, intituled Tb_FINAL.vhd

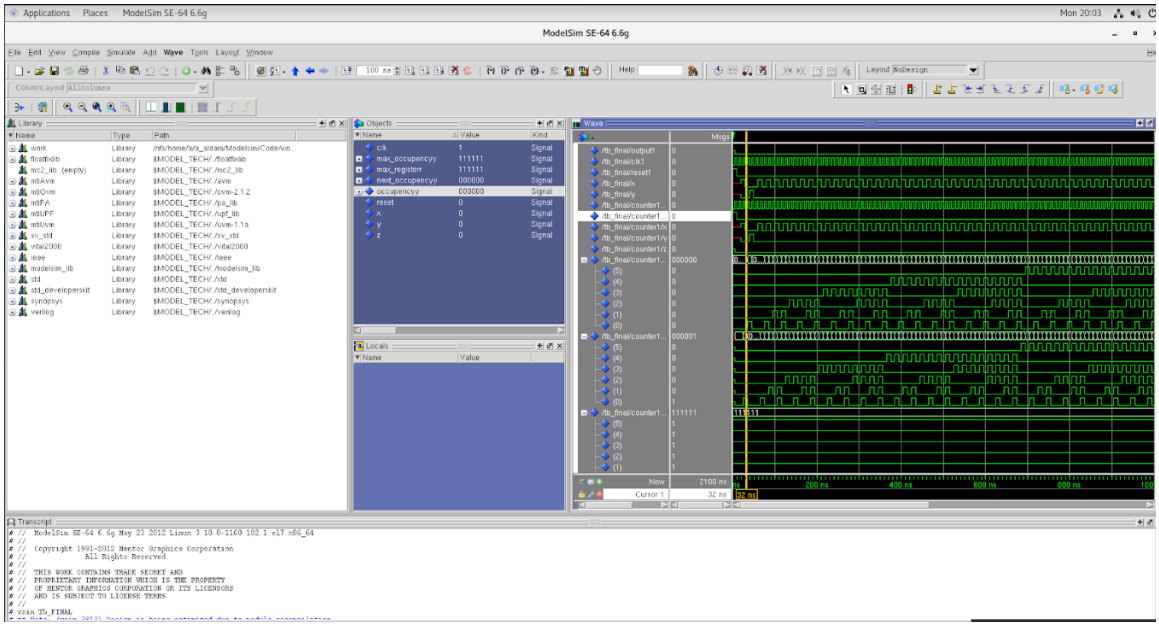
Here are the initial results after running the testbench multiple times

Figure 2-Modelsim simulation of testbench

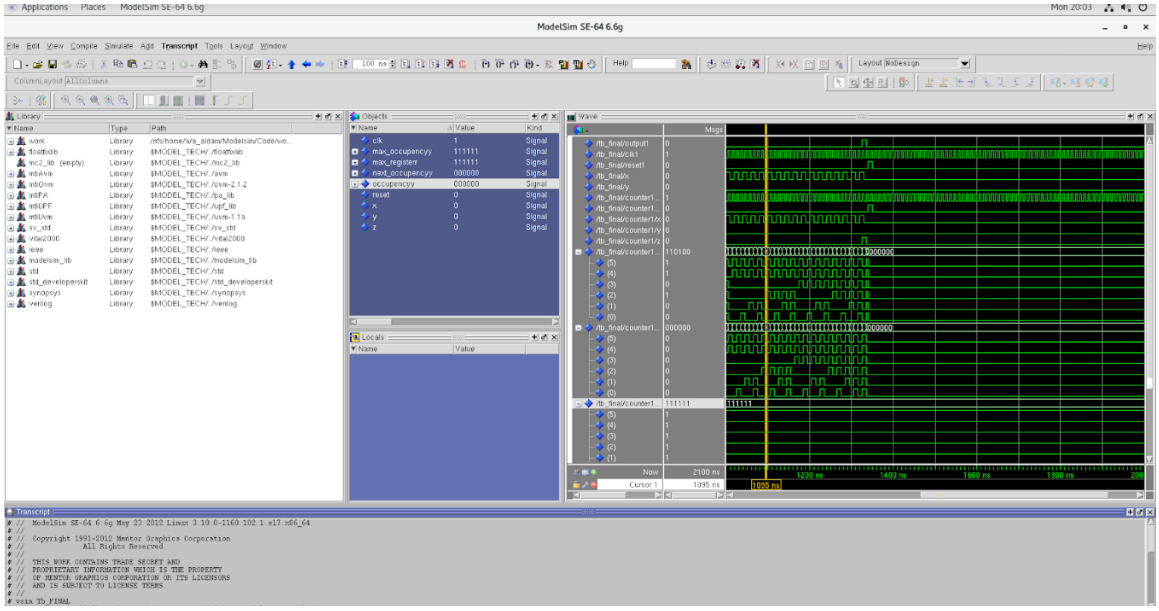
a)



b)


Applications Places ModelSim SE-64 6.6g
ModelSim SE-64 6.6g
Library
Objects
Locals
Wave
Transcript

c)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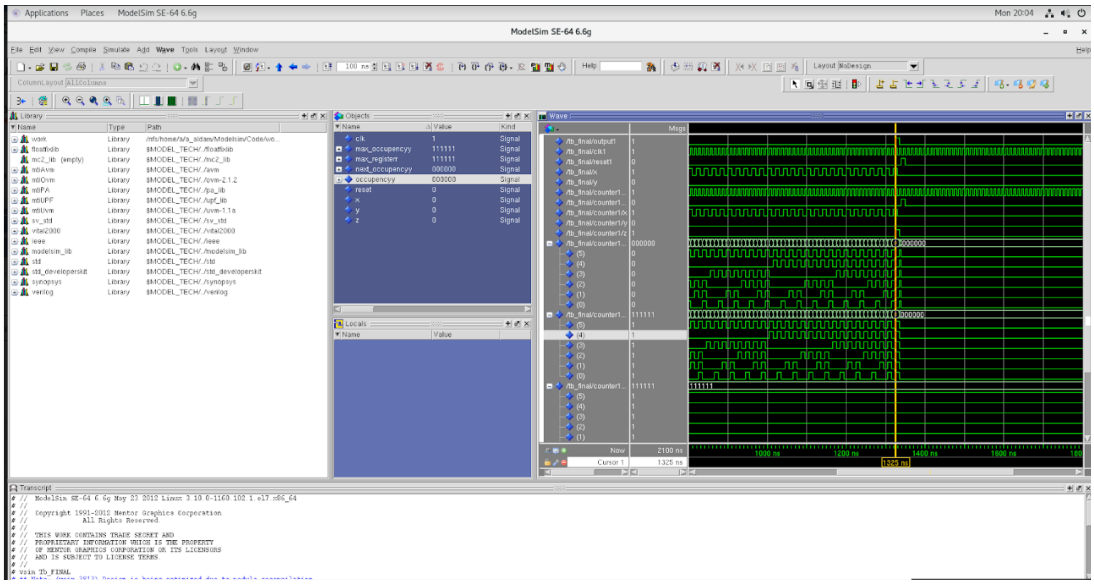
d)



It is possible to verify that many of the operations work correctly, in a) that the decrement and decrement work correctly, in b) is the previous to a) , it can be observed that b) incremented to one and in a when y=1 it is decremented, in c) it is observed that z is now 1 when the max is reached and finaly in d the values are reseted

We were able to observe all the function expected of the system in the Modelsim simulations.

Xilinx synthesis and implementation

It was required to run a simulation and implementation of the code

The synthesis and implementation were successfully performed on vivado

The schematic obtained corresponded to the design showed in the first figure, its is composed of a MUX, two register and a comparator.

DISCUSSION

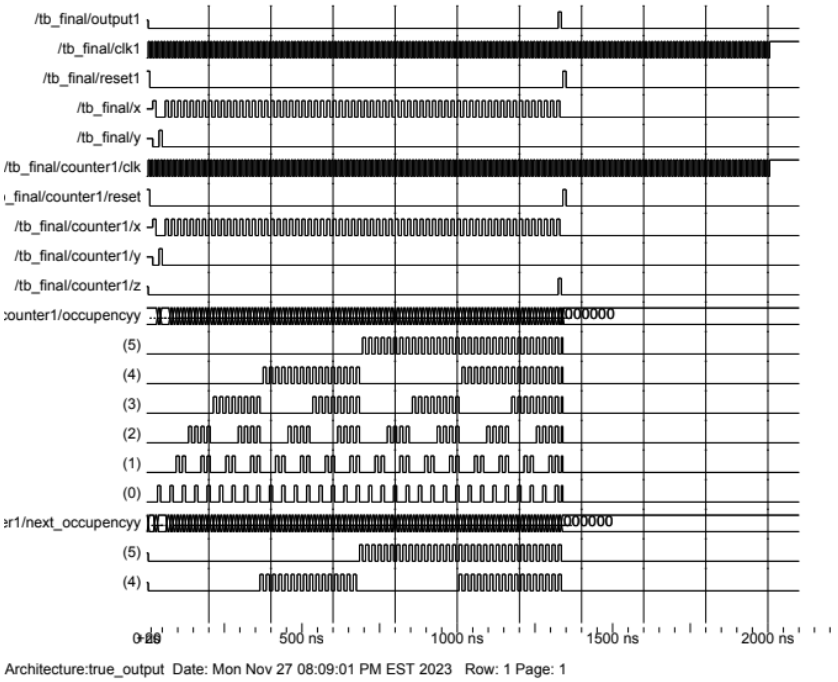
On a fpga board, the resources will be used efficiently with this design and it is executed fastly.

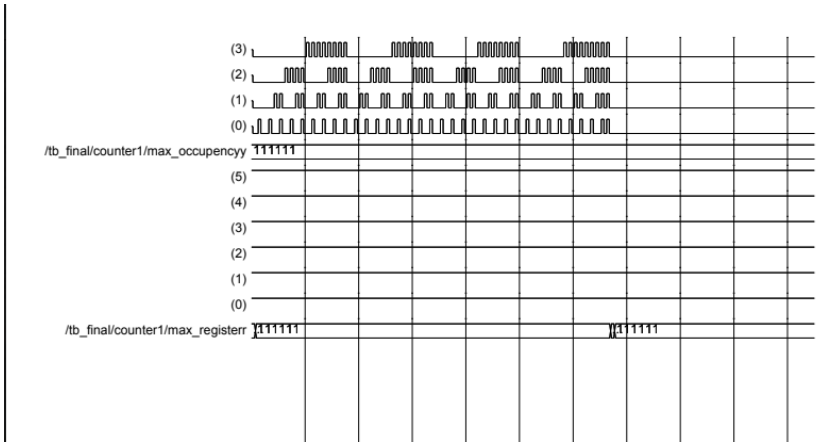
Conclusion

In conclusion, I used the knowledge learnt in the COEN 313 course and in the laboratories in order to accomplish this project, a design capable of respecting all the constraint was designed, simulated, synthetized and implemented. Through this project I learned a lot about VHDL and helped me better understand its use for future project may they be in a workplace, in a academic setting or a personal project

Appendix

Modelsim complete wave files





Vivado elaborated design