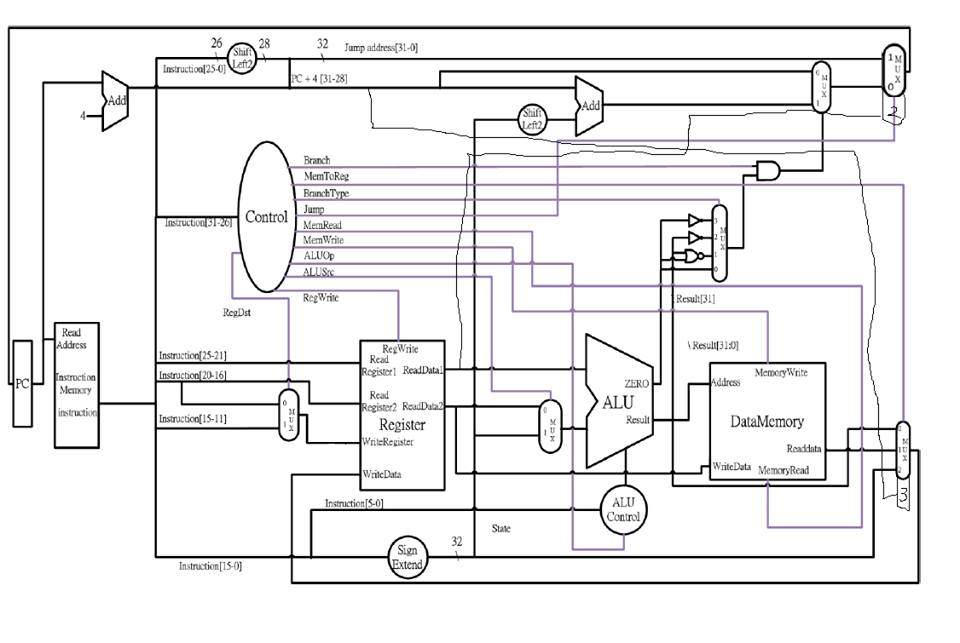
**­Computer Organization**

**Architecture diagrams:**



**Hardware module analysis:**

In this assignment, we add the module DataMemory into our previous LAB02 project. Some multiplexers and sign-extension module also inserted to our new architecture.

The relation between modules are almost the same with the previous lab. However, LAB03 we add a DataMemory which enables us to store and load data to memory.

**Experiment result:**

Based on lab2, we modified our programme architecture and added some new functions to it according to the requirements. We implemented the basic part, the advanced part as well as the bonus parts.

**Problems you met and solutions:**

For us, the most difficult part was job distribution. It’s not always easy to separate our work without interfering with each other. We spent extra time on job distribution in a way that is efficient and less prone to confusions. We used msysgit to help us trace our codes and it worked out really well.

Others problems might be small bugs on the codes, such as forget to change the size of a wire used in previous lab or typo.

**Summary:**

**0016328江振皓:** Through this lab, I had a better understanding of the relationships between the modules and learnt various skills of debugging with the aid of the waves. I also realised the importance of communication skills in teamwork.

**0016110 洪茂榮:**

I got a better understanding of how a simple CPU works. In the programming side, I got more familiar with Verilog and inter-modules relations and also the IDE which is Model SIM. Moreover, translating from C code into Assembly and further into MIPS machine code brings me a whole picture of CPU!

I also learnt a lot in how to use GIT as our version control software properly.

**Job distribution:**

**Basic – 0016110 洪茂榮**

**Advanced – 0016328 江振皓**

**Bonus 1 – 0016328 江振皓**

**Bonus2 – 0016110 洪茂榮**