9/10/2023

In Fall 2023, we started adding files to support the use of the A7 board besides the N4 board.

In a year, we will move to all A7 board.

While the .xdc file has several changes needed to port to A7 from N4,

the top Verilog file needs only a single change of removing "MemOE, MemWR, RamCS" while moving from the \_N4 to \_A7 top file.

The zip file should contain the following 11 files   
including this number\_lock\_verilog\_README.docx file.

