

ANTHONY HERMEZ

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EDUCATION

The University of Texas at Austin – Austin, Texas

Master of Science in Electrical and Computer Engineering

May 2026

GPA: 4.00

Bachelor of Science in Electrical and Computer Engineering

May 2025

Bachelor of Science in Mathematics

May 2025

Minor: Computational Science and Engineering

Relevant Graduate Coursework:

ASIC Design Lab, Computer Architecture for Machine Learning, Parallel Computer Architecture, Advanced MCU Systems, VLSI, Operating Systems, Computational HW/SW Co-Design for HPC, Numerical Linear Algebra, Tensor Processing Methods

SKILLS

Design: VHDL, Verilog, SystemVerilog, UVM, Genus, Innovus, Tempus, Voltus, Virtuoso, Primetime, Verdi, Indago, Vivado

Programming: C, C++, Python, ARM Assembly, Embedded C, BASH, MPI, CUDA, PyTorch

Protocols: AXI, UART, SPI, I2C

EXPERIENCE

Applied Research Laboratories – Austin, Texas

June 2025 – Present

FPGA Engineer Intern

- Designed RTL for ECC decoding for a low-SNR RF application in VHDL on a Zynq UltraScale+ FPGA.
- Analyzed multiple ECCs across code rates, BERs, and computational complexity to contribute to system design decision.

Apple – Austin, Texas

May 2024 – August 2024

SoC Design Verification Engineer Intern

- Developed a complete UVM testbench for a distributed MMU IP at RTL level in SystemVerilog.
- Leveraged Cadence Verification IP to control AXI bus transactions.
- Wrote timing assertions in a full-chip SoC IP.

Texas Instruments – Dallas, Texas

May 2023 – August 2023

Validation Engineer Intern

- Designed and simulated an analog circuit that isolates high voltage from a temperature forcing unit.
- Captured final design in Altium to be printed and surge tested before use.

Applied Research Laboratories – Austin, Texas

June 2022 – December 2022

Embedded Software Engineer Intern

- Programmed firmware in C++ for a high-frequency radio-link simulator to interface with analog and digital attenuators.

PROJECTS

Google Tensor Processing Unit

Spring 2025

- Designed a TPU in SystemVerilog from RTL into a low-power ASIC design using Cadence/Synopsys flows.
- Architected a 5-instruction CISC ISA and wrote a TPU compiler in Python.
- Validated ASIC with host FPGA via a serial scan chain interface on a custom PCB testing board developed in Altium.

HPC Ordinary Differential Equations HW Accelerator

Spring 2024

- Implemented a novel, single-precision FP RK4 numerical ODE accelerator in Verilog on a Zynq UltraScale+ FPGA.
- Interfaced FPGA to physics application via Linux kernel modules, achieving 600% speedup.

Laser Tag on a Budget

Spring 2023

- Wrote firmware in C on an ARM M0-based μ C for radio, audio, and display to recreate a multiplayer laser tag game.

CPU Cycle-Level Simulator

Fall 2022

- Programmed a cycle-level simulator in C for the LC-3b, a 16-bit processor.
- Developed microarchitecture for the LC-3b datapath to handle interrupts and exceptions.

LEADERSHIP

Graduate/Undergrad TA: *Intro to Embedded Systems, Intro to Computing, Intro to Professional Engineering* 2022 – Present

Freshman Mentor: *First-year Interest Group (FIG) Leader, ECE Amplify Leader, FIG Mentor of the Year (2022)* 2022 – 2024

Eagle Scout 2021