

CMOS INVERTERS AND THEIR VOLTAGE TRANSFER CHARACTERISTICS (VTC) DESIGN, SIMULATION, EXPERIMENTAL TEST, AND ANALYSIS

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Abstract—Upon studying the basic structure and function of the NMOS and PMOS transistor, we study its voltage transfer characteristics when implemented as a complimentary MOS (CMOS). Noise margins, propagation delay and the switching threshold (V_m) are all looked at in this report. Simulations done in Pspice are shown as well as their experimental counterparts.

Index Terms—CMOS, NMOS, PMOS, High & Low Noise Margins (NM_H and NM_L respectively), Propagation Delay, Switching Threshold (V_m).

I. INTRODUCTION

The complimentary MOS or CMOS is one of the most fundamental implementations of the CMOS and PMOS transistors. CMOS digital circuits utilize NMOS and PMOS transistors operating as switches.

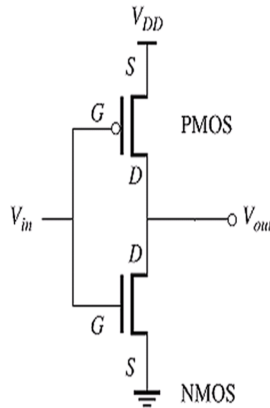


Figure 1. CMOS inverter schematic

An NMOS transistor will behave similar to a closed switch, exhibiting a small resistance between the drain and source when its gate voltage is "high" (logic 1). Conversely, when the gate voltage is "low" (logic 0), the transistor acts as open switch and the transistor is cut-off. The PMOS works in a similar fashion only in reverse. When we use these inverters in this way, with the PMOS on top of the NMOS (shown in

figure 3), the CMOS will invert the input which is what is demonstrated in figure 4.

	Channel OFF	Channel ON
PMOS	$V_{gs} > V_{Tp}$ or $V_{in} > V_T + V_{DD}$	$V_{gs} < V_T$ or $V_{in} < V_T + V_{DD}$
NMOS	$V_{gs} < V_{Tn}$ or $V_{in} < V_{Tn}$	$V_{gs} > V_T$ or $V_{in} > V_{Tn}$

Figure 2. Relationship between the gate-source voltage V_{gs} and the threshold voltage V_t

A. Propagation Delay and Noise Margins

The propagation delay describes the amount of time between the change of the input and output at the 50% point. These measurements are taken when the output changes from high to low and from low to high since the propagation delays are usually not equal. The two values are then averaged out, giving us the following equation:

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} \quad (1)$$

Noise margins describe a "safety margin" to prevent the circuit from producing incorrect outputs due to a noisy input signal. Noise margins tell us the ranges we should be in to allow the circuit to work properly given a certain amount of noise. Noise margins are given for both high and low input levels are given by:

$$NM_L = V_{IL} - V_{OL} \quad (2)$$

$$NM_H = V_{OH} - V_{IH} \quad (3)$$

II. PROCEDURES, SIMULATION AND EXPERIMENTAL SET-UP

A. Case 1 ($100\text{kHz} \leq f \leq 200\text{kHz}$)

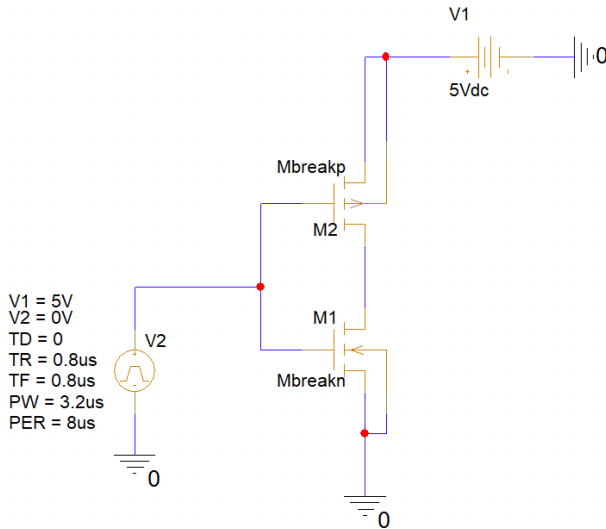


Figure 3. Case I - 5V, 122kHz Rectangular input

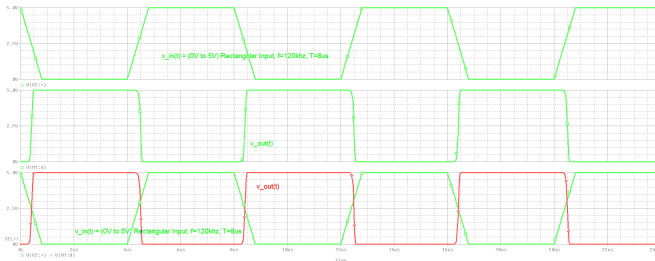


Figure 4. Case I - 5V, 124kHz Rectangular input, simulation

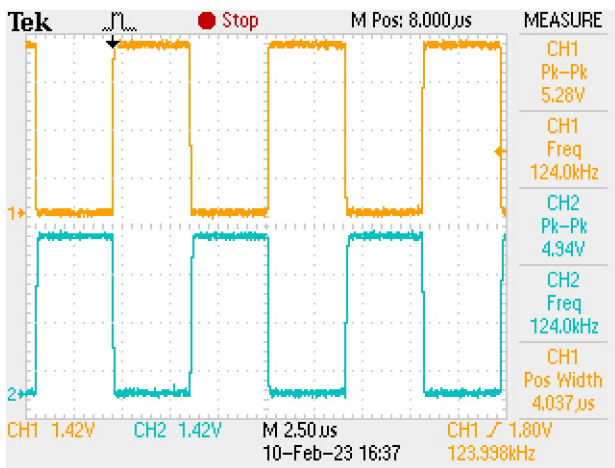


Figure 5. Case I - 5V, 124kHz Rectangular input, experimental

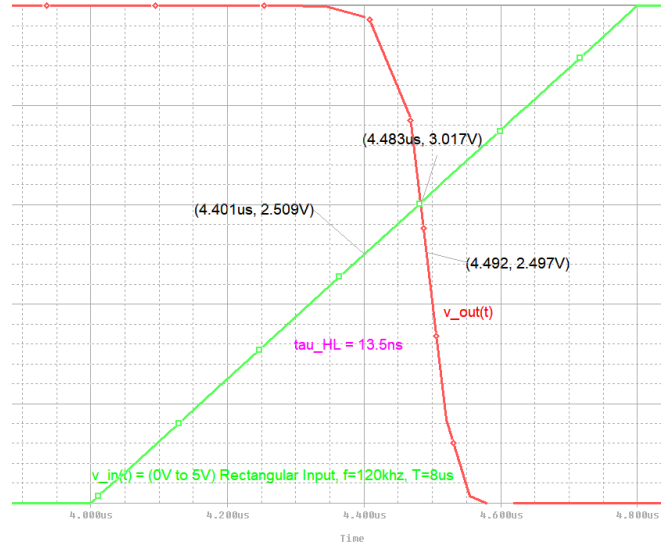


Figure 6. Case I - 5V, 122kHz, VTC simulation (High to Low)

Trace Color	Trace Name	X1	X2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	-12.317m	
CURSOR 2	V(V2+)	3.0740	2.5090	565.078m	577.396m	0.000	3.0740 2.5090 2.7915
CURSOR 1	V(M1:d)	2.4967	4.8900	-2.3934	0.000	2.3810	4.8900 2.4967 3.6933

Figure 7. Case I - 5V, 122kHz, VTC simulation data (High to Low)

Figure 7 shows propagation delay at the 50% point when the output goes from high to low. There is a typo in Fig. 6 for the value of tau, but we can see that from the data, there is about 90ns between the input and output which will be our τ_{PHL} value.

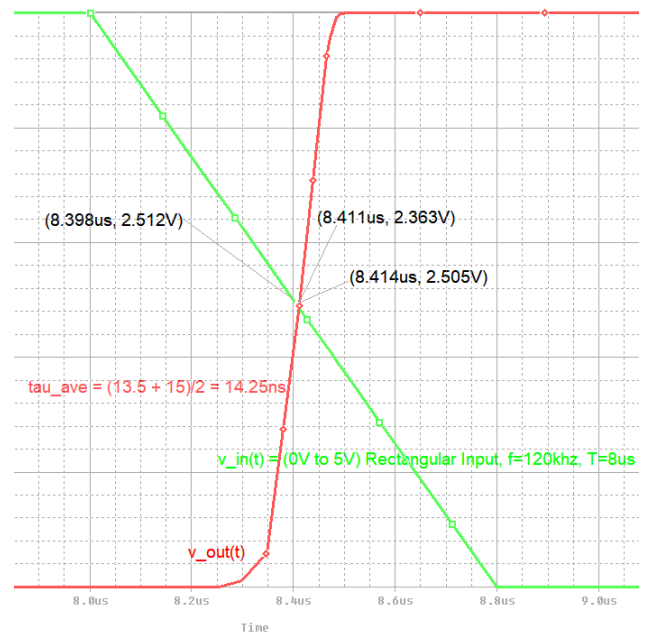


Figure 8. Case I - 5V, 122kHz, VTC simulation (Low to High)

Trace Color	Trace Name	X1	X2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 2	V(V2-)	2.4181	2.5124	-94.251m	-96.397m	0.000	2.5124	2.4181
CURSOR 1	V(M1.d)	2.5045	1.9547	549.796m	0.000	-557.651m	2.5045	1.9547

Figure 9. Case I - 5V, 122kHz, VTC simulation data (Low to High)

Here we see that $\tau_{PLH} = 15ns$, giving us a propagation delay of $\tau_P = (90ns + 15ns)/2 = 52.5ns$

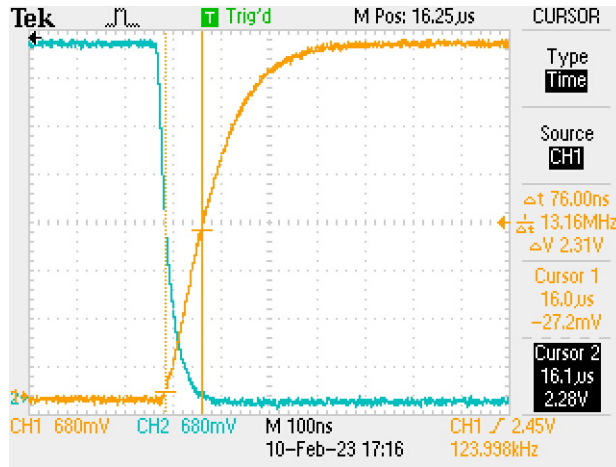


Figure 10. Case I - 5V, 124kHz, VTC experimental (High to Low)

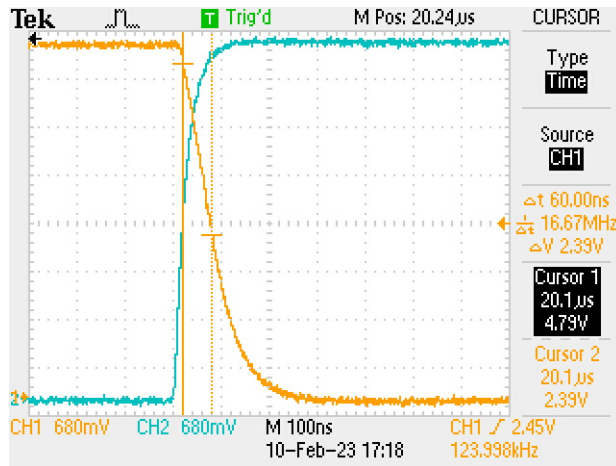


Figure 11. Case I - 5V, 124kHz, VTC experiemtnal (Low to High)

For the experimental case, we see that $\tau_{PHL} = 76ns$ and $\tau_{PLH} = 60ns$, giving us a propagation delay of $\tau_P = 68ns$

B. Case 2 ($300kHz \leq f \leq 500kHz$)

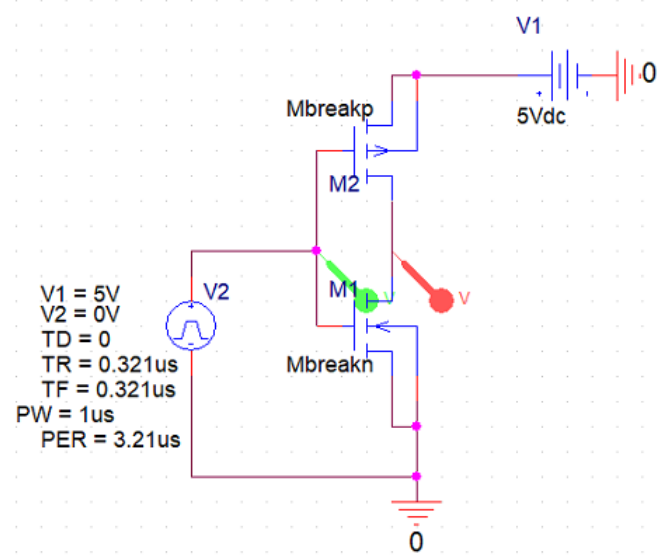


Figure 12. Case II - 5V Square input, $f = 312kHz$ and $t = 3.21us$

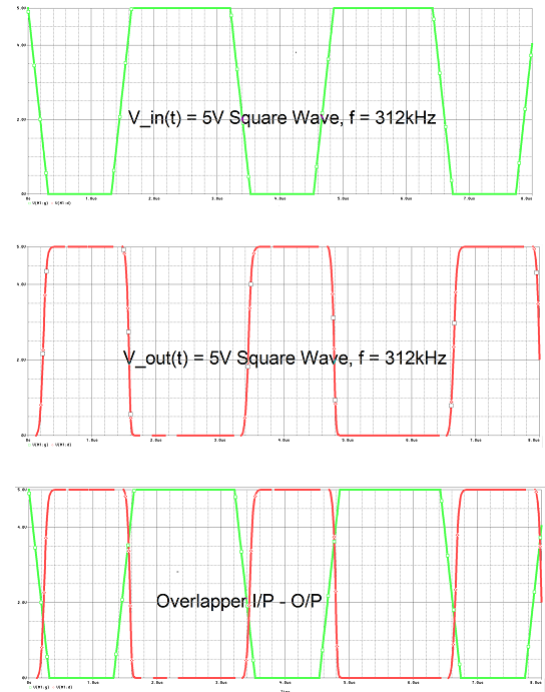


Figure 13. Case II - 5V Square input, $f = 312kHz$ and $t = 3.21us$, simulation

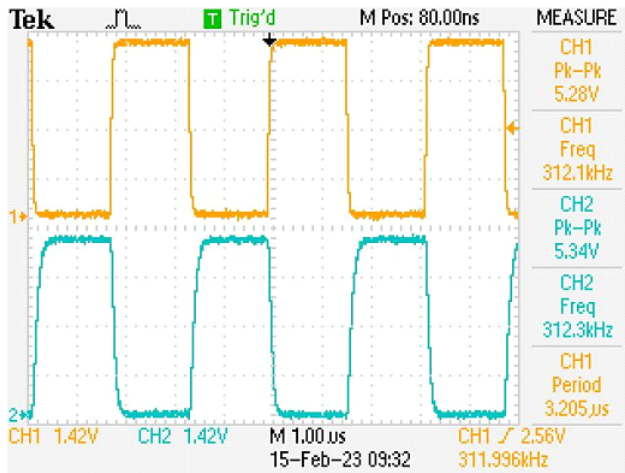


Figure 14. Case II - 5V Square input, $f = 312\text{kHz}$ and $t = 3.21\mu\text{s}$, experimental

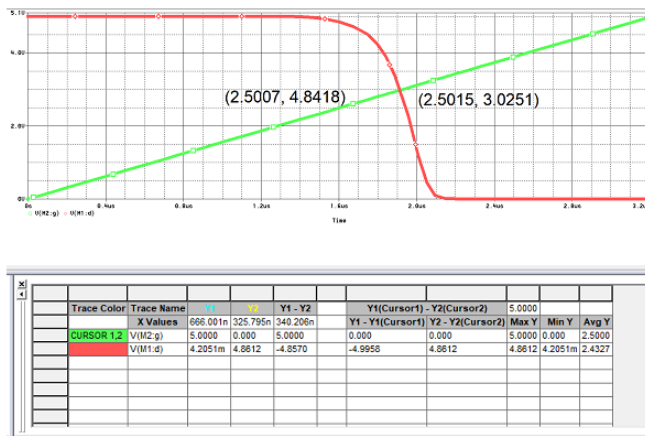


Figure 15. Case II - 5V, $f = 312\text{kHz}$, VTC simulation (High to Low)

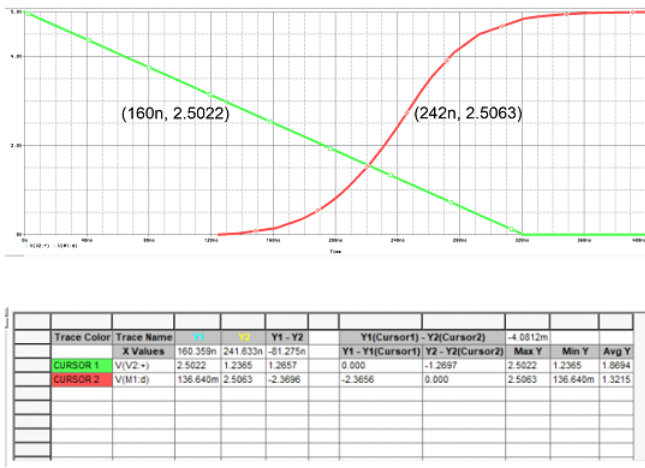


Figure 16. Case II - 5V, $f = 312\text{kHz}$, VTC simulation (Low to High)

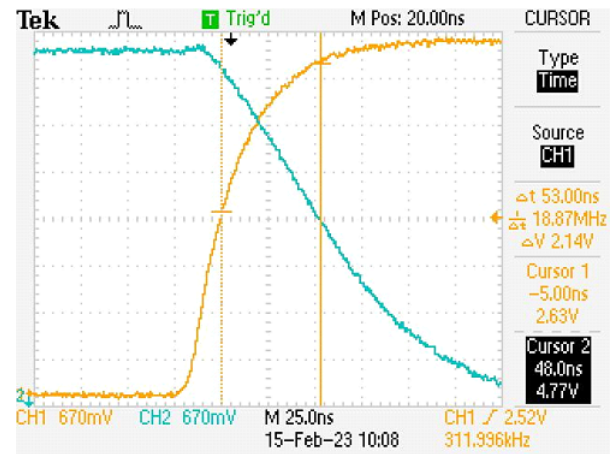


Figure 17. Case II - 5V, $f = 312\text{kHz}$, VTC Experimental (High to Low)

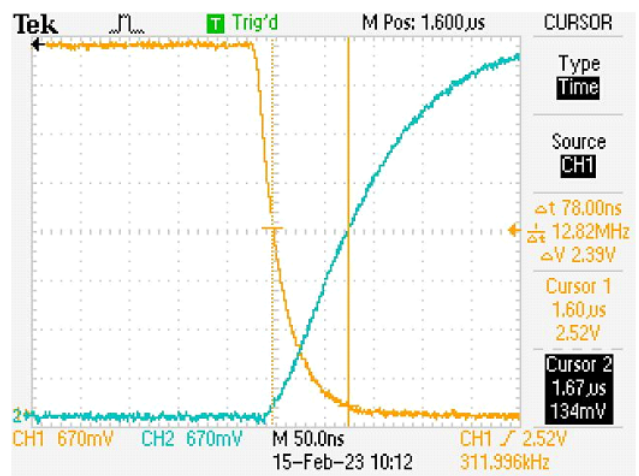


Figure 18. Case II - 5V, $f = 312\text{kHz}$, VTC Experimental (Low to High)

C. Case 3 ($600\text{kHz} \leq f \leq 800\text{kHz}$)

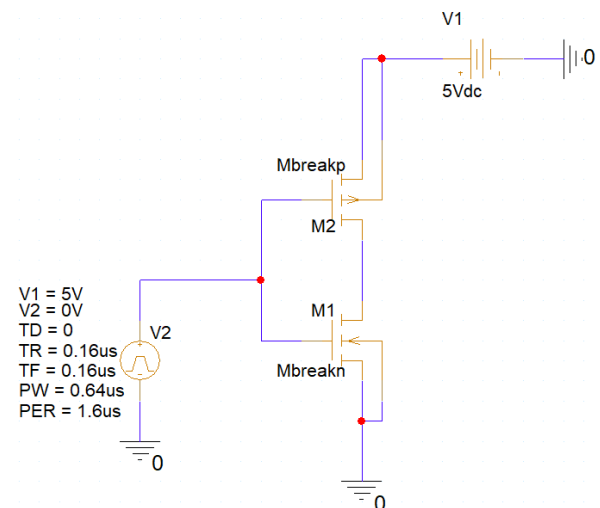


Figure 19. Case III - 5V, 622kHz Rectangular input

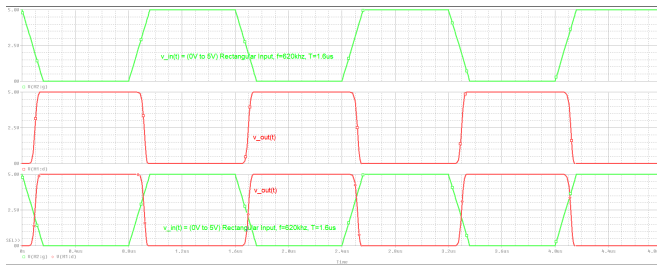


Figure 20. Case III - 5V, 622kHz Rectangular input, simulation

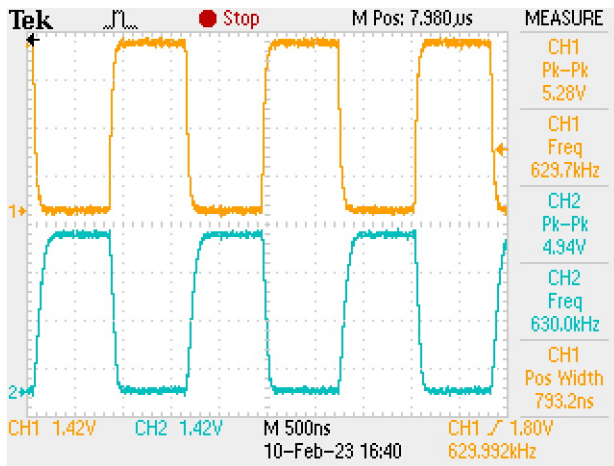


Figure 21. Case III - 5V, 630kHz Rectangular input, experimental

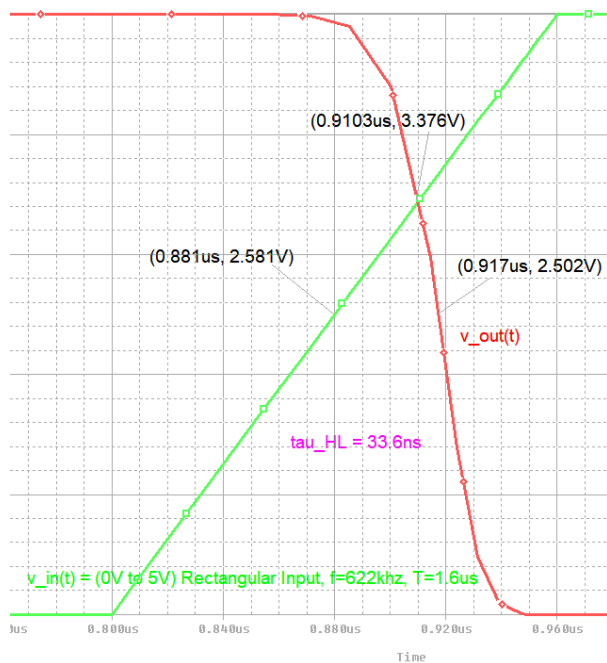


Figure 22. Case III - 5V, 622kHz, VTC simulation (High to Low)

Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	-7.8542m		
	X Values	917.208n	880.898n	36.310n	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y
CURSOR 2	V(M2.g)	3.6591	2.5281	1.1310	1.1389	0.000	3.6591	2.5281
CURSOR 1	V(M1.d)	2.5202	4.9307	-2.4105	0.000	2.4026	4.9307	2.5202

Figure 23. Case III - 5V, 622kHz, VTC simulation data



Figure 24. Case III - 5V, 622kHz, VTC simulation (Low to High)

Trace Color	Trace Name	Y1	Y2	Y1 - Y2	Y1(Cursor1) - Y2(Cursor2)	-7.8542m		
	X Values	1.6981u	1.6796u	18.449n	Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y
CURSOR 2	V(M2.g)	1.9390	2.5124	-573.359m	-565.505m	0.000	2.5124	1.9390
CURSOR 1	V(M1.d)	2.5045	643.047m	1.8615	0.000	-1.8693	2.5045	643.047m

Figure 25. Case III - 5V, 622kHz, VTC simulation data (Low to High)

Here we see that $\tau_{PLH} = 18\text{ns}$, giving us a propagation delay of $\tau_P = (36\text{ns} + 18\text{ns})/2 = 27\text{ns}$

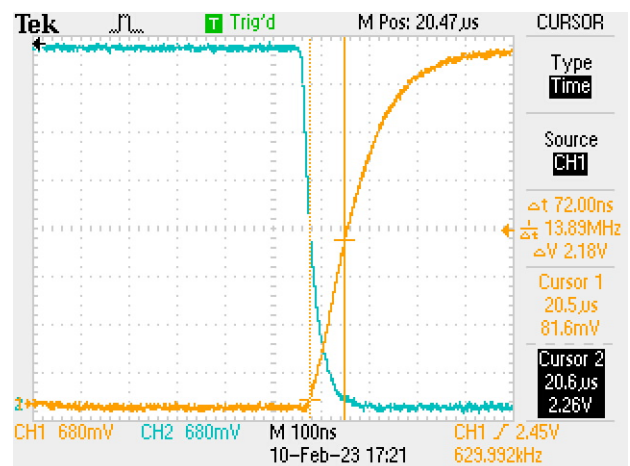


Figure 26. Case III - 5V, 624kHz, VTC experimental (High to Low)

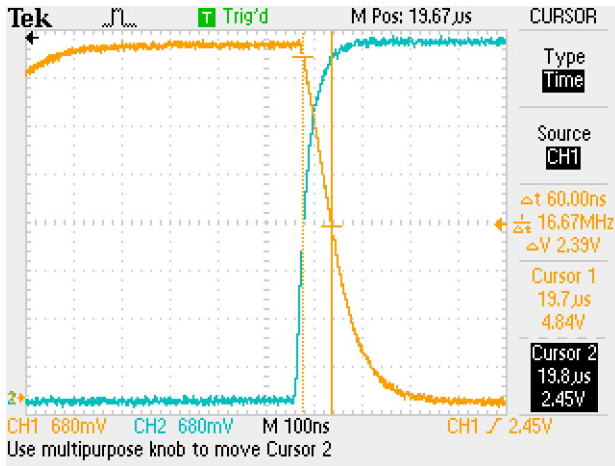


Figure 27. Case III - 5V, 624kHz, VTC experimtnal (Low to High)

For the experimental case, we see that $\tau_{PHL} = 72ns$ and $\tau_{PLH} = 60ns$, giving us a propagation delay of $\tau_P = 66ns$

D. Case 4 ($900kHz \leq f \leq 1.2MHz$)

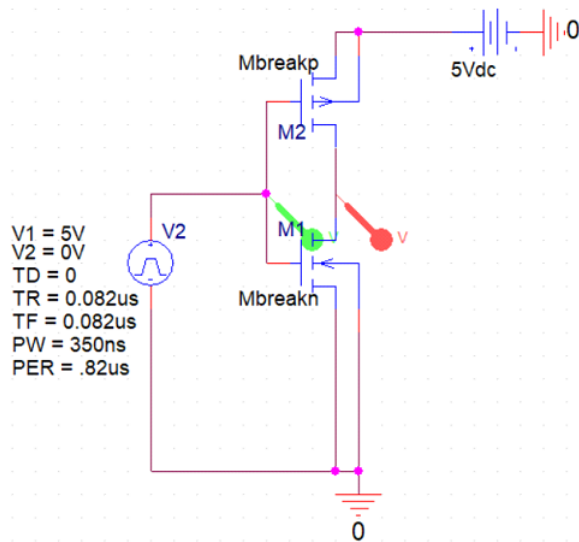


Figure 28. Case IV - 5V Square input, $f = 1.22MHz$ and $t = 0.82us$

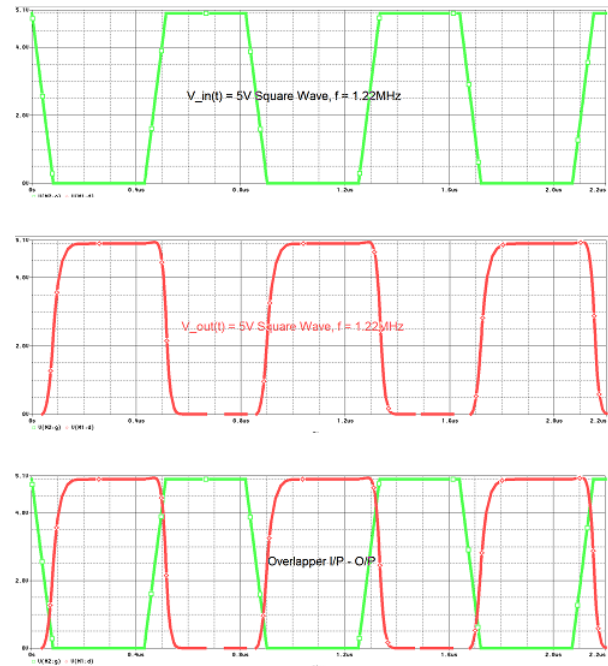


Figure 29. Case IV - 5V Square input, $f = 1.22MHz$ and $t = 0.82us$, simulation

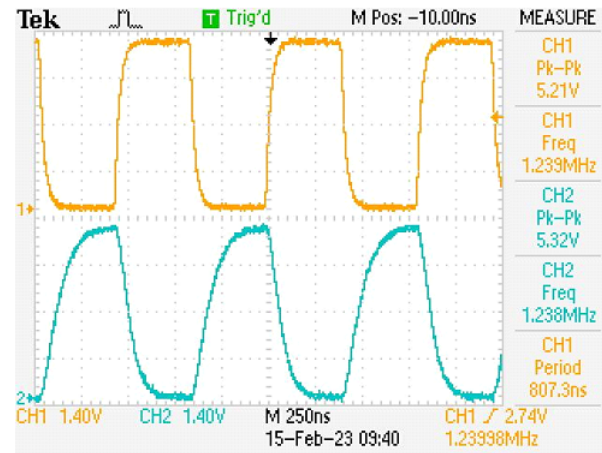


Figure 30. Case IV - 5V Square input, $f = 1.22MHz$ and $t = 0.82us$, experimental

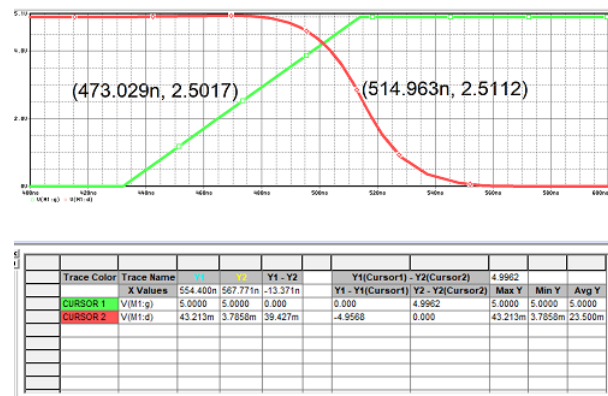


Figure 31. Case IV - 5V, $f = 1.22MHz$, VTC simulation (High to Low)

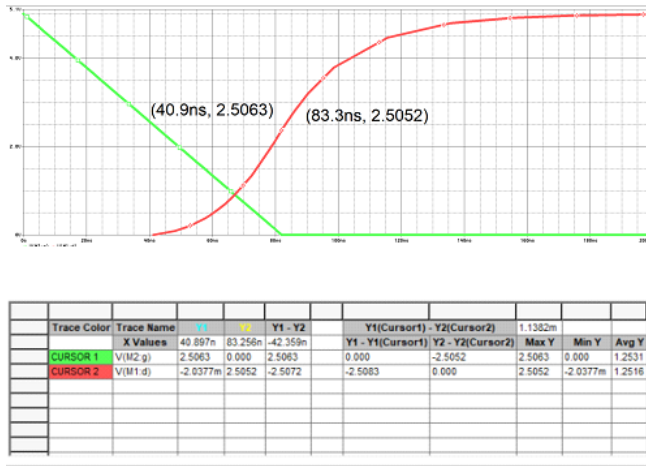


Figure 32. Case IV - 5V, $f = 1.22\text{MHz}$, VTC simulation (Low to High)

E. Ramp Case 1 ($80\text{kHz} \leq f \leq 100\text{kHz}$)

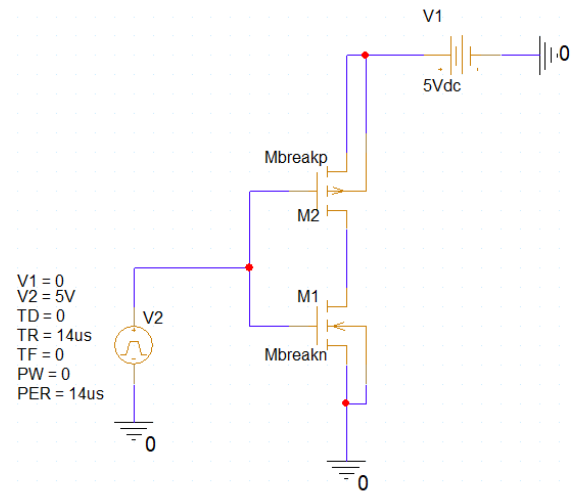


Figure 35. Ramp Case I - 5V, 80kHz Ramp input

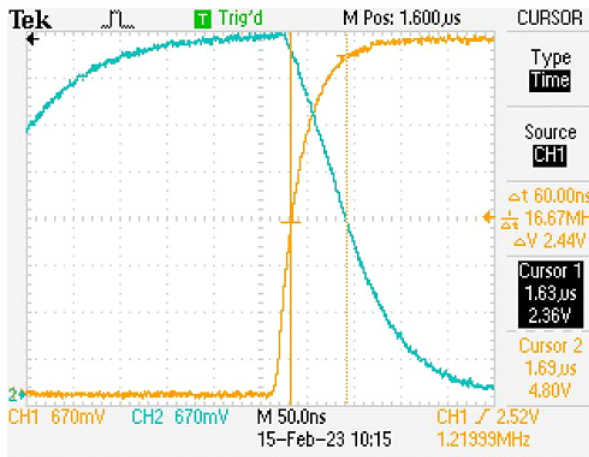


Figure 33. Case IV - 5V, $f = 1.22\text{MHz}$, VTC Experimental (High to Low)

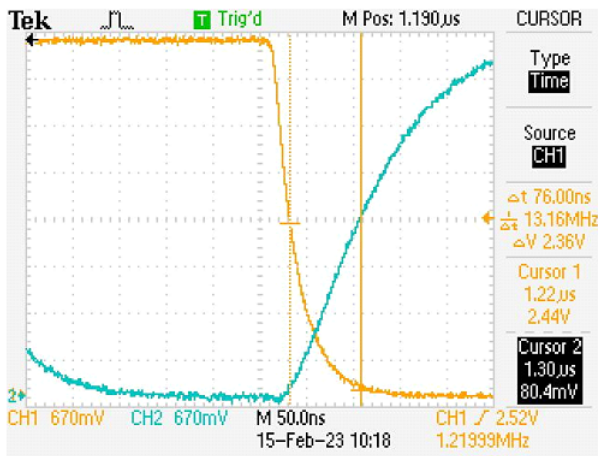


Figure 34. Case IV - 5V, $f = 1.22\text{MHz}$, VTC Experimental (Low to High)

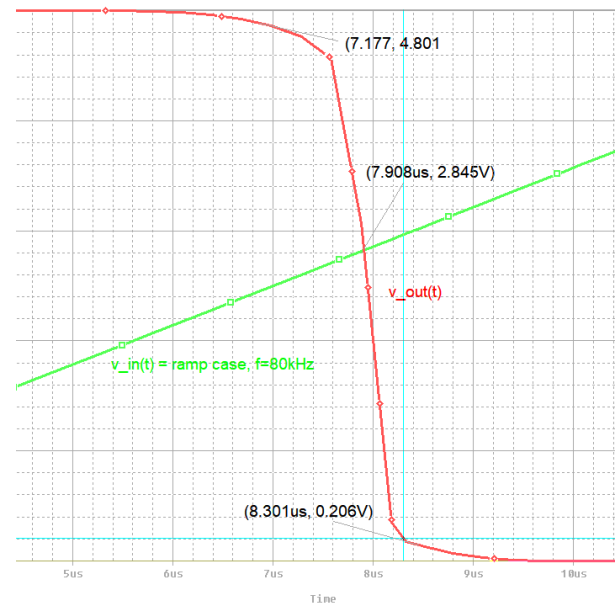


Figure 36. Ramp Case I - 5V, 80kHz Ramp input, simulation

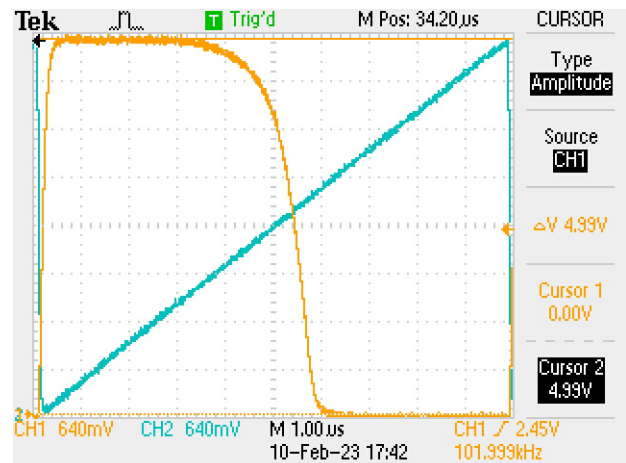


Figure 37. Ramp Case I - 5V, 100kHz, experiemtnal

F. Ramp Case 2 ($180\text{kHz} \leq f \leq 200\text{kHz}$)

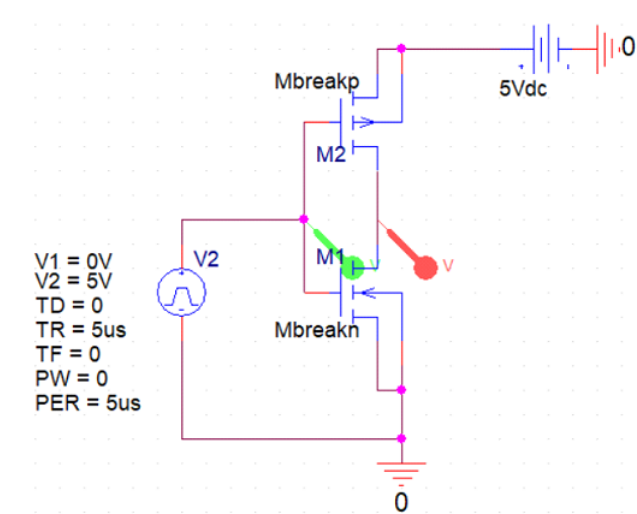


Figure 38. Ramp Case II - 5V Ramp input, $f = 200\text{kHz}$ and $T = 5\mu\text{s}$

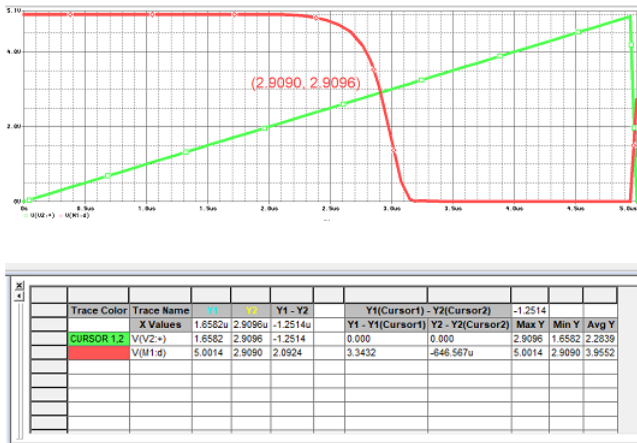


Figure 39. Ramp Case II - 5V Ramp input, $f = 200\text{kHz}$ and $T = 5\mu\text{s}$, simulation

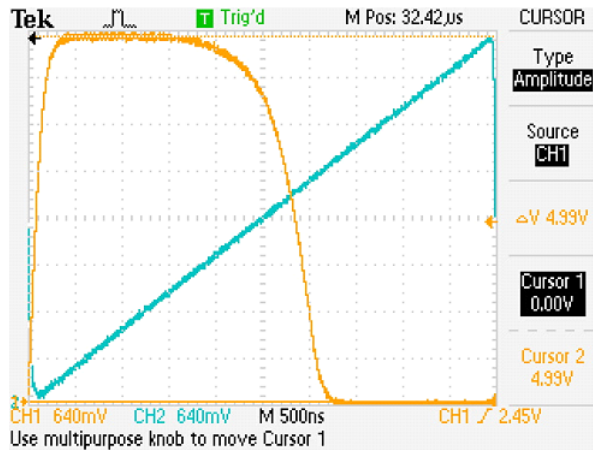


Figure 40. Ramp Case II - 5V Ramp input, $f = 200\text{kHz}$ and $T = 5\mu\text{s}$, experiemtnal

III. CONCLUSION

REFERENCES

[1] ECE 442L Manual
[2] ECE 442L supplementary slides
[3] Sedra, Adel S., et al. Microelectronic Circuits. Oxford University Press, 2021.